Analysis of the Low-Frequency Noise in Graded-Channel and Standard SOI nMOSFET

E. L. R. da Silva[a], M. Miguez[b], M. de Souza[a], A. Arnaud[b] and M. A. Pavanello[a]

[a] Department of Electrical Engineering, Centro Universitário da FEI, São Bernardo do Campo, Brazil

[b] Department of Electrical Engineering, Universidad Católica, Montevideo, Uruguay

In this paper a comparison between the low-frequency noise in graded-channel SOI nMOSFETs (GC SOI MOSFET) and standard fully depleted (FD) SOI nMOSFETs will be presented. The evolution of noise with bias and frequency, mainly in the GC SOI MOSFETs, will be demonstrated. Numerical bidimensional simulations are used to reproduce the same tendencies observed experimentally in order to allow for a physical insight on the noise in GC SOI transistors.

Introduction

Silicon-On-Insulator (SOI) nMOSFET with asymmetric doping concentration in the channel, so-called graded-channel (GC SOI MOSFET) and schematically shown in Fig. 1, has been developed in order to raise the drain breakdown voltage of fully depleted SOI transistors. In this structure, a length L_{LD} at the drain side is screened from threshold voltage ion implantation remaining with the intrinsic SOI substrate doping concentration, while the threshold voltage (V_T) implantation is performed at the source side of the device. In a first approximation, the lightly doped region can be understood as an extension of the drain region, reducing the effective channel length (L_{eff}). Several works shows promising results, indicating a significant improvement in the drain conductance and saturation current, as well as a substantial reduction in the occurrence of parasitic bipolar effects (1-2). These characteristics make this device very attractive for analog applications, as already demonstrated in operational transconductance amplifiers, current mirrors, common-drain amplifiers and RF circuits (3-7).

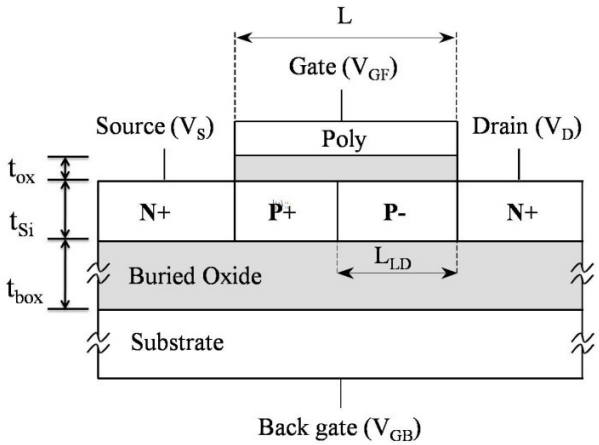

Figure 1. Schematic cross-section of graded-channel structure.

In recent years, the SOI technology has been showing great potential to be used in the manufacturing of integrated circuits with high degree of miniaturization (8), conquering a

firm place in the large-scale production of commercial ULSI circuits (9). Due to this evolution, noise research in SOI devices and technologies has boomed, especially flicker noise. In general, the flicker noise appears both through quality-dependent and fundamental noise processes. The 1/f noise is an important variable to investigate the analog performance of the devices. It is hoped that the transistors that are applied to analog circuits add little noise to the input signal in order to keep their fidelity.

Since the early days of the low-frequency noise research in MOS transistors, it has been demonstrated that the flicker noise dominates at the lower part of the frequency spectrum (f < 10 KHz). This type of noise is characterized by a current noise spectral density (SI) that reduces approximately according to $1/f^{\gamma}$ with the frequency exponent γ somewhere between 0.8 and 1.2 typically (10). The low-frequency noise is typically represented by its power spectral density, expressed in V^2/Hz or A^2/Hz.

In reference (11) the low-frequency noise behaviour of GC SOI nMOSFET was experimentally studied, demonstrating that to achieve high gain and low flicker noise in GC structure depends of optimal choice of the experimental conditions. In this reference the devices are biased with similar voltages, leading to different drain currents.

In this work an analysis of the flicker noise in GC SOI nMOSFETs in comparison to standard SOI transistors with same total channel length is presented. Experimental results obtained in saturation region are shown to support this analysis. Two-dimensional numerical simulations were performed aiming to extend the experimental analysis and reproduce the experimental results, both in saturation and linear region in order to allow for a physical insight on the noise origin.

Experimental Results

GC and standard SOI devices were fabricated starting from a SOI wafer with doping concentration of 10^{15} cm^{-3} and buried oxide thickness of 400 nm, with a 31 nm-thick gate oxide in a silicon layer with final thickness of 80 nm (12). The p-type threshold voltage ion implantation leads the body concentration level to about $6x10^{16}$ cm^{-3}. Both standard and graded-channel transistors present L = 2 μm and W = 20 μm. The measured GC devices present L_{LD}/L = 0.20 and 0.65.

Figure 2 (A) presents the drain current (I_{DS}) and the transconductance (g_m) as a function of the gate voltage obtained for standard and GC transistors in linear region with V_{DS} = 50 mV. From Figure 2 (A) it is clear that a GC devices exhibit higher transconductance than the standard SOI, due to the reduction of effective channel length. The same behaviour is observed in the drain current curves, as larger the L_{LD}/L ratio, higher is the drain current. Apart from the larger current level, from Figure 2 (B) it is possible to see the output conductance improvement and larger drain breakdown voltage promoted by the GC structure.

Figure 3 presents the noise spectra of one standard and two GC SOI transistors, with L_{LD}/L = 0.20 and 0.65. The noise measurements have been performed in saturation, short-circuiting gate and drain nodes and fixing the drain current, I_{DS} = 800μA. The noise was measured at the drain/gate node using the Agilent 4395A Spectrum Analyzer, after two stages of amplification.

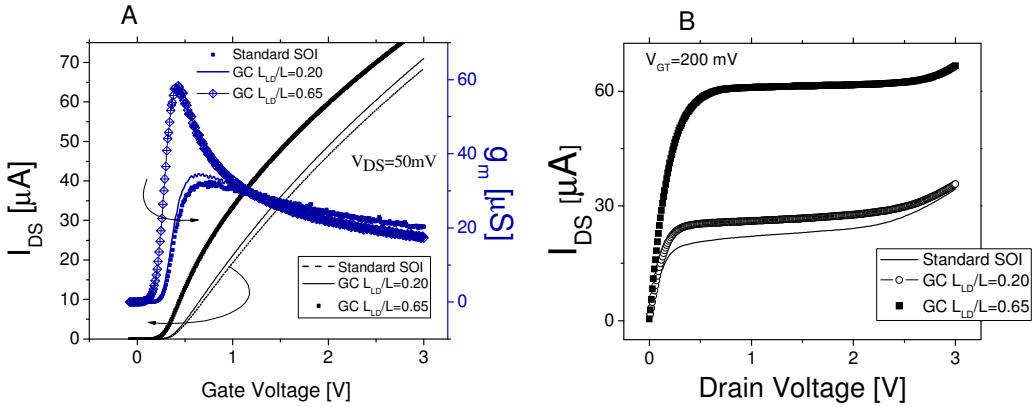

Figure 2. (A) Drain current and the transconductance as a function of the gate voltage, with L = 2 µm and V_{DS} = 50 mV. (B) Drain current *versus* gate voltage for a different L_{LD}/L of the GC SOI MOSFETs and Standard SOI MOSFET, with L = 2 µm and V_{GT} = 200 mV.

As seen in Figure 3, the current noise spectral density S_I reduces approximately according to 1/f, as expressed by the empirical relationship proposed by by Hooge:

$$S_I / I^2_D = \alpha_H / Nf \qquad [1]$$

As can be seen in the results presented in Figure 3, GC transistors present higher current noise density than standard SOI, and this worsening increases with L_{LD}/L ratio.

One of the advantages of GC nMOSFETs for analog applications is related to their improved g_m (7). However, as shown by equation [2] larger g_m results in a worsening of S_I, which could be a problem for low-noise applications. This increase can be observed in the expression of the current noise spectral density (13):

$$S_I = K_F \, g_m^2 / C_{oxf}^2 \, W \, L_{eff} \, f \, [2]$$

where K_F is a constant characteristic coming from the manufacturing process.

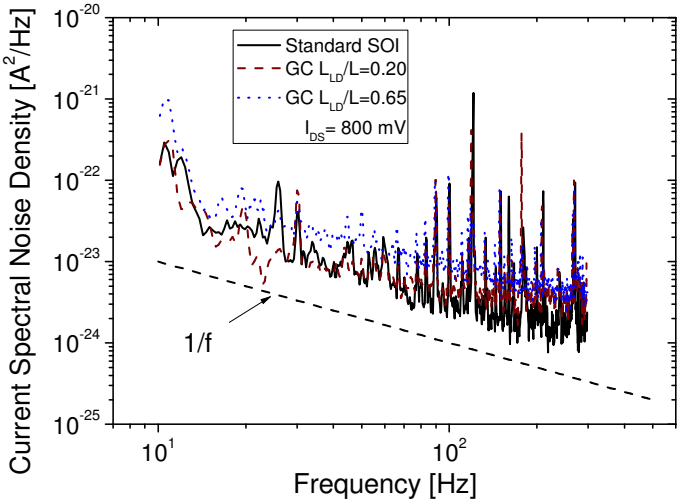

Figure. 3. Low-frequency noise spectra for a GC and standard SOI nMOSFET with L = 2 µm, biased in saturation, with I_{DS} = 800 µm.

Two-Dimensional Numerical Simulations Analysis

In order to extend the noise analysis in GC SOI transistor, two-dimensional numerical simulations were performed with Atlas simulator (14). The devices were simulated considering a total channel length L = 2μm. In the case of GC devices, different L_{LD}/L ratios were simulated (L_{LD}/L = 0.1; 0.2; 0.3 and 0.5). The gate oxide thickness is t_{ox} = 30 nm, the silicon thickness is t_{Si} = 80 nm, the buried oxide thickness is t_{box} = 390 nm, the p-type doping concentration is $N_A = 6 \times 10^{16}$ cm^{-3}, the intrinsic doping concentration is $N_{intrisic} = 1 \times 10^{15}$ cm^{-3} and the n-type doping concentration in the source and drain region is $N_D = 5 \times 10^{20}$ cm^{-3}. The models used account for the mobility dependence with horizontal and vertical electric field, and temperature, bandgap narrowing, Auger and SRH recombination and impact ionization. It is worthwhile mentioning that no optimization of model parameters have been made, which may affect the quantitative results but does not affect the qualitative analysis.

The device noise is obtained in Atlas by calculating the statistical behaviour of equivalent random current sources connected in its ports. The 1/f noise is based on the Hooge empirical model (15), whose value for the Hooge parameter is $\alpha_H = 2 \times 10^{-3}$ has been taken for both electron and holes (10). In the Hooge model, the flicker noise considers the influence of the random trapping and detrapping processes of charges in the oxide traps near the Si-SiO_2, attributed to mobility fluctuations of carriers of channel region.

Figure 4 presents the drain current I_{DS} (A) and the transconductance g_m (B) as a function of the gate voltage simulated for standard and different GC transistors in linear region with V_{DS} = 50 mV.

As illustrated in Figure 4 (A) it is clear that a GC device with L_{LD}/L = 0.5 exhibits a higher drain current, while the standard SOI has the lowest. This is the same that occurred in Figure 4 (B), the GC structure exhibits a higher transconductance (g_m) compared with the others.

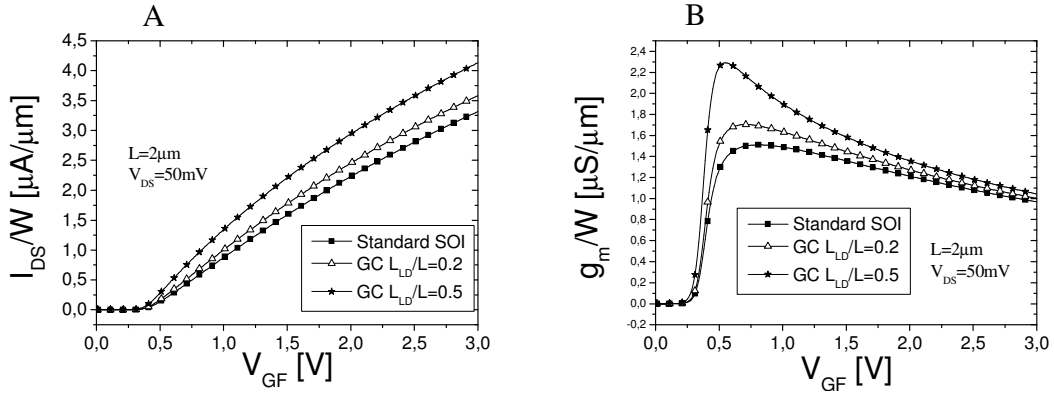

Figure 4. Drain current (A) and transconductance (B) *versus* drain voltage for a different L_{LD}/L of the GC SOI MOSFETs and Standard SOI MOSFET, with L = 2 μm and V_{DS} = 50 mV.

In Figure 5, it is possible to see the higher drain current for the GC structure with L_{LD}/L = 0.5. It is also possible to see in Figure 5 that the GC structure is better than

standard SOI, presenting a larger current level and breakdown voltage, similar as in the experimental data.

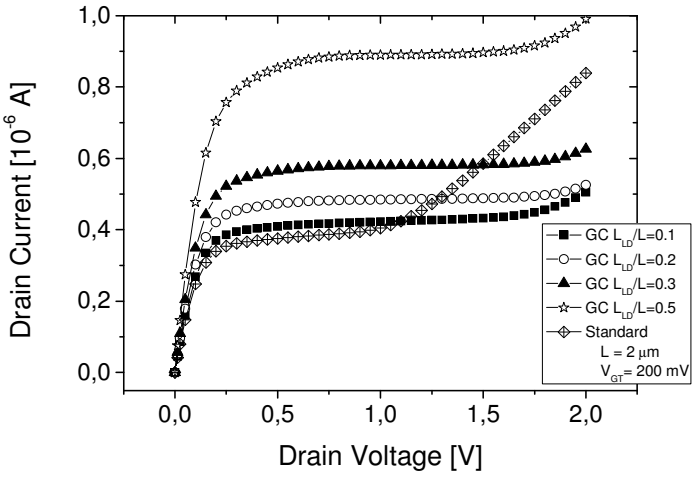

Figure 5. Drain current *versus* gate voltage for a different L_{LD}/L of the GC SOI MOSFETs and Standard SOI MOSFET, with L = 2 µm and V_{GT} = 200 mV.

Figure 6 presents the noise spectra for different GC SOI transistors, simulated in saturation, short-circuiting gate and drain nodes and imposing a fixed drain current, I_{DS} = 1 µA/µm. As can be seen in the presented results as the length L_{LD} is increased, higher noise is present in the transistor, as seen in the experimental measurements. This larger noise can be linked with the larger g_m of GC SOI (2).

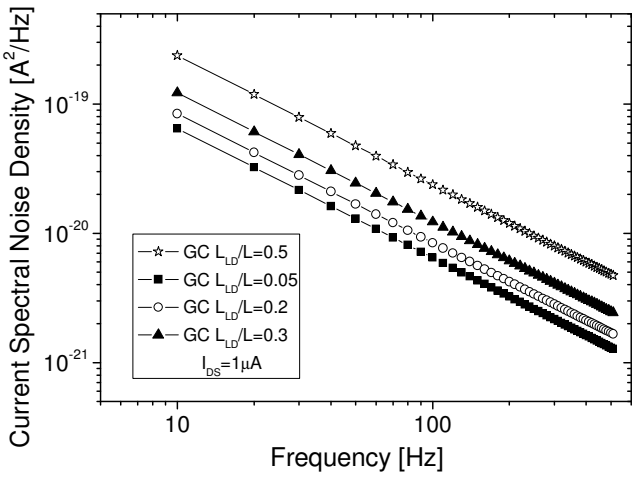

Figure 6. Low-frequency noise spectra for GC SOI nMOSFET with L = 2 µm in saturation, with I_{DS} = 1µA/µm.

Because of the inhomogeneous nature of the channel in saturation, the 1/f noise modeling becomes quite complex and results generally in dedicated, not user-friendly analytical solutions (16-17). Therefore, from this point on, all numerical simulations analysis will be made in linear operation.

In Figure 7, the current noise spectral density (S_I) in linear operation (V_{DS} = 25 mV and V_{GT} = 200 mV) is represented *versus* the frequency. This curve represents the

spectral density of the flicker noise. As shown by these results, GC transistors present larger noise density than the standard counterpart and it is worsened as the L_{LD}/L ratio increases. In addition, it is possible to observe that as in simulations, the GC structure presents higher noise than the standard SOI transistor.

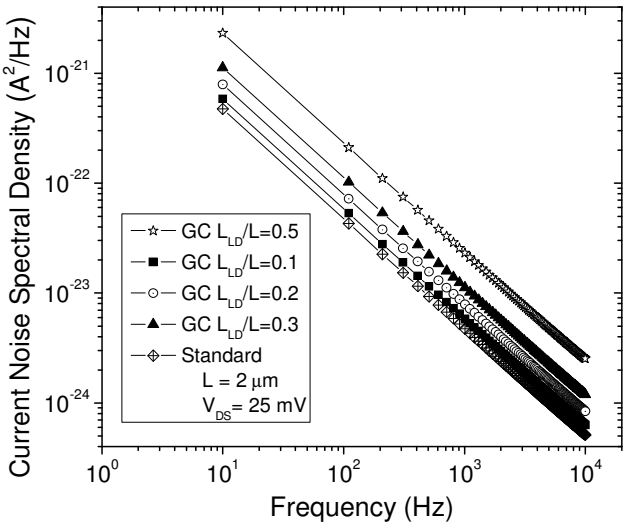

Figure 7. Current noise spectral density *versus* frequency in linear operation (V_{DS} = 25 mV and V_{GT} = 200mV) for different L_{LD}/L GC SOI MOSFET and a Standard SOI MOSFET.

In order to compare S_I taking into account the differences of drain current among the devices, Figure 8 presents the current noise spectral density as a function of the drain current. From these curves it is possible to note that for a fixed current, GC transistors present larger S_I than the standard device. For $I_{DS} = 1x10^{-10}$ A, S_I for the GC transistor with $L_{LD}/L = 0.5$ increases about 4 x 10^{-24} A^2/Hz in comparison to the standard device. In addition, it is possible to see that S_I increases with current level.

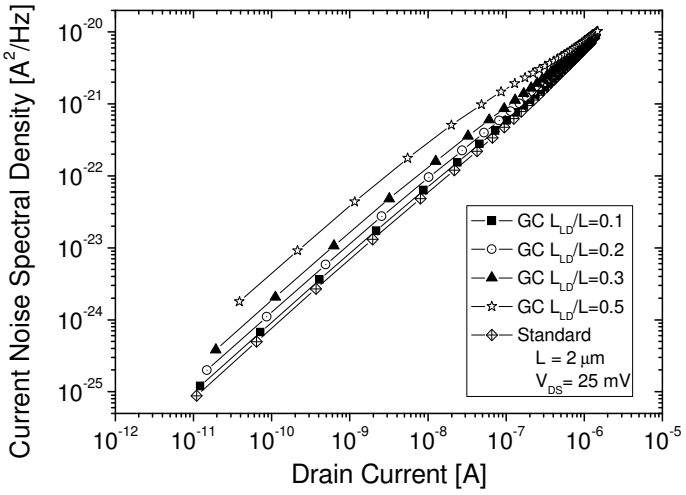

Figure 8. Current noise spectral density *versus* drain current in linear operation (V_{DS} = 25 mV and V_{GT} = 200mV) for different L_{LD}/L GC SOI MOSFET and a Standard SOI MOSFET.

The same worsening of noise figure with L_{LD}/L increase can be observed in the data shown in Figure 9, which presents S_I as a function of the normalized current drain (I_{DS} / (W / L_{eff})). From these results it is demonstrated that the noise is higher in the GC structure, even when the dimensions are withdrawn of the drain current, suggesting that the noise does not change when observed with the normalized current.

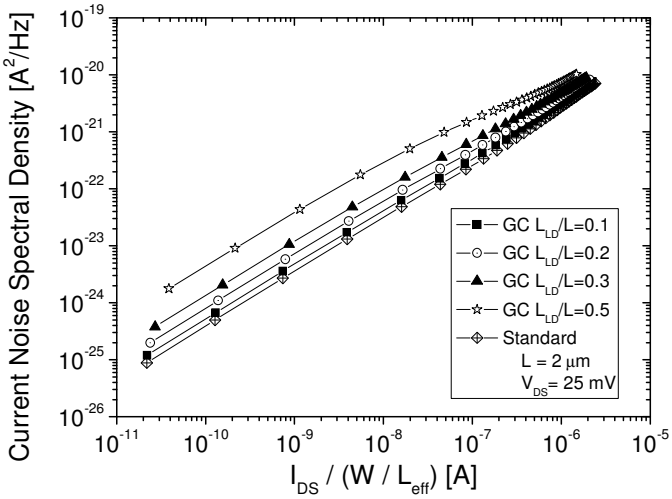

Figure 9. Current noise spectral density *versus* $I_D/(W / L_{eff})$ in linear operation (V_{DS} = 25 mV and V_{GT}=200mV) for different L_{LD}/L GC SOI MOSFET and a Standard SOI MOSFET.

Figure 10 presents the current noise spectral density as a function of the g_m/I_{DS} ratio. From these curves one can observe that the noise remains virtually unchanged in weak inversion and strong inversion independently on the device. For strong inversion, this behavior is related to the surface electron concentration along the channel from source to drain and different applied gate voltages (18). On the other hand, S_I is higher in moderate inversion, and this increase becomes higher for higher L_{LD}/L ratio. Comparing the GC device with L_{LD}/L = 0.5 and the standard one, there is an increase of 1.24 x 10^{-21} A^2/Hz at g_m/I_{DS} = 9.84 V^{-1}.

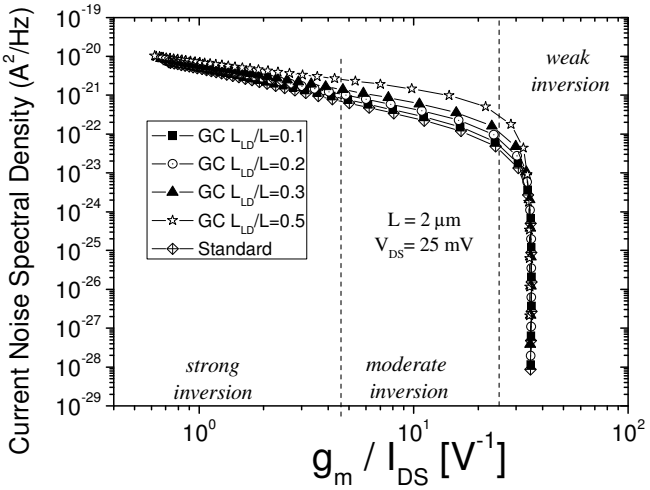

Figure 10. Current noise spectral density *versus* $I_D/(W / L_{eff})$ ratio in linear operation (V_{DS} = 25 mV) for different L_{LD}/L GC SOI MOSFET and a Standard SOI MOSFET.

Conclusions

This work presented an analysis of low-frequency noise in SOI transistors with asymmetrical doping concentration in the channel. Through experimental results it has been shown that although GC SOI MOSFET present better results in analog performance, it exhibits higher current noise spectral density, which could be a problem for low-frequency applications. Two-dimensional numerical simulation showed the same tendency observed in the measurements. It has been shown that the GC transistors present larger SI for a fixed current than the standard devices. In addition, it is possible to see that S_I increases with current level. Also S_I is higher in moderate inversion, and is as higher as larger is the L_{LD}/L ratio.

Acknowledgments

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