A Precision Autozero Amplifier for EEG Signals

Guillermo Costa
Departamento de Ingeniería Eléctrica
Universidad Católica del Uruguay
Av. 8 de Octubre 2801
Montevideo, Uruguay
+5982 4872717 / 407
gcosta@ucu.edu.uy

Alfredo Arnaud
Departamento de Ingeniería Eléctrica
Universidad Católica del Uruguay
Av. 8 de Octubre 2801
Montevideo, Uruguay
+5982 4872717 / 407
aarnaud@ucu.edu.uy

Matías Miguez
Departamento de Ingeniería Eléctrica
Universidad Católica del Uruguay
Av. 8 de Octubre 2801
Montevideo, Uruguay
+5982 4872717 / 409
mmiguez@ucu.edu.uy

ABSTRACT
Amplifiers for biological signals aimed to implantable medical devices require high gain and low noise, while maintaining very low power consumption. Therefore, a major challenge is the design of efficient low-noise circuits. These amplifiers work at low frequency ranging from sub-Hz to few kHz, thus besides the presence of thermal (white) noise, flicker noise (1/f noise) can be the largest. Autozero technique is used to reduce offset and flicker noise. However, a main issue in this kind of amplifiers is the aliasing of white noise inherit to the switching process, which increases the noise floor at low frequencies. In this work, the design of a low-noise amplifier for electroencephalography (EEG) signal recording is presented. The Autozero technique is applied to an instrumentation amplifier in the range of biological signals, with the addition of a low-pass filter in the noise cancellation feedback with the objective of reducing the impact of aliasing. Time domain simulations of the proposed amplifier show the benefits of the used architecture.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Style – Input/output circuits, VLSI.

General Terms
Design.

Keywords
Analog design, CMOS, low-power, low-noise, Autozero.

1. INTRODUCTION
A typical adult EEG signal is about $10-100\ \mu V$ in amplitude when measured from the scalp and about $10-20\ mV$ when measured from subdural electrodes [1]. At the low frequencies of EEG signals ($0{,}5\ Hz \sim 150\ Hz$), both thermal and flicker noise represent an important limitation [2][3]. Autozero (AZ) is a well known technique used to reduce flicker noise and offset in amplifiers [4][5]. It consists of taking successive samples of the amplifier's noise and subtracting them from the input signal. A typical AZ amplifier is shown in Figure 1, where $V_N(t)$ is the amplifier's input referred noise and offset voltage. The circuit works in two phases, during the *AZ phase* (very short in time) the amplifier is disconnected from the signal path and the value of V_N is sampled in the capacitor C. This value remains constant during the next phase, named *Amplification phase*, in which it is subtracted from the input signal V_{in}.

In Section 2, the design of an AZ-EEG amplifier is presented. First a continuous time (CT) amplifier (without AZ) is discussed, and then in Section 3 the AZ phase is incorporated. Because AZ amplifiers are affected by an excess of white noise due to aliasing, in the proposed amplifier a low-pass filter is included in the noise cancellation loop to reduce aliasing's impact. The amplifier was designed in a $0.6\ \mu m$ technology; it has a $40\ dB$ gain within $0.5\ Hz \sim 150\ Hz$, with a simulated input referred noise of less than $2\ \mu V_{rms}$.

1.1. Noise in Autozero amplifiers
The efficiency of the noise cancelation in AZ amplifiers depends on the autocorrelation of the noise source in the time domain. While offset is practically cancelled, flicker noise is high-pass filtered [4]. But in case of white noise, because there is no correlation between successive samples, AZ does not contributes to noise reduction and an excess of noise appears at low frequencies due to the effect of aliasing [4].

Denoting as $S_N(f)$ the PSD of the input referred noise V_N, and $H_0(f)$ the amplifier's transfer function, with no input signal the output PSD can be discomposed in two terms [4]: one caused by the band base noise attenuated by the AZ process, and other due to the noise aliasing:

$$S_{AZ} = |H_0(f)|^2 S_N(f) + S_{fold}(f) \quad (1)$$

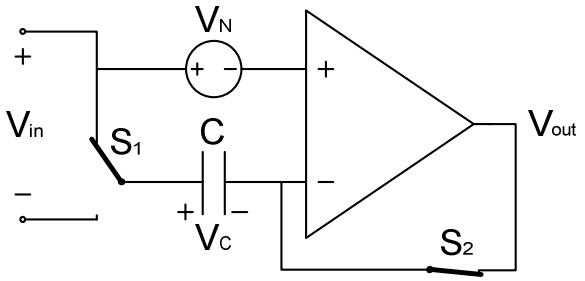

Figure 1. Scheme of an AZ amplifier.

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S_{fold} results from the sum of the successive shifts of the noise spectrum at n-times the AZ process frequency f_{AZ}. Analytic expressions of S_{AZ} depending on the noise source (white or flicker) derived in [4] are shown in Figure 2 and Figure 3 respectively. The plots are normalized against S_N, taking $f_C T_{AZ} = 5$ and $f_k T_{AZ} = 1$. T_{AZ} is the period of AZ process, f_k is the corner frequency of flicker noise and f_c is the bandwidth of the noise source. Note the remarkable increase of white noise as a result of the aliasing in Figure 2. In Figure 3, flicker noise is strongly reduced at low frequencies, although there is still a foldover component due to the aliasing of the $1/f$ tails.

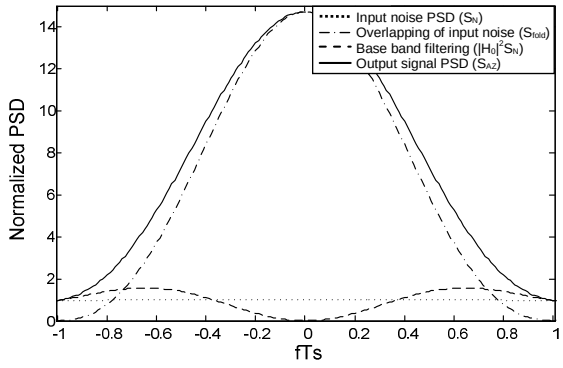

Figure 2. Autozero's response to white noise.

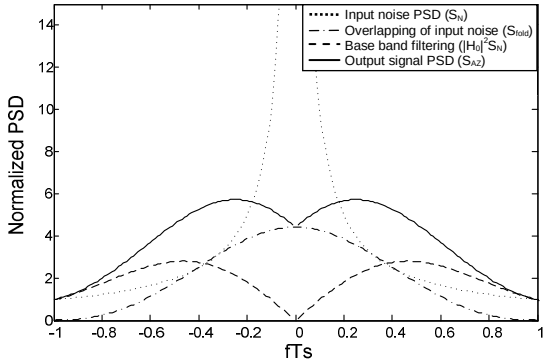

Figure 3. Autozero's response to flicker noise.

2. A LOW-NOISE AMPLIFIER FOR EEG SIGNALS (CONTINUOUS TIME)

The scheme of the proposed amplifier is shown in Figure 4. It is composed by a main amplification block designed as the triple differential input transconductor OTA shown in Figure 5, and a feedback loop $G_m - R$ to fix the gain. The third input will be employed in section 3 for the AZ feedback R_{AZ},C_{AZ}. The architecture is inspired in [6], where a low-distortion low-noise instrumentation amplifier is designed using a double differential input transconductor with a class AB output stage.

In Figure 5 the input V_1 is dedicated to the input signal to be amplified and V_3 to the $G_m - R$ feedback. The transconductor G_m in Figure 4 is a symmetrical OTA with a single input pair. The amplifier's output current i_o is given by:

$$i_o = (g_{m1}V_1 + g_{m2}V_2 + g_{m3}V_3)\frac{1}{B} \tag{2}$$

In (2) g_{m1}, g_{m2} and g_{m3} are the transconductances of the each MOS differential pair, while B is the copy factor of the NMOS current mirrors in Figure 5. Being G_m the transconductance of the OTA and C_L the load capacitance, during the amplification phase the transfer function between the output voltage V_o and the input voltage V_i is:

$$\frac{V_o}{V_i} = \frac{g_{m1}}{g_{m3}G_m R + BC_L s} \tag{3}$$

Equation (3) does not consider the internal poles of the amplifiers, since the one imposed by the load capacitance is much lower. The gain in (3) would have variations with the temperature and the fabrication process. However, these variations are not a problem in medical devices where calibration is necessary because of the variability of biomedical signals. For this application, the objective is the detection of the signal, instead of its exact value.

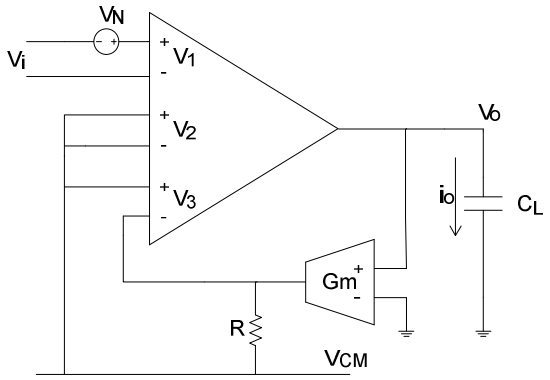

Figure 4. Designed amplifier for EEG signals.

2.1. Noise and offset analysis

A noise analysis over the amplifier was conducted separately for white and flicker noise. The transistor's noise is modelled as a noise current source in parallel, with a PSD given by:

$$S_{n_{white}}(f) = \gamma n k_B T g_m \tag{4}$$

$$S_{n_{flicker}}(f) = \frac{K_F g_m^2}{C'_{ox} WL} \cdot \frac{1}{f} \tag{5}$$

in case of white noise (eq. 4), and flicker noise (eq. 5). In (4) and (5) g_m is transconductance of the corresponding transistor, W and L are its width and length, k_B is the Boltzmann's constant, T is the temperature, n is the slope factor, γ = 2 or 8/3 depending on the transistor's operation region, K_F is a parameter of the process to be adjusted and C'_{ox} is the capacitance per area of the transistor's oxide.

In Figure 5, the input referred white noise voltage PSD can be calculated as:

$$S_{n_{input}}(f) = S_{n1}\left\{\begin{array}{c} 1 + \frac{(g_{m2}/I_{D2})}{(g_{m1}/I_{D1})} + \frac{(g_{m3}/I_{D3})}{(g_{m1}/I_{D1})} + \\ +3\frac{(g_{m4}/I_{D4})}{(g_{m1}/I_{D1})} + 3B\frac{(g_{m5}/I_{D5})}{(g_{m1}/I_{D1})} + \\ +3B\frac{(g_{m6}/I_{D6})}{(g_{m1}/I_{D1})} \end{array}\right\} \tag{6}$$

where S_{n1} is the noise voltage PSD generated by the first input stage M1A, M1B:

$$S_{n1}(f) = \frac{2\gamma n k_B T}{g_{m1}} \quad (7)$$

In (6), g_{mi} and I_{Di} are the transconductance and the bias current of each MiA and MiB transistor in Figure 5. From (6), the contribution of each pair of transistors in the total noise can be reduced by increasing the (g_{m1}/I_{D1}) ratio, while decreasing the (g_{mi}/I_{Di}) ratio for the remaining transistors. Therefore, the transistors of the input stage V_1 (M1A, M1B) were biased in weak inversion (WI) [7], those of the other two input stages (M2A, M2B, M3A, M3B) were biased in moderate inversion (MI) because this resulted in a good compromise between noise and power consumption, and the remaining mirrors in Figure 5 in strong inversion (SI). Bias currents were assigned according to the available power budget. The input referred noise from the amplification block was calculated by integrating the resulting PSD over the frequency range. From (5), to reduce flicker noise, the use of large transistors in the differential input stages is required [7]. However, in this case it is not necessary since flicker noise is supposed to be filtered by the AZ process. By reducing the total die area, the integration of multi-electrode systems is possible. It can be shown that with a careful design, the noise contribution of the OTA (G_m) and the resistor R in the feedback loop is negligible in comparison to the total noise of the amplifier.

The selected bias currents, transconductances and transistor sizes are shown in Table 1. The NMOS current mirrors copy factor B was taken equal to 2. The input referred white and flicker noise were estimated in 1.08 μV_{rms} and 3.70 μV_{rms} respectively. Thus for the CT amplifier, total rms noise in the band of interest is dominated by flicker noise. Considering the manufacturer's data for the fluctuations of threshold voltage V_T and current factor β of the process, the input offset voltage was estimated in $8.76\,mV$ (standard deviation).

From (3), once g_{m1} and g_{m3} were fixed, G_m and R were chosen to reach de desired gain of $40\,dB$ in the frequency band of interest. The selected values are $G_m = 0.193\,\mu S$ and $R = 1$ MΩ. The total current consumption is $1.89\,\mu A$.

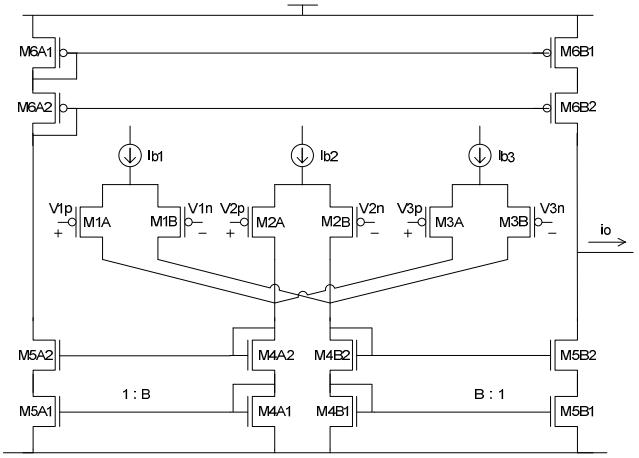

Figure 5. Scheme of the main amplification block.

Table 1. Selected parameters for the transistors of the amplification block.

Transistors	I_D (nA)	g_m (µS)	g_m/I_D (V^{-1})	W/L	W (µm)	L (µm)
M1A, M1B	335.0	8.27	24.70	19.347	58.0	3.0
M2A, M2B	33.5	0.34	10.15	0.082	3.0	36.8
M3A, M3B	33.5	0.34	10.15	0.082	3.0	36.8
M4A, M4B	402.0	2.00	4.98	0.066	6.0	90.0
M5A, M5B	201.0	0.10	4.98	0.033	3.0	90.0
M6A, M6B	201.0	0.10	4.98	0.097	6.0	62.0

2.2. Simulated transfer function

The simulated transfer function for the designed circuit is shown in Figure 6, for three different transistor models provided by the manufacturer: Typical Model (TM), Worst Slow (WS) and Worst Power (WP). Eldo [8] was used for all SPICE like simulations. The desired amplification gain is reached, with little variation in all three cases. The pole of the transfer function can be determined from (3) knowing the value of the load capacitor C_L, and it is approximately $1.04\,kHz$ with $C_L = 5pF$.

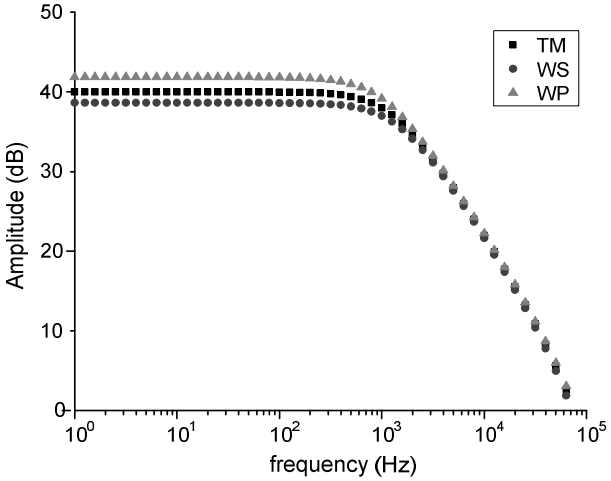

Figure 6. Simulated transfer function of the amplifier in Figure 4.

3. THE AUTOZERO AMPLIFIER

To reduce the impact of flicker noise, but also to cancel the offset that may produce the saturation of successive circuit stages, the AZ process was applied to the amplifier of Section 2. The complete scheme is shown in Figure 7, where minimum size transistors were used for the switches. It works in two phases: when Q1 is high and Q2 is low (AZ phase) the input signal V_{in} is disconnected and the amplifier's noise is followed by the RC circuit in the negative feedback across V_2. At the end of this phase, the final value on V_N is stored in C_{AZ}. When Q2 is high and Q1 is low (Amplification phase), the value on C_{AZ} is held and subtracted from input signal which is amplified; here the amplifiers behaves as described in section 2. The main difference with a regular AZ amplifier is that instead of instantaneously sampling the noise source, sampling process is done through a $R_{AZ}C_{AZ}$ circuit, which is being commuted between both phases.

This low-pass circuit has a benefit, because V_N will be followed more smoothly. In effect, if a large time constant $\tau = R_{AZ}C_{AZ}$ is selected, instead of samples, a low-pass then hold structure is included in the AZ loop, which limits the effect of the aliasing by reducing the sampled noise bandwidth. The AZ principle is preserved but the impact of white noise due to aliasing is reduced.

During the sampling phase, the transfer function between the voltage V_c on the capacitor C_{AZ} and the noise source V_N is given by:

$$\frac{V_c}{V_N} = \frac{g_{m1}}{BC_{AZ}.s + g_{m2}} \tag{8}$$

So, at the end of the AZ phase the value of V_N will be stored in C_{AZ} multiplied by the ratio between the transconductances of the input stages V_1 and V_2:

$$V_c \rightarrow \frac{g_{m1}}{g_{m2}} V_N \tag{9}$$

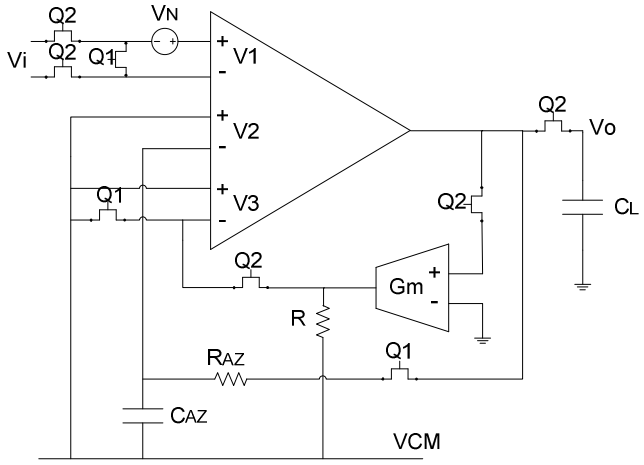

Figure 7. Complete design of the EEG amplifier including AZ process.

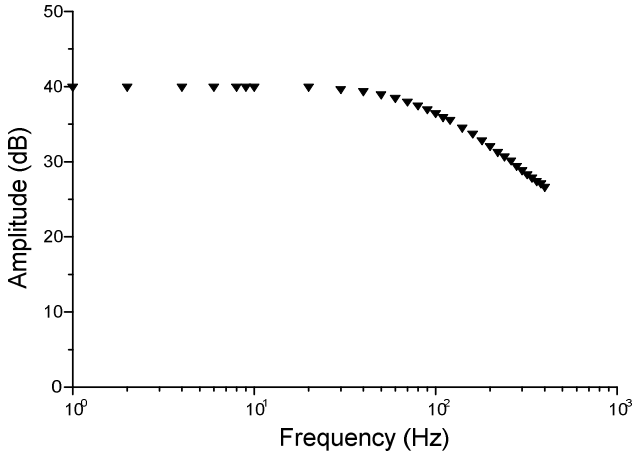

Figure 8: Amplifier's transfer function with AZ.

3.1. Complete amplifier simulations

In Figure 8, the transfer function of the amplifier including the AZ process is shown. Since the circuit is now being commuted, it is not possible to obtain the transfer function from an AC SPICE analysis. Thus, each point of the plot in Figure 8 corresponds to a single time domain transient simulation, in which the amplification gain was derived from the relation between the output and input signals amplitude. As expected, at low frequency the gain is equal to the gain of the amplifier without AZ.

In Figure 9 and Figure 10, two transient simulations of the amplifier are shown. In both of them a particular signal V_N was included at the amplifier's input like in Figure 7, to simulate the input referred noise. V_c is the voltage of the capacitor C_{AZ}, and V_o is the output voltage on the load C_L (Figure 7). The input signal employed in the simulation was a $100\ \mu V$ sine wave, of $20\ Hz$ and $3\ V$ common mode.

In Figure 9, the noise signal V_N is just a $10\ mV$ DC offset. The small signal voltage on C_{AZ} is given by (9), where $g_{m1}/g_{m2} \approx 19.7$. So $V_c \approx 3V_{DC} + (19.7) \times 10mV \approx 3.197\ V$, which is exactly the value of V_c in Figure 9. On the other hand, the undesired offset does not appear at the output V_o, and only the input signal amplified by 100 does.

The same simulation is repeated but considering a sine wave noise signal V_N of low frequency (a component of flicker noise), and the result is shown in Figure 10. The voltage V_c follows the noise signal (by small periods of sampling) and it is totally cancelled in the output signal V_o, resulting once again only the amplified input signal. As a result, the AZ process on the amplifier effectively filters both offset and low frequency noise.

3.2. Noise time domain simulations

Because the designed amplifier is not a time invariant system, the input noise of the complete circuit in Figure 7 cannot be estimated with regular SPICE simulator tools. Instead, time domain simulations were performed using a MATLAB program that emulates the AZ amplifier operation and a simulated random input that follows either white o flicker noise statistics. The search for optimums values of R_{AZ} and C_{AZ} was also carried with the aid of MATLAB, looking for a minimum in the input referred noise voltage. The switching frequency f_{AZ} and the duty cycle d were also varied: $v_{noise\_rms} = f(R_{AZ}, C_{AZ}, f_{AZ}, d)$. The selected values for the AZ are: $R_{AZ} = 1\ M\Omega$, $C_{AZ} = 10\ pF$, $f_{AZ} = 15\ kHz$, $d = 82\%$.

In Figure 11 the simulated total noise PSD of the amplifier is shown. Note the difference with Figure 2 and Figure 3 due to the low-pass AZ loop. The total rms noise voltage when integrating the plot in Figure 11 from 0.5 to $150\ Hz$ results $v_{in\_total} = 1.6\ \mu V_{rms}$.

In comparison to the CT amplifier of Section 2, noise was reduced because of flicker noise cancellation. On the other hand, if a traditional AZ is employed (instant samples) instead of the selected $R_{AZ}C_{AZ}$ network, the total estimated noise would have been $2.25\ \mu V_{rms}$. Thus for this case, the use of the band limited AZ sampling result a valuable option.

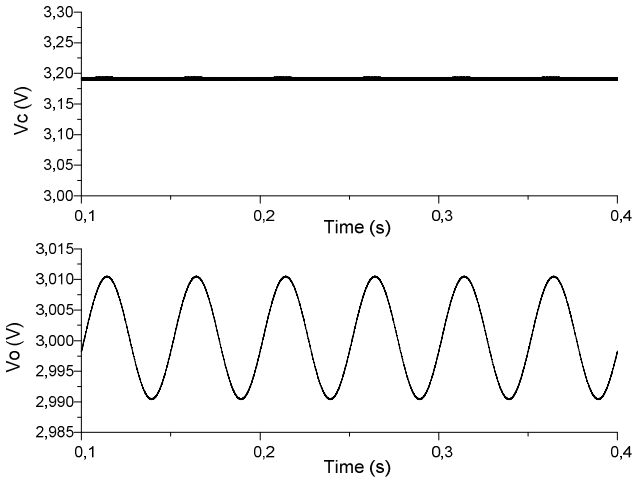

Figure 9. Amplifier's transient simulation with simulated offset V_N.

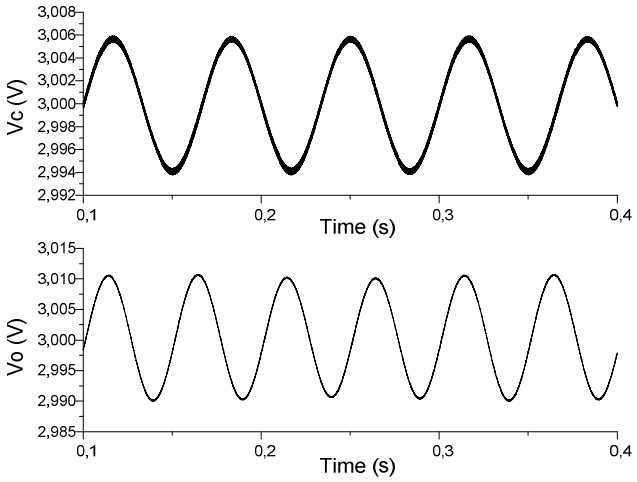

Figure 10. Amplifier's transient simulation with a simulated low frequency noise signal V_N.

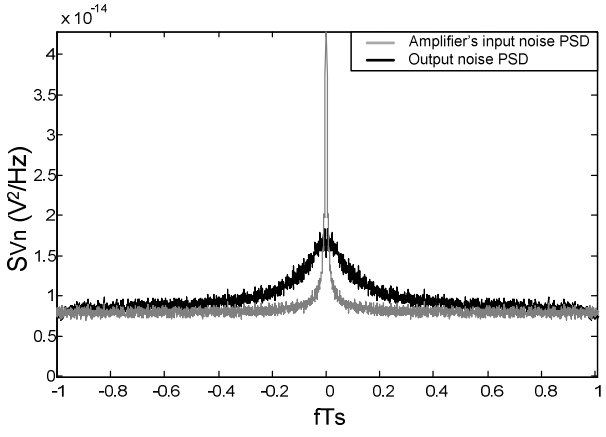

Figure 11. Output PSD considering both white and flicker noise.

4. CONCLUSIONS

The design of an EEG amplifier using a novel AZ topology was presented. The circuit is currently being fabricated in a 0.6 μm CMOS technology. The designed circuit is low-pass, with a 40 dB gain. It has a 1.6 μV_{rms} input noise voltage in the range from 0.5 to 150 Hz, and has 6.8 μW total power consumption from a 3.6 V supply voltage V_{DD}.

It has been demonstrated that the addition of a commuted low-pass filter in the AZ cancellation network has a positive impact in the reduction of white noise aliasing, while preserving AZ characteristics.

The future work includes to continue the study of the proposed technique for a better theoretical comprehension and design space exploration, as well as to improve the EEG design by lowering the supply voltage for a further power consumption reduction.

5. AKNOLEDGMENTS

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