A self-protected integrated switch in a HV technology

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ABSTRACT
An integrated switch to control electrical stimuli in implantable medical devices is presented in this work. First a self-biased protection mechanism to avoid V_{GS} reaching maximum rated value is presented. Then, using a HV-CMOS technology this technique is incorporated in a fully integrated switch, to control 0 to 16V, and 0 to 30 mA, pulses for implantable stimulators. Because of the low supply voltage V_{CC} between 2 to 5V, and safety considerations in implantable devices, special level shifters, drivers, and a voltage multiplier, that drive a large 40000µm/3µm dual PMOS switch, were necessary for the circuit.

Categories and Subject Descriptors
D.3.3 [**Programming Languages**]: Language Contructs and Features – *abstract data types, polymorphism, control structures.* This is just an example, please use the correct category and subject descriptors for your submission. The ACM Computing Classification Scheme: http://www.acm.org/class/1998/

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1. INTRODUCTION
Modern CMOS technology usually incorporates thick oxide possibility to allow certain transistor gates to be driven by higher voltages. In a deep submicron technology, a thick oxide may allow 5V inputs, and in the so called High Voltage (HV) technologies the limit is extended to 12 or 18 Volts, now we will focus on the latter. In a typical HV CMOS transistor, the drain may support up to for example 20 or 60 Volts V_{DS} but gate to source and bulk voltage is limited by the gate oxide strength.

In mixed mode circuits, low voltage logic drives high voltage transistors, usual level shifters can translate between different voltage levels below the maximum rated V_{GS} voltage for the thick oxide. To translate larger voltages, a bit more complex circuit techniques should be employed [1] that normally rely in current signalization and assume a fixed high-side voltage that are not always present.

In this paper a novel circuit will be presented to deal with large voltages using CMOS transistors. The idea can be summarised as follows: consider a PMOS transistor, to turn it off, the gate and the source can be connected to each other; to turn it on, the gate is pushed as much as possible to the most negative voltage in the circuit. There is a control loop that stops pushing the gate to the negative voltage if the source to gate voltage becomes close to the maximum rated V_{GS} value for the technology. In this way the PMOS is turned on with a maximum V_{GS} voltage ensuring a minimum on-resistance.

In Section II, the circuit technique will be applied to a PMOS integrated switch that is part of an implantable medical device. Most implantable medical devices, are electrical stimulation systems, that deliver either current or voltage pulses to the patient according to different requirements. Stimuli section of the circuit may consist of the basic elements shown in Figure 1: a stimuli generator (either a voltage or current source), electrodes which connects the tissue to the device, a switch that toggles the electrical connection of the electrodes, and a control block that decides when and for how long a stimulus should be applied. Stimulation can be done either by applying a voltage in the tissue from a few mV to well over 10 V or driving a current through it, ranging form a few µA to tens of mA. A high voltage (HV) 0.6 µm CMOS technology was selected to allow switching up to 16V stimuli.

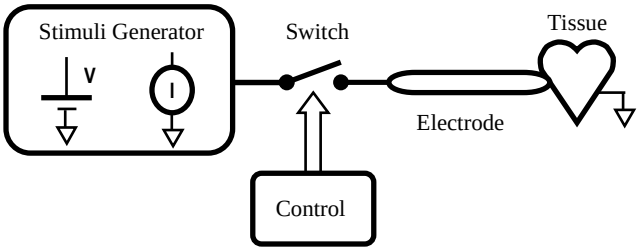


Figure 1. Typical stimuli section of implantable medical device.

SBCCI'09, August 31st - September 3rd, 2009, Natal, RN, Brazil.

1.1 A novel V_{GS} overvoltage protection circuit

The circuit in Figure 2 shows a PMOS switch M1, which may be a large output driver transistor that may connect the voltage V_{IN} to V_{OUT}. While V_{DS1} (V_{IN}-V_{OUT}) may be large for example up to 50V in a HV technology, V_{GS1} is limited to a much lower value, 5V in standard CMOS to 12-18V in a HV technology. To turn on M1, a driver may connect its gate to V_{SS} (the most negative voltage in the circuit) but there is a risk of gate puncturing if V_{GS1} exceeds maximum rating. To overcome this problem a voltage control loop is proposed. V_{CTRL} is a low voltage logic signal varying between a low voltage V_{CC} (i.e. 3 V) and V_{SS}; when V_{CTRL} = V_{CC} M2 is turned on if I_{Ref} = 0 thus pushing V_{G1} to V_{SS}, and turning on M1. But as I_{Ref} increases, the voltage drop through R1 increases as well, and M2 resistance dramatically increases (up to cutoff) and V_{G1} may reach an equilibrium voltage well above V_{SS}. I_{Ref} is a function of V_{GS1} voltage because of the n diode-connected M_{di} transistors, which copy their current to the V_{G2} node through M_{ci} transistors. As V_{GS1} increases, I_{Ref} increases in a strongly-non linear way, and an equilibrium V_{GS1} voltage close to the voltage drop of the stacked M_d diodes is achieved. V_{GS1} voltage during M1 conduction is a function of n, the number of stacked M_d transistors, their threshold voltage and M2, R1 characteristics. These circuit elements should be designed according to rated V_{GS} voltage for the technology and corner cases. When V_{CTRL} = V_{SS}, M2 transistor is opened and R2 pushes V_{G1} to V_{IN} thus M1 is opened. R2 has been placed to illustrate circuit operation but may be substituted by a more complex circuit to avoid static current consumption when M1 is turned on, or to increase speed. Note that this control loop also draws some current when M1 is on (that can be minimum with a careful design), but may operate regardless of the VIN value ranging to an arbitrarily large value. A modified version of the circuit in Figure 2 will be employed in the following section, to implement a stimuli delivery switch for implantable medical devices in a HV technology.

Finally it should be pointed that in regular switching applications M1 size is very large thus validating the use of the extra circuit elements count. In the example of section II a large M1 (W/L = 40000µm/3µm) dual transistor is employed, and the control loop area is much smaller.

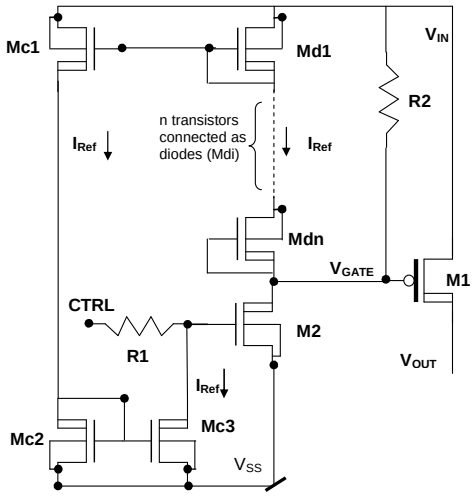


Figure 2. Proposed control loop for VGS over-voltage protection.

1.2 HV-Technology

Introducing new layers, a HV CMOS technology allows the fabrication of devices that can support elevated voltages, in the selected technology up to 50V. Regular 5V CMOS core can also be fabricated, as well as double poly capacitors and high-resistivity poly resistors. As an example, in Figure 3 a HV NMOS transistor, named nhv, vertical cut is shown. Nhv has the regular structure of a HV transistor, incorporating a thick gate oxide that enables up to 18V V_{GS}, V_{GB} voltage values, and the drain diffusion is growth into a NWELL to complete a diffused Drain to support elevated V_{DS} voltages. As different kind of transistors are used (HV transistor and the standard 5V one), in Figure 4 the symbols used for each case are shown. HV transistors are not symmetrical, the drain which is designed to withstand the highest voltage, is marked with a double line.

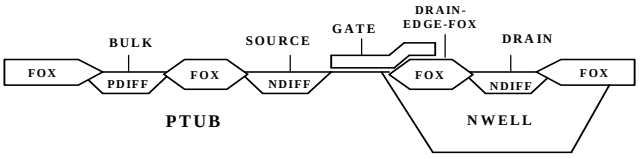


Figure 3. Vertical cut of a typical HV NMOS (NHV).

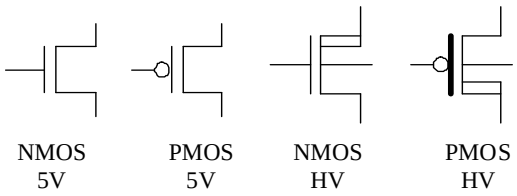


Figure 4. Symbols for the different kinds of transistors.

2. AN INTEGRATED SWITCH FOR IMPLANTABLE MEDICAL DEVICES

All The circuit is simply a switch that can connect/disconnect the electrodes from the electric pulse generator in Figure 1. In Figure 5 a detailed scheme is shown. A microcontroller commands this special switch through the CTRL signal.

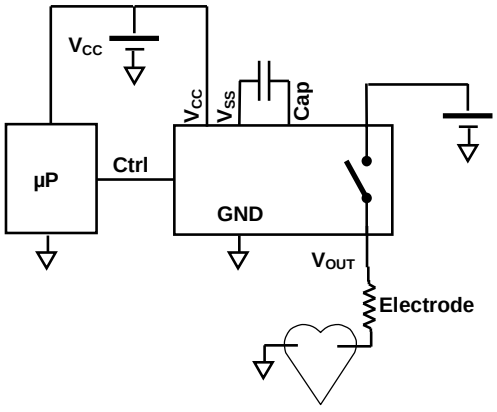


Figure 5. Typical application for designed switch.

Initial specifications are the following:

- The switch must operate correctly with commutation voltages V_{IN} from 100 mV to 16V.
- It must work with supply voltage V_{CC} from 2V (end of life of a lithium-iodine pacemaker like battery) up to 4.2V (a fully charged rechargeable medical grade battery) [2], [3].
- The switch must have an ohmic resistance of 5 Ω or less, in all ranges of operation. As voltage bellow GND were necessary to fulfil this requirement, a voltage inverter that generated V_{SS} = -V_{CC} was included (using an external capacitor).
- There must not be any static current consumption when not stimulating.
- Current spikes during on/off time must be minimum, as well as current spikes through the switch when it is open and the tissue voltage varies.
- Safety: the failure of a single circuit element (for example a perforated MOS gate) must not produce DC current flow through the electrode larger than a few micro-amps because otherwise it may be a risk for the patient.

2.1 Circuit Design

In this section the subcircuits used in this design will be presented. The complete circuit is shown in Figure 6, with the two PMOS switching transistors in series and their driving circuitry. This two transistors allow the stimuli to pass or not into the tissue. The transistors were designed to have an impedance below 5Ω.

The circuit consists of:

i) Two Negative Level Shifters (LSN1(2)).

ii) Two Special Level Shifters (SLS1(2)).

iii) Two PMOS transistors acting as switches (M1,M2).

iv) Two Negative Drivers (NegD1(2)).

v) One Generator of V_{SS} (Gen_VSS) (uses external capacitor).

vi) Two Drivers (DRV1(2)).

vii) One Control loop (Lazo).

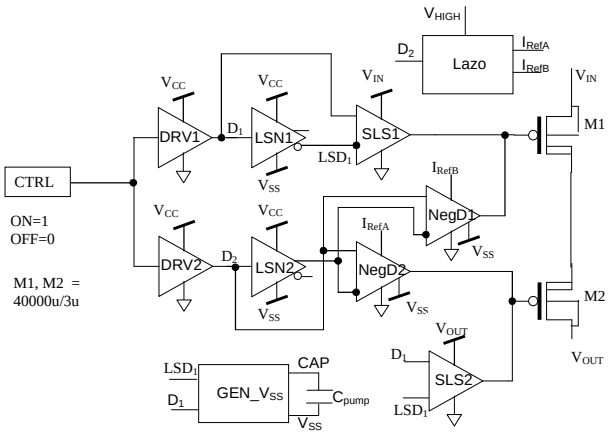
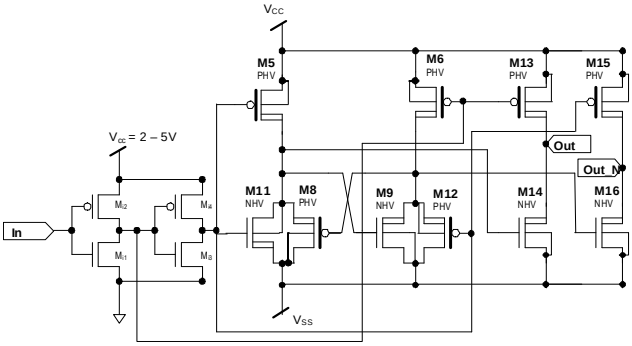


Figure 6. Complete circuit of designed switch.

In Figure 7 the LSN subcircuit is shown [1]. The LSN subcircuit receives a digital signal between 0-V_{CC} and transforms it into a V_{SS}-V_{CC} signal. This signal is needed by the SLS and NegD subcircuits. Its two states are:

- High state: When In = '1', the transistors M6, M8, M11, M13 and M16 are closed and transistors M5, M9, M12, M14, M15 are open. This ensures OUT = V_{CC} and N_OUT = V_{SS}.
- Low state: When In = '0', the transistors M5, M9, M12, M14, M15 are closed and transistors M6, M8, M11, M13 and M16 are open. This ensures OUT = V_{SS} and N_OUT = V_{CC}.



Transistor Size: HV transistors (µm)
Input inverters: M5,M6,M13,M14,M15,M16: W/L = 60/3
M_{i1-4}: W/L=20/3 M8,M9,M11,M12: W/L = 10/3

Figure 7. Negative Level Shifter schematic.

In Figure 8 the Special level shifter SLS is shown. This subcircuit connects its output, GATE, with the input, V_{IN}, when the CTRL signal is a logical 0. If CTRL is a logical 1, GATE is left in third state. Φ_{2N} is generated by the LSN used as an inverter. The SLS subcircuit is very similar to the LSN, but with a few differences:

1- All transistors connected to V_{IN} (M4x, M5x, M6/M7) are implemented with two transistors connected in series but flipped (Source connected to Source). This configuration with two diodes connected in opposite directions, prevents current circulation through those transistors in case of voltage peaks in V_{IN} (remember V_{IN} is connected to tissue and its voltage may vary).

2- The only connection to the output GATE is V_{IN} through M6/M7, which is controlled by CTRL, allowing leaving GATE to high impedance (third state) when CTRL=1.

3- As V_{IN} can vary from 16V to 100mV, M4x, M5x, M6/M7 are connected as a transmission gate, ensuring operation in all the possible ranges.

4- As M4, M5 and M7 gates are connected to V_{CC} when no stimulus is present, for safety reason this could be a problem, as if any of this transistors oxide is punctured (single failure), there will be a direct current path into the tissue. The connection of this gates through an RC circuit, limit this current to acceptable levels (two capacitors are used to withstand the HV after a failure).

The actual switch is implemented by two PMOS transistors with W=40000µm L=3µm connected in series but flipped (M1, M2 in Figure 6), to prevent conduction through Bulk-Drain diode if the switch is off and VIN > VOUT. Such large transistors were

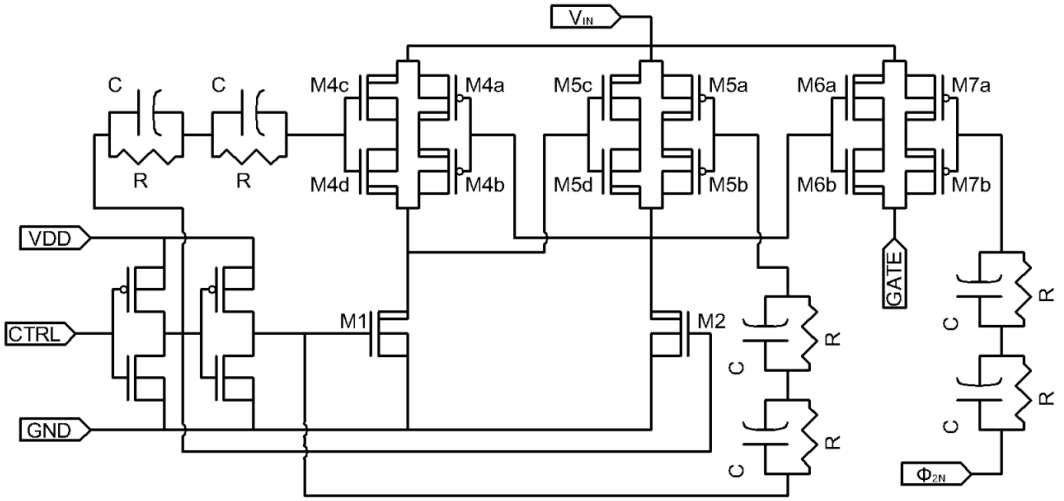


Figure 8. Special Level Shifter schematic. R=650kΩ, C=5pF.

required to maintain low impedance in all possible scenarios, even when the battery is almost discharged and V_{CC} = 2V.

Figure 9 shows the Negative Driver (NegD) subcircuit. The Negative Driver connects its output GATE to V_{SS} (depending on the control loop current I_{Ref}) when the CTRL signal is a logical 1. If the CTRL signal is a logical 0, the GATE is left in third state. CTLS is generated by the LSN and is in phase with CTRL. When IRef ≈ 0, and CTRL = '1', the transistor M2 is closed and Gate is connected to VSS through M1 and M2, but if I_{Ref} is large enough, M2 will be open and GATE will be connected to GND through M3 and the diode. The diode also ensures that when IRef ≈ 0 no conduction between GATE and GND occurs. To summarize, NegD connects GATE to a low voltage when CTRL = '1' and leaves it in third state otherwise. The low voltage is either V_{SS} if IRef ≈ 0 or GND. Note that this is a variation of the circuit proposed in Section I.A.

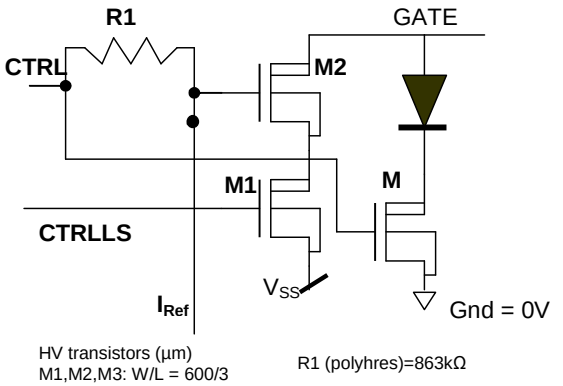


Figure 9. Negative Driver Schematic

Both the LSN and the NegD require a negative voltage (V_{SS}). This voltage is generated on-chip by the Gen_Vss subcircuit shown in Figure 10. As the V_{SS} is only needed when there is stimulation, the topology selected only generates it when CTRL= '1'. The generated voltage V_{SS} = -V_{CC}, uses an external capacitor Cpump. CTRLLS is generated by LSN using the inverted output. To explain how this subcircuit functions, its two states will be considered:

- V_{SS} = 0 state: When CLK = '0' the node CAP is connected to V_{CC} through Mi2 and the node V_{SS} is connected to GND through M1 and M2. This effectively charges the external capacitor Cpump to V_{CC}. The diode is used in the start-up of the circuit.
- V_{SS} = -V_{CC} state: When CLK = '1' the node CAP is connected to GND but the capacitor cannot discharge, so the node V_{SS} acquires a negative voltage of -V_{CC}.

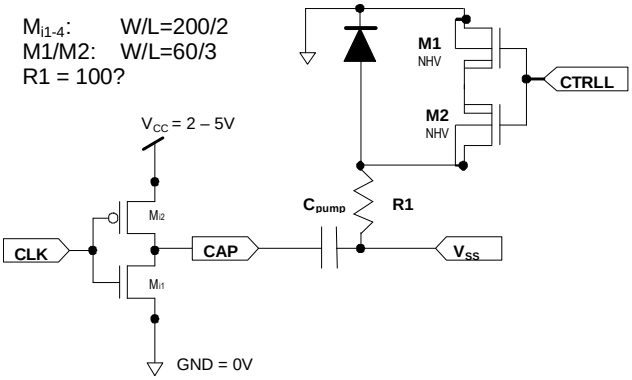


Figure 10. V_{SS} Generator Schematic

The DRV subcircuits are standard drivers containing 2 inverters.

Finally in Figure 11, the control loop (Lazo) subcircuit is presented. This subcircuit generates the current I_{Ref} for the NegD. The subcircuit copies the current through the M0 branch to the output transistors M2 and M3. If there is no stimulation, CTRL = '0' and M0 is closed so I_{Ref} = 0. When CTRL = '1', M0 is closed, but only if V_{HIGH} is high enough to overcome the V_{GS} of the 6 transistors (M_{di}) connected as diodes, does current actually flow through M0. Therefore the I_{Ref} current is only generated if CTRL = '1' and V_{HIGH} is high enough. Note that this is a variation of the control loop proposed in Section I.A, where the reference voltage is measured to fixed ground instead of V_{GATE}.

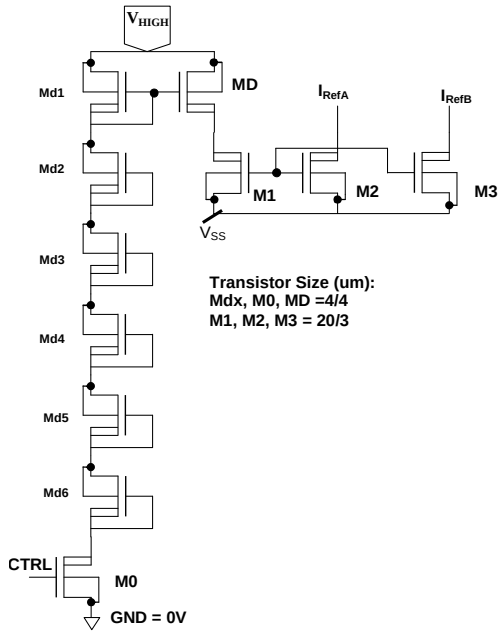


Figure 11. 'Lazo' subcircuit schematic. This is a modification of the circuit proposed in section I.A.

2.2 The Complete Switch

The topology of the complete switch is shown in Figure 6. Stimuli current conduction is done through transistors M1, M2. When the switch must be open, CTRL = '0', SLS1 connects M1's gate to V_{IN} and SLS2 M2's gate to V_{OUT}. Since V_{IN} and V_{OUT} may vary considerable only in this way we guarantee that V_{GS} = 0 and effectively open the transistors. In this case V_{SS} = GND and no static current is consumed.

When the switch must be closed, CTRL = '1', the SLS do not act (gates in third state) and both NegD connects the gates to either GND or V_{SS} to ensure the transistors are closed. The negative voltage V_{SS} is necessary as the stimulus voltage can be very small (0.1V), as in that case connecting the transistors' gate to GND does not allow current conduction through M1 and M2. On the other hand, when the stimulus voltage is very high (16V) and V_{SS} = -4V the V_{GD} ~ 20V and can puncture the oxide. To solve this problem, V_{HIGH} must be connected to the highest voltage, either V_{IN} or V_{OUT}. The subcircuit 'Lazo' was designed to generate a high enough current (I_{Ref}) to close the path to V_{SS} in NegD when V_{HIGH} > 12V. In this way the circuit is protected in extreme voltages while ensuring low impedance when the stimulus voltage is very low.

To sum up the complete switch has two states:

- Open state: When CTRL = '0', SLS1 open M1 and SLS2 open M2. V_{SS} = GND and no static current is consumed.
- Closed State: When CTRL = '1', Gen_Vss generates V_{SS} = -V_{CC}, NegD1 closes M1 and NegD2 closes M2. If V_{HIGH} > 12V, I_{Ref} closes the path to V_{SS} and M1 and M2 gates are connected to GND, otherwise they are connected to V_{SS}.

In Figure 12, a complete layout of the switch is shown.

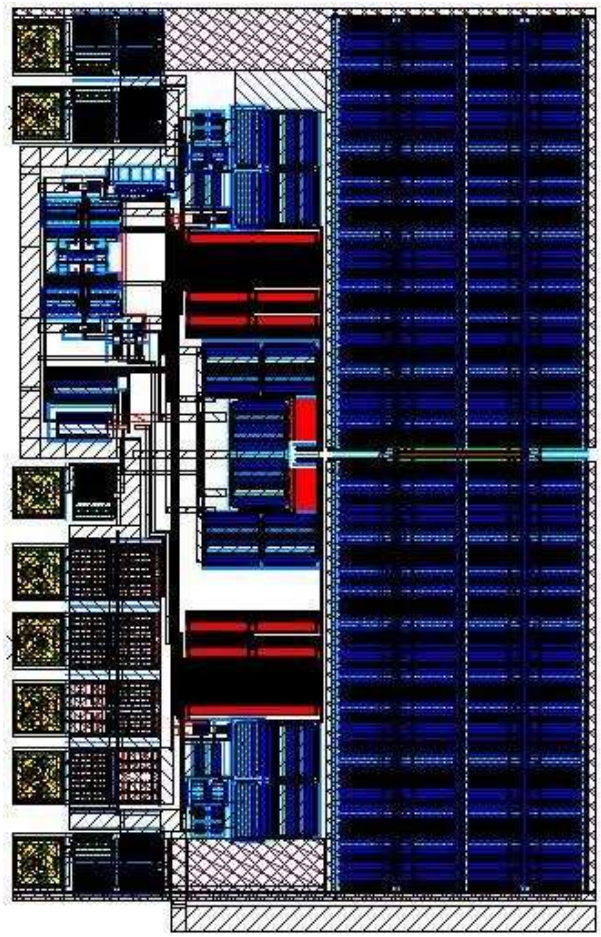


Figure 12. Final layout. PMOS switches in the right, control circuits in the middle and pads to the left. Total area < 2 mm2 (1.740 mm x 1.135mm) including PADS.

2.3 Simulations

The circuit is being fabricated. Some simulations of the switch will be presented in this section. In Figure 13 the impedance of the switch is shown (M1, M2, in Figure 6) using different transistors models: typical (TM), worst slow (WS) and worst power (WP). This simulation was conducted with V_{CC} = 2V (which is the worst possible case). Figure 13 shows that in all three cases the impedance of the switch is always below 5 Ω (careful design of the metal cables connecting the transistors to the pads was necessary to fulfil this condition).

In Figure 14, a second simulation is presented: V_{OUT} of Figure 5 is shown for the two most extreme cases of V_{IN}, with a load impedance of 1kΩ. The switch works in all the necessary voltage ranges, for all transistors models.

Finally in Figure 15, the current through the switch is plotted, when V_{IN} is connected to ground and a square wave of 8V of amplitude was applied to V_{OUT}. Only parasitic current spikes can be observed, caused by the charge change in the gate-drain capacitance of M2, but no DC current circulates between the tissues. In table 1, the simulated characteristic of the complete switch are summarized.

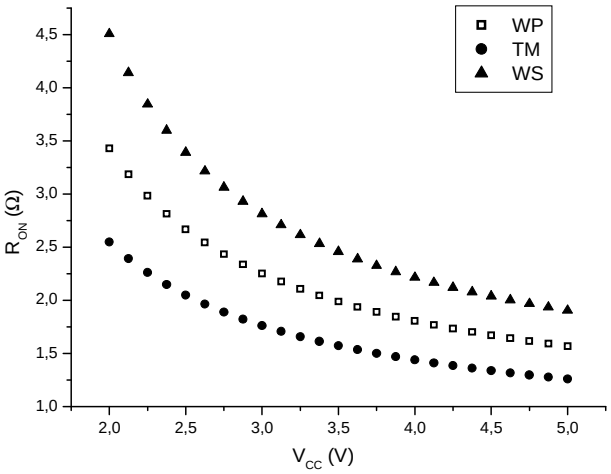


Figure 13. Switch Impedance as a function of V_{CC}. Impedance is bellow 5Ω even for the worst case.

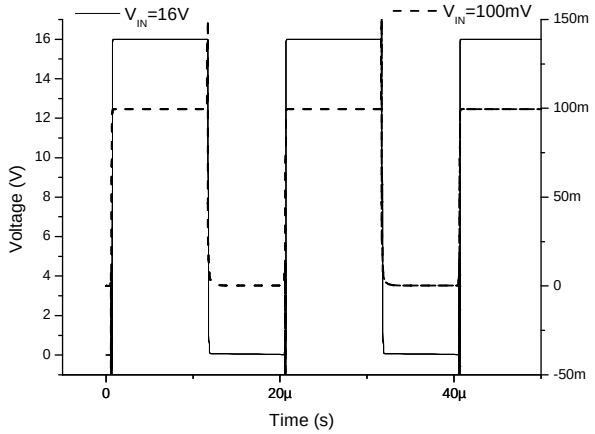


Figure 14. V_{OUT} voltage with V_{IN}=16V and V_{IN}=0.1V. Simulation configuration as shown in Figure 5.

Table 1. Switch Simulated Characteristics

Characteristics	Value
Switch Impedance (Typical)	3 Ω
Power supply (V_{CC})	2-5 V
Commutation voltage (V_{IN}/V_{OUT})	0.1-16 V
Commutation time	0.5 μs

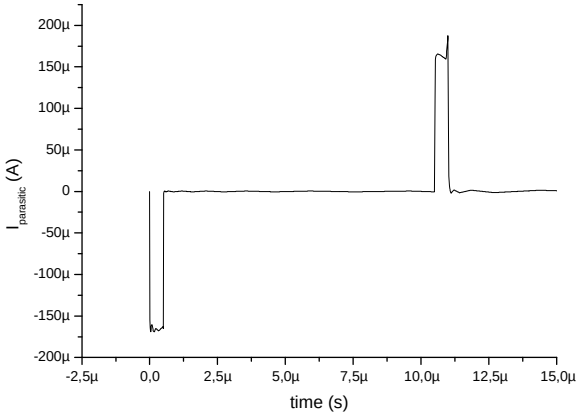


Figure 15. Only parasitic current spikes are observed when the switch is off. Parasitic spikes correspond to the charging of the gate capacities of the transistor.

3. CONCLUSIONS

A self biased overvoltage protection circuit technique was presented that allows driving MOS transistor in their full VDS range above V_{GS} voltage limits. The complete design of an integrated switch, to precisely control electrical stimulation in implantable medical devices (currently under fabrication) using this technique was presented. The simulations of the designed switch fulfil all specifications and safety requirements, a complete testing will be realized when the fabrication is complete.

4. ACKNOWLEDGMENTS

The authors would like to thank CCC del Uruguay, for the support to this research, and Eng. Pedro Arzuaga, and Federico de Mula for helpful suggestions.

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