On the design of ultra low noise amplifiers for ENG recording.

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ABSTRACT
Due to the extremely low amplitude of the input signals, the design of electro-neurgo-graph (ENG) amplifiers normally involves special care for flicker and thermal noise reduction. The task becomes really challenging in the case of implantable devices, because power consumption is restricted to few tens μW. In this paper, two different circuit techniques aimed to reduce flicker and thermal noise, in ultra-low noise amplifiers for implantable electronics are demonstrated. In both cases circuit design and measurement results are presented, showing an excellent performance in circuit simplicity, and noise to power consumption trade-off. The first circuit is a very simple G_m-C chopper low-pass amplifier for flicker noise cancellation. It consumes only 28mW, with a measured input referred noise and offset of 1.2 $nV/\sqrt{Hz}$, and 2.5μV, respectively. For the reduction of thermal noise with minimum power consumption, in the second circuit, a ultra-low noise amplifier, a energy-efficient DC-DC downconverter, and low voltage design techniques are combined. Measured input referred noise in this case was 5,5 $nV/\sqrt{Hz}$ at only 380μW power consumption. Both circuits were fabricated in a 1,5 micron technology.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Style – *Input/output circuits, VLSI.*

General Terms
Design.

Keywords
Analog design, CMOS, low-power, low-noise.

1. INTRODUCTION
Most implantable neuroprostheses are stimulators of the nervous system. The main improvement that, in both the industry and research laboratories is nowadays being investigated, is to enable neural signals (electro-neuro-graph or ENG) to be used as inputs in the control feedback of neuroprosthetic systems [1]. ENG signals are registered from electrodes placed around nerves and may be used instead of a wide variety of artificial sensors in implants. Microelectronics technology is steadily contributing to develop this group of medical devices, and in recent years there has been a considerable research effort in the development of integrated amplifiers for ENG [1-4]. The main challenges are: the extremely low noise required for amplifying μV range signals, and the ultra-low power consumption specified for implantable electronics since they are normally battery powered. Power consumption is the main restriction for the development of such amplifiers. On the other hand, circuits must be extremely reliable because they may be life supporting devices for the patient. ENG signals range from a few Hz to a few kHz; an amplifier requires an input referred noise of a few $nV/\sqrt{Hz}$, a high gain, and a high CMRR [1,4]. In this paper the focus will be on noise.

The main sources of electrical noise in the frequency span of biological signals –apart from coupling noise- are thermal and flicker noise of the circuit elements at the input stage. For a MOS transistor, thermal noise current model is in general not questioned its PSD being (the PSD of the noise current in parallel with the transistor) [5]:

$$S_{i\_th}(f) = \gamma k_B T g_m \quad (1)$$

Where k_B is the Boltzmann's constant, T the absolute temperature, g_m is the transistor's transconductance, $n \approx 1$ is the slope factor, γ = 2, or 8/3 in strong an weak inversion respectively [5]. Although some existing flicker noise models may cause misleading results, as pointed in [5] the application of the empirical model for flicker noise:

$$S_{i\_1/f}(f) = \frac{q^2 N_{ot} g_m^2}{WLC_{ox}'^2} \cdot \frac{1}{f} \quad (2)$$

is an accurate approximation of a physical noise model in all the operation regions of the transistor. q is the charge of the electron, W, L, C_{ox}' are the transistor width, length, and oxide capacitance per unit area respectively. N_{ot} is the effective number of traps, a technology parameter to adjust. Integrating (1), (2) in the frequency band of interest in a continuous time amplifier, input

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Table I: Reported results of ENG amplifiers.

	Filter Band	Supply Voltage	Area	Noise	Power	Type	Technology	ζ [nV.Hz$^{-1/2}$.mW$^{1/2}$]
Sacristan et al [4]	100-5KHz	5 V	1.1 mm^2	5.1 nVHz$^{-1/2}$	1 mW	Non-chopped	0.7 µm	5.1
Uranga et al [3]	DC-3K	5 V	2.7 mm^2	6.6 nVHz$^{-1/2}$	1.3 mW	Chopper	0.7 µm	7.52
Gosselin et al [2]	100-5KHz	1.8 V	---	30 nVHz$^{-1/2}$	25 µW	Chopper	0.18 µm	4.74

referred noise result a combination of power consumption and area constrains [5]:

$$v_{n\,rms} \approx \underbrace{\frac{A}{g_m}}_{\text{Thermal noise}} + \underbrace{\frac{B}{W.L}}_{\text{Flicker noise}} = \frac{A}{g_m/I_D}\cdot I_D + \frac{B}{W.L} \qquad (3)$$

In (3), $v_{n\,rms}$ is the input referred rms noise voltage, g_m is transconductance of the input pair. A, B, are constants depending on frequency band, technology parameters, and the number of transistors introducing noise at the input branch. As pointed in [4,5] low input noise requires: a large bias current for a large g_m to reduce thermal noise; and a large W,L for flicker noise reduction. Multiplying and dividing by the drain current I_D the first term, it is simple to conclude that to minimize thermal noise with a fixed current budget, input transistors should be biased in weak inversion (WI) to maximize the ratio g_m/I_D. At WI $g_m/I_D \approx 25$; further noise reduction necessarily require for the designer an increase of the bias current and thus power consumption. To reduce flicker noise, as huge as possible transistors can be utilized at the input. A more elegant solution, is the use of known circuit techniques like autozero or chopping [6] that also contribute to offset cancellation. Chopper amplifier has been extensively used in ENG recording, and is suitable to preserve a reduced area for example in the case of multi-channel nerve signal recording [2]. However, a complex chopper topology increases also area, and power consumption. For example, band-pass filter tuning [6] adds an extra circuit demanding a considerable silicon area. Most reported complex chopper topologies, aim to reducing residual offset. On the other hand, for ENG applications offset cancellation is a byproduct of flicker noise reduction techniques. Thus simpler architectures are the better option, suitable to remove flicker noise, but simple enough to achieve the lowest possible power and die area budget.

This paper presents some guidelines for the design process, and measurement results on fabricated ENG oriented circuits, for the reduction of flicker and thermal noise with minimum power consumption. Firstly, a very simple chopper circuit is shown. The topology has been previously proposed in [7], in this work a circuit design for ENG specifications is presented as well as measurement results are shown. Less than 2nV/√Hz input referred noise, and only 2.5µV input offset were measured while the circuit contains only 15 transistors including chopper modulators.

In section 3, thermal noise is addressed, and a technique for thermal noise reduction is proposed. The idea is simple: as depicted in eq.(3) thermal noise is inversely proportional to bias current, not to power consumption. Lowering the supply voltage with a energy-efficient DC-DC converter and using low voltage circuit techniques, bias current can be increased without an increase in power consumption. A circuit with the same specifications of [4] is presented in section 3, but dividing the supply voltage by 3 with an 80% efficient DC-DC, power consumption is reduced to approximately 1/3rd without a significant loose in performance. The circuit consumes only 380µW power with a measured input referred noise of $0{,}5\mu V_{rms}$ in the band of interest, from 0.1 to 5kHz.

1.1 A figure of merit

A careful chopper design makes possible to push most flicker noise energy out of the band of interest. Regarding thermal noise, it appears useful to define a figure of merit that allows comparing two different low noise amplifier realizations. It should be noted that if all the transistors in two low noise circuits of similar topology, are assumed to operate in the same inversion level (ideally WI), and the circuits have the same supply voltage, the input referred noise voltage is related to power consumption in both circuits (1),(3):

$$\frac{v_{n1}(f)}{v_{n2}(f)} = \sqrt{\frac{P_2}{P_1}} \qquad (4)$$

Where $v_{nx}(f) = \sqrt{PSD}$ [nV/$\sqrt{\text{Hz}}$] is the noise voltage ($v_n(f) = v_n$ in the case of thermal noise) and P_x is the power consumption of each circuit. Equation (4) shows that to reduce the noise voltage by 5, power consumption has to be increased by 25, and so on. Observing (4), it is possible to define the following figure of merit:

$$\zeta = v_n \cdot \sqrt{P} \qquad (5)$$

A lower ζ indicates a more efficient low-noise circuit for the task of amplifying signals at the minimum power consumption. For example, compare the circuits listed in table I corresponding to several reported ENG amplifiers. Note that although the circuits show rather different figures of power consumption and input noise, their efficiency in the sense of (5) is very similar in the three cases.

2. A CHOPPER AMPLIFIER FOR ENG FLICKER NOISE AND OFFSET REDUCTION.

The proposed chopper amplifier is shown in Fig.1. The input signal v_{in} is chopped at a frequency f_{ch} - period $T_{ch} = f_{ch}^{-1}$ - and then amplified on each phase through two independent G_m-C low pass filters. The intermediate signals v_{out1}, v_{out2} are further amplified by means of a low-pass filter (LPF) to remove residual frequency components above the band of interest. v_{Out} is the output signal. The square wave $m(t)$ switches the modulators. v_n represents a parasitic voltage source like for example input noise or offset. The circuit is extremely simple: just two transconductors, two capacitors, and an output low pass filter. Even G_{m2} can be substituted by an integrated resistor, and the output low-pass is not essential (it was placed just to provide a 'clean' output signal).

Because the input signal v_{in} is chopped, both branches are amplifying roughly the same signal, but with opposite sign. Their output is then subtracted, the result being $v_{out}(f) = H(f)v_{in}(f)$. On the other hand, noise and offset voltage at the input v_n are amplified with equal sign and then subtracted. To guarantee a proper noise cancellation, the hypothesis is that the signal v_n does not change too much from one phase to another of the chopper. This is true for offset, and flicker noise (if $f_{ch} >> f$) but unfortunately not in the case of thermal noise [7]. The factor 2 of the capacitor in (6) is the result of switching the transconductances at a 50% duty cycle [7].

$$H(\omega) = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{[1 + j\omega 2C/G_{m2}]} \qquad (6)$$

The circuit was designed to amplify ENG signals with amplitudes greater than 1μVp in the band from 100 to 5KHz, with noise initially specified as less than 5 $\text{nV}/\sqrt{\text{Hz}}$. The gain of this first stage must be at least 50, while further amplification can be obtained in successive stages. Additionally, a high CMRR (~90dB) is expected. As pointed in section 1, the best option is to operate in weak inversion. Unfortunately unless very low currents are used, this results in a high *W*/*L* ratio increasing the transistor area. In our case a maximum value of *W*/*L* = 100 was selected to prioritize a reduced area. L was chosen as the minimum allowed.

G_{m1} was implemented as a standard symmetrical OTA using 8 transistors, with a total occupied area of less than 0.04 mm^2, including the switching transistors for signal commutation. A 3.4mA bias current was selected, large enough to guarantee a reduced thermal noise according to (3). G_{m2} was substituted by an integrated poly resistance of 62KΩ. The output capacitors were calculated to set the low-pass filter pole at 5kHz. The two 300pF double poly capacitors were integrated in the chip, increasing the total area to 1 mm^2.

The nominal chopper frequency is 20 KHz. The nominal gain is 70, and input signals of up to 1mV were measured. The circuit was fabricated in a 1.5μm technology. In Fig.2 the measured gain vs. frequency of the amplifier is presented, and in table II measured results are shown.

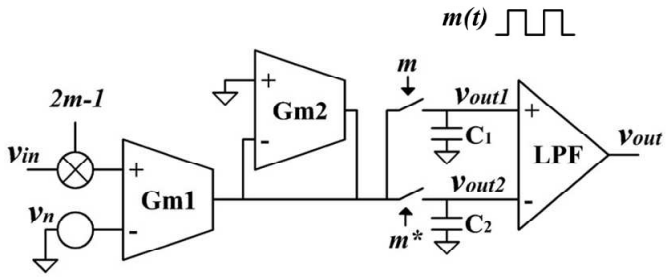

Figure 1: Topology of the proposed G_m-C amplifier. *m(t)* is the clock signal and *m is the complementary clock.**

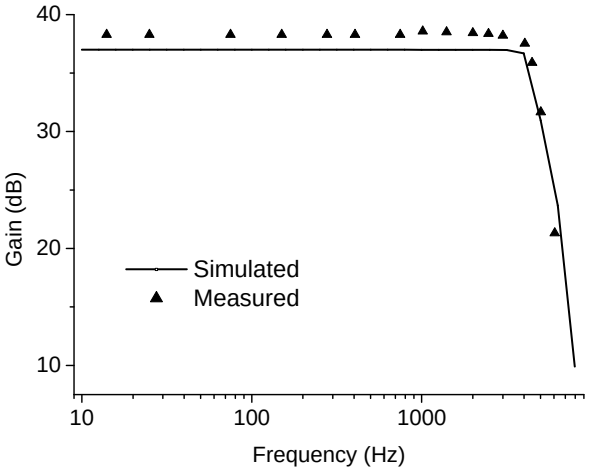

Figure 2: Measured and simulated Gain vs frequency.

Table II: Measured and simulated results

	Simulated	Measured
Gain	70	80
Bandwidth	5 kHz	5 kHz
CMRR	(*)	88 dB
V. noise	4 $nV/Hz^{1/2}$	1,2 $nV/Hz^{1/2}$
Consumption	28 mW	
Supply	5 V	
Area	1,0 mm^2	
Offset	(*)	2.5 μV
Active area	0,04 mm2	

(*) In a chopper, residual offset as well as CMRR, involve several complex phenomena (coupling, etc.) that are difficult to simulate.

2.1 Considerations about the results

Although the power consumption of the amplifier is still high (28 mW), both supply voltage and bias current can be reduced without increasing noise, by increasing *W/L* ratio of the transistors pushing them closer to weak inversion. Since most of the area of our circuit is used by the integrated capacitors (more than 90 %), increasing the area of the transistors will result in a slightly increase of the total area.

Using the figure of merit in (5), for this amplifier ζ = 5.8 $\mathrm{nV}\cdot\sqrt{\mathrm{mW}}/\sqrt{\mathrm{Hz}}$ close to the reported values in table I.

2.2 Circuit Layout

The G_m-C chopper amplifier as well as the one in Section 3, were designed and fabricated in a 1.5µm technology. In Fig.3 the layout of the both amplifiers is presented.

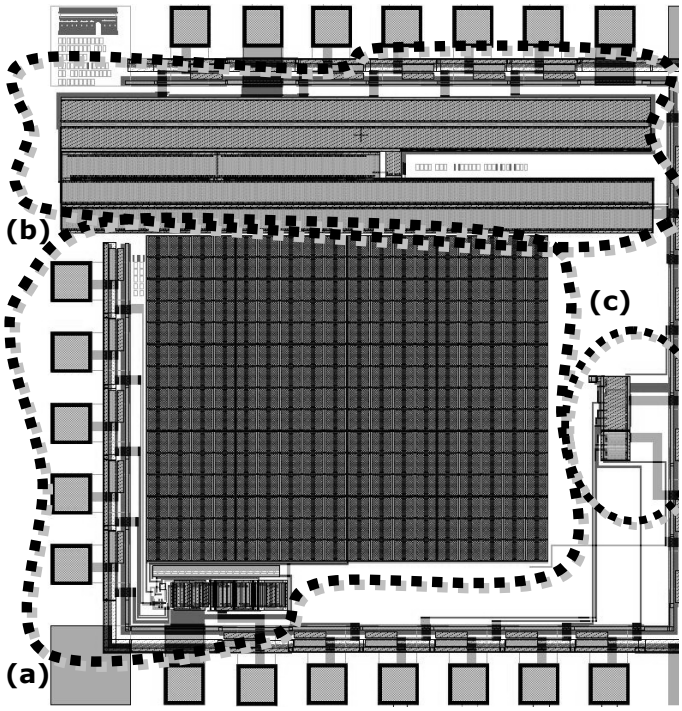

Figure 3: Layout of fabricated circuits. (a) G_mC Chopper amplifier of section 2, including integrated capacitors. (b) Low noise preamplifier of section 3 is used in conjunction with (c) a charge pump DC-DC converter, using external capacitors.

3. THERMAL NOISE REDUCTION

Thermal noise is inversely proportional to bias current (2), thus by reducing the supply voltage by means of a DC-DC converter (efficiency close to 100%), it is possible to keep the same bias current of an amplifier (and thus thermal noise) but reducing the power consumption of the battery (see Fig.4(a)). To demonstrate the technique, in this work a low-noise amplifier with the same topology of the one in [4] is presented, but supply voltage is reduced by a factor of 3 (to only 1.8V). The DC-DC converter is shown in Fig.4(b), it is a charge-pump downcoverter, with 3 external C_{fly} capacitors that are periodically charged in series, and then transfer charge in parallel to a storage capacitor C_{sto}. The preamplifier is shown in Fig.4(c), and transistor sizes were optimized to operate at low voltage in the same 1.5µ technology. The input transistors operate in WI to reduce saturation voltage and thermal noise, and also have a large area to reduce flicker noise and offset. The transfer function of the circuit in Fig.4(c) is:

$$H(f) = \frac{Rg_{mpd}\cdot j2\pi f}{j2\pi f + \frac{ng_{mpd}}{2C}} \qquad (7)$$

where g_{mpd} = 2,2x10^{-3}S is the differential pair M_{pd} transconductance, R=50kΩ and C=2,2µF. Theoretical gain is G_{DC}=110 with low-pass cut-off frequency at f_c=100Hz.

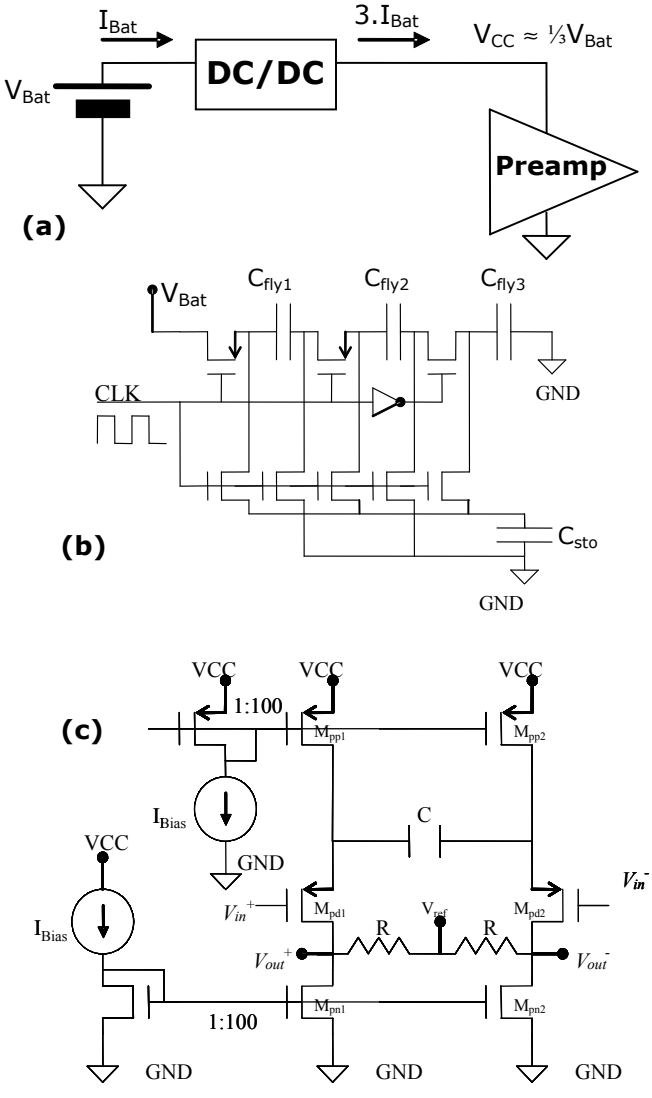

Figure 4: a) Block diagram of the amplifier of section 3. b) DC-DC converter, V_{BAT}=5,4V, V_{out}=1,8V, C_{fly*}=100nF, C_{sto}=10µF and f_{CLK}=30kHz. c) Preamplifier. I_{Bias}=1µA.

For transistor sizing, first it is necessary to examine the noise contribution at the input, of each pair of transistors in Fig.4(c), the result being:

$$Sv_{ind}(f) = \frac{2S_{ipd}(f)}{g_m{}^2}$$

$$Sv_{inp}(f) = Sv_{ind}(f)\frac{g_{ms}{}^2}{(g_{ms}{}^2 + 16\pi^2 C^2 f^2)} \qquad (8)$$

$$Sv_{inn}(f) = Sv_{ind}(f)\frac{g_m{}^2 R^2}{|H(f)|^2}$$

To deduce (8) all of M_{pd}, M_{pp}, M_{pn}, in Fig.4(c) are supposed to be equal in size, and as depicted in Fig.4(c) all have the same bias current. $Sv_{ind}(f), Sv_{inp}(f), Sv_{inn}(f)$, are the input referred noise voltage caused by the noise introduced in the circuit respectively by the differential pair M_{pd}, PMOS mirror M_{pp}, and NMOS mirror M_{pn}. g_m, g_{ms} are the gate, and source transconductance of the differential pair respectively. $S_{ipd}(f)$ is the noise current of M_{pd} (can be calculated using (1),(2)). Integrating (8) in frequency one arrives to the conclusion that the noise contribution of the NMOS current source and the differential pair is nearly the same, but the noise introduced by the PMOS current has little impact on total input noise. So to fix transistor size, the PMOS noise contribution is neglected. Then, the differential pair, and NMOS mirror will be of the same size, *L* is selected as three times the minimum channel length, and *W* is chosen enough large to guarantee that flicker and thermal noise are the same in the band of interest. According to an existing current budget I_{Bias} (Fig.4(c)) is 1μA so the bias current of each transistor is 100μA. In table III, a summary of each transistor size is shown.

Table III. Transistor size (W,L in microns), NMOS current source, PMOS current source, differential pair.

NMOS CS	PMOS CS	D.Pair
W=14826 L=4,5	W=3760 L=4,5	W=14826 L=4,5

3.1 Considerations about the results

In Fig.5 the simulated and measured transfer function of the preamplifier is shown. The measured DC gain is much less than expected in (7) because the channel resistance r_{ds} of the NMOS current source is close to *R* value. Some of the signal current flows through the NMOS instead of *R*, lowering the gain form 100 to 60 approximately. A list of measured and simulated characteristics is presented in table IV. The results show a input noise similar to the amplifier in [4]. It is still necessary to investigate the origin of the still poor measured CMRR.

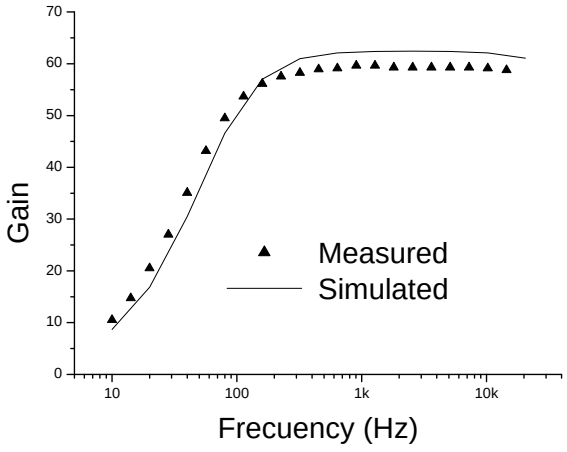

Figure 5: Preamplifier transfer function, simulated (line) and measured (triangles)

Using ζ as defined in (5), the amplifier here presented has an figure of merit $\zeta = 2.1\ \text{nV}\cdot\sqrt{\text{mW}}/\sqrt{\text{Hz}}$ (preamplifier is connected to the DC-DC converter). Comparing to table I, the figure of merit of [4] has been improved by a factor 2,4 , just by using the voltage reduction technique in a 1.5μ technology.

Table IV: Simulated and measured results.
(*) DC-DC converter included

	Simulated	Measured
Cut-off frequency	82 Hz	60 Hz
Preamplifier Gain	62	60
CMRR	-----	58 dB
Input noise (100-5kHz)	$0.5\mu V_{rms}$	$0.54\mu V_{rms}$
Power consumption (*)	-----	380μW
DC-DC output	1.76 V	1.72 V
Efficiency DC-DC	85 %	80 %

4. CONCLUSIONS

Two circuit techniques were investigated, for the design of ultra-low noise amplifiers for ENG recording in implantable applications. First a very simple G_m-C chopper amplifier was successfully employed to eliminate flicker noise, measurement results include only 2.5μV input offset, only $1.2\ \text{nV}/\sqrt{\text{Hz}}$ input noise, a high CMRR, all at 28mW power consumption. For thermal noise reduction, an integrated preamplifier was successfully tested with low power supply (1,8V), and using a efficient DC-DC converter to generate the supply voltage. Measurement results include only $5.5\ \text{nV}/\sqrt{\text{Hz}}$ input noise, at

only 380μW power consumption, a result almost 2 ½ times more efficient than other reported amplifiers for the same purpose.

5. ACKNOWLEDGEMENT

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