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## **MOSI Integrated Circuit Report.**

### **Project Number: 77217**

This report correspond to the Project number 77217, fabricated under de MOSIS MEP instructional account of Universidad Católica del Uruguay, Departamento de Ingeniería Eléctrica. The circuit was fabricated in AMIS ABN 1.5micron technology; it has a total area of 2.2mm x 2.2mm.

The circuits are the result of advanced undergraduate student work, as part of the course "Microelectronics". This course pretend to be a first glance to undergraduate students, on modern microelectronic technology, and ASIC design process. First the students review the different design tools for analog microelectronics, that are then applied on a full-custom design. The main software tool is University version of Mentor, licensed trough Mentor Higher Educational Program. Some students are also working with Electric (free design suite).

In the following report, a brief description of the circuits inside the chip is presented, as well as measurement results. A general conclusion is that all the circuits are operative, working close to expected performance. For any extra information please contact:

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Finally, the students and staff at Universidad Católica would like to acknowledge MOSIS for its support in IC fabrication. Without the help from MOSIS, it couldn't have been possible for students to turn into practice, the theory and tools them acquired during the Microelectronics course.

## **1 - Overall chip description**

The fabricated chip contains 2 different analog circuit designs.

- 1- 100Hz-5kHz Band-Pass  $G_m$ -C filter
- 2- Mismatch test structures

Circuit 1 correspond to a band-pass filter aimed to be included in ENG (Electro-Neuro-Graph) signal registration in implantable medical devices [1]. Main characteristics are 100Hz-5kHz passband, ultra low-power consumption, low noise, high CMRR, among others. This circuit uses continuous time  $G_m$ -C technique.

Circuit 2, are a set of non-unitary current mirrors with a copy factor 1:64, to allow students practice layout matching techniques, and high-precision measurement techniques. Measurements are similar to those presented in [2], where current copy error is measured for several decades of the current value.

A description of each circuit and measurement results is presented below.

## 2. Continuous time G<sub>m</sub>-C band-pass filter for ENG signals

This circuit, a band-pass filter (BPF) using G<sub>m</sub>-C technique shown in Fig1, is used to eliminate noise out of the band of interest in ENG signal recording in an implantable medical devices [1]. The OTA's are symmetrical ones, while G<sub>m2,3</sub> use series-parallel current division at the output to achieve such low transconductances [2]. This BPF has a gain  $G_{BP} = 33$  and cut-off frequencies at 100Hz and 5KHz. OTAs and capacitor values were selected:  $G_{m1}=20\mu\text{S}$ ,  $G_{m2}=682,8\text{nS}$ ,  $G_{m3}=2,2\text{nS}$ ,  $C_1=78\text{pF}$  and  $C_2=22\text{pF}$ .

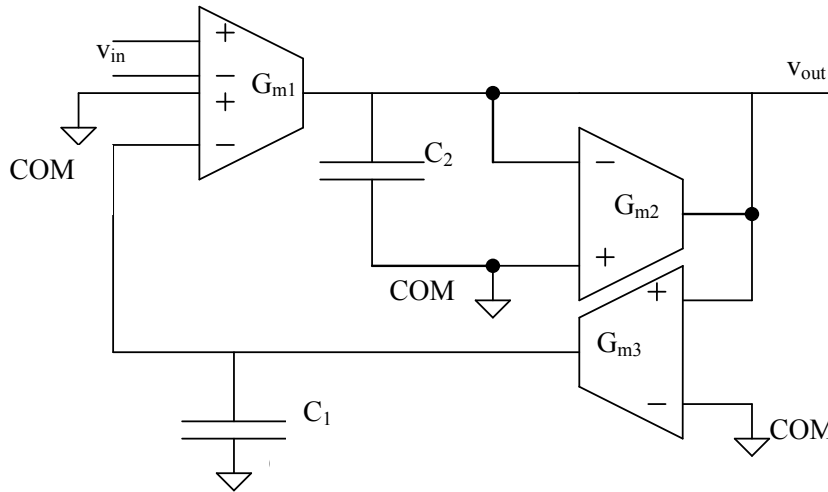


Figure 1) G<sub>m</sub>-C band pass filter ,  $G_{BP}=33$ ,  $G_{m1}=20\mu\text{S}$ ,  $G_{m2}=682,8\text{nS}$ ,  $G_{m3}=2,2\text{nS}$ ,  $C_1=78\text{pF}$  and  $C_2=22\text{pF}$ .

Measurement Results:

Fig.2 shows the measured transfer function of the G<sub>m</sub>-C filter. An overall conclusion is that the circuit worked as expected. Current consumption was measured in  $20\mu\text{A}$ . Power supply is 5V, and input noise is  $33\mu\text{V}_{rms}$ .

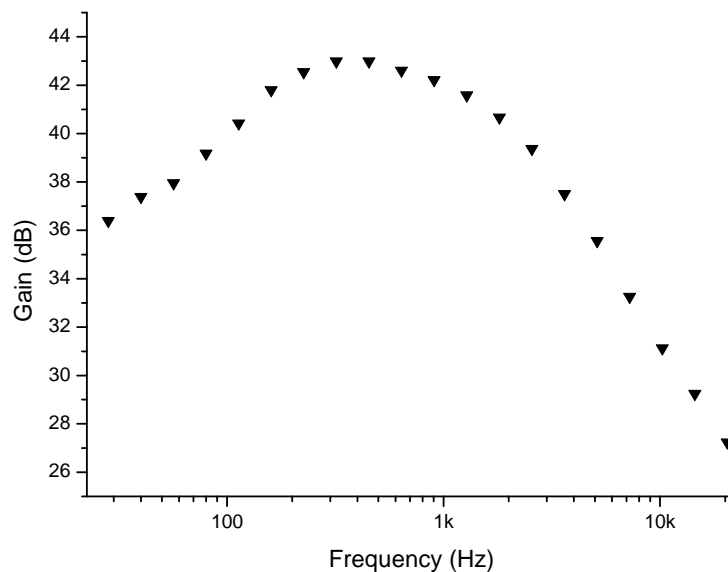


Figure 2) Measured transfer function.

Conclusions: The filter worked as expected.

### 3. Mismatch characterization of transistors according to transistor geometry.

The benefits of series-parallel association of transistors regarding mismatch, show some interesting results [2], particularly to design very low transconductance OTA's. Non-unitary current mirrors, were fabricated to complete the study of the previous circuit, as well as to practice matching layout techniques, and low current measurements in the laboratory.

Six different 1:64 current copiers were fabricated; in matched ones the matching rules described in [2] are followed while non-matched ones are just transistors of different aspect ratio. The detail of the fabricated mirrors are as follows:

- E1 matched mirror M1 = 8x8 unitary transistor array, M2 = 64 parallel unitary transistors.
- E2 matched mirror M1 = single unitary transistor, M2 = 64 parallel unitary transistors.
- E3 matched mirror M1 = 3x24 unitary transistor array, M2 = 24\*3 parallel unitary transistors.
- E4 non-matched mirror M1 = single transistor, M2 = 64 times wider.
- E5 non-matched mirror M1 = wide and large transistor W/L=1, M2 = single W/L = 64 transistor.
- E6 non-matched mirror M1 = single W/L = 3/24 transistor, M2 = single W/L = 24/3 transistor.

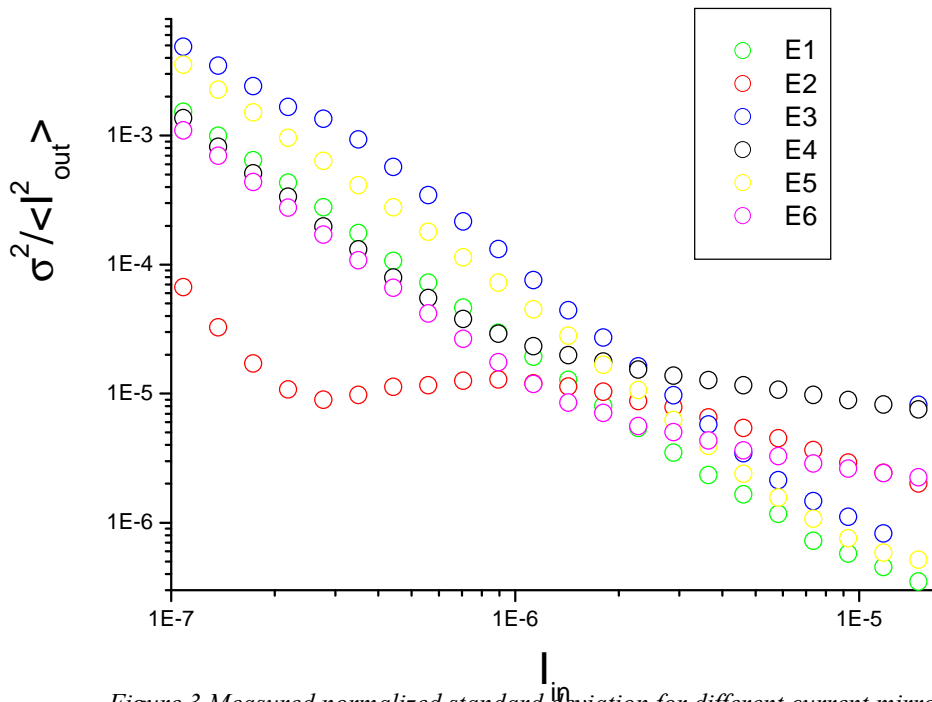


Figure 3 Measured normalized standard deviation for different current mirrors.

The input and output currents were generated and measured measured respectively, using an HP4155 Semiconductor Parameter Analyzer. The standard deviation was calculated with the 5 circuit samples from MOSIS. The results are plotted in Fig.3 as in [2], for a input current ranging several decades.

### Conclusion:

The current mirrors worked as expected, with a copy factor close to 64 in all cases. As expected also, the curves in Fig.3 decay from weak to strong inversion. However, no significant difference is observed between the curves as predicted in [2]. There are several reasons that may explain this observation: first of all only 5 samples were used to calculate a standard deviation; also since the mirror is a current multiplier, the effect of output conductance mismatch may hide threshold voltage fluctuation effect. Finally it should be pointed, that leakages in the current mirrors much higher than expected (up to hundreds nA) were observed. Probably the origin of leakages is the use of protected PADs.

### References:

- [1] J.Sacristan, M.T.Oses, "Low noise amplifier for recording ENG signals in implantable systems", *IEEE ISCAS'2004*, vol.IV, pp.33-36, May-2004.
- [2] "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors" Alfredo Arnaud, Rafaella Fiorelli, Carlos Galup-Montoro, *IEEE Journal of Solid State Circuits*, Vol. 41, n°9, pp.2009 – 2018, Sept. 2006.