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MOSI Integrated Circuit Report.

Project Number: 76065

This report correspond to the Project number 76065, fabricated under de MOSIS MEP instructional account of Universidad Católica del Uruguay, Departamento de Ingeniería Eléctrica. The circuit was fabricated in AMIS ABN 1.5micron technology; it has a total area of 2.2mm x 2.2mm.

The circuits are the result of advanced undergraduate student work, as part of the course "Microelectronics". This course pretend to be a first glance to undergraduate students, on modern microelectronic technology, and ASIC design process. First the students review the different design tools for analog microelectronics, that are then applied on a full-custom design. The main software tool is University version of Mentor, licensed trough Mentor Higher Educational Program. Some students are also working with Electric (free design suite).

In the following report, a brief description of the circuits inside the chip is presented, as well as measurement results. A general conclusion is that all the circuits are operative, working close to expected performance. For any extra information please contact:

Dr. Alfredo Arnaud
Universidad Católica del Uruguay
Av.8 de Octubre 2738/DIE, Montevideo – Uruguay. CP:11800
Tel: (5982) 4872717 ext.407
Email: aarnaud@ucu.edu.uy

Finally, the students and staff at Universidad Católica would like to acknowledge MOSIS for its support in IC fabrication. Without the help from MOSIS, it couldn't have been possible for students to turn into practice, the theory and tools them acquired during the Microelectronics course.

1 - Overall circuit description

The fabricated chip contained 3 different analog circuit designs.

- 1- Pre-amplifier for ENG signals
- 2- DC-DC power supply
- 3- Chopper pre-amplifier for ENG signals

Circuits 1 and 3 correspond to preamplifiers for very low amplitude signals, like those of ENG (Electro-Neuro-Graph) signal registration [1,2,3]. Main characteristics are ultra low-noise, low power consumption since the circuits are intended to operate in implantable medical devices, high CMRR, among others. Circuit -1- uses continuous time techniques, while circuit -3- uses chopper modulation for flicker noise removal. Noise reduction is made in circuit -1- by lowering the voltage from the hypothetical battery, by means of a energy efficient DC-DC converter. The latter is the circuit -2-.

A description of each circuit and measurement results is presented below.

2. Continuous time preamplifier for ENG signals

This circuit is a ENG amplifier following the topology presented in [1]. The designed circuit is the one shown in figure 1. Specifications include: supply voltage = 1.8V, gain >50 for the preamplifier, noise < .25 μ V_{rms} at the input in the band from 100 to 5kHz, the preamplifier must be high-pass. Noise analysis and low noise design, followed the guidelines in [4].

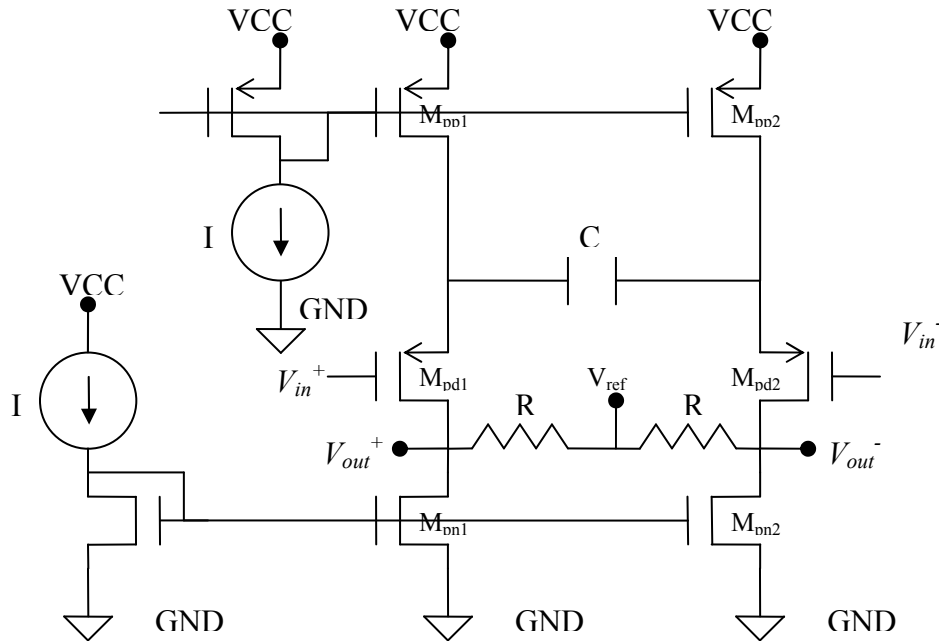


Figure 1. Pre-amplifier schematics

The transfer function of the circuit is as follows:

$$H_{preamp}(s) = \frac{Rg_{mpd}s}{s + \frac{ng_{mpd}}{2C}} \quad (1)$$

g_{mpd} , n is the slope factor slightly depending on the gate voltage [5], is the gate transconductance of the differential input pair. The gain G_{DC} can be calculated:

$$\left. \begin{array}{l} G_{DC} = g_{mpd}R \\ g_{mpd} = 2,2 \times 10^{-3} \\ R = 50k\Omega \end{array} \right\} \Rightarrow G_{DC} = 110 \text{ but the simulated } G_{DCsim} \cong 60, \text{ the error on}$$

the estimated gain is due to the output transconductance of Mpn1 that is 100k, close to the value of R.

Figure 3 shows the measured transfer function of the pre-amplifier, the measured gain is $G_{DC} \cong 59,64$. With a C of 2,5uF the expected position of the pole is 91 Hz. The measured was $f=54Hz$. The expected CMRR was 90dB, the measured one was only 60dB.

Conclusions: The preamplifier worked as expected, the CMRR has to be improved.

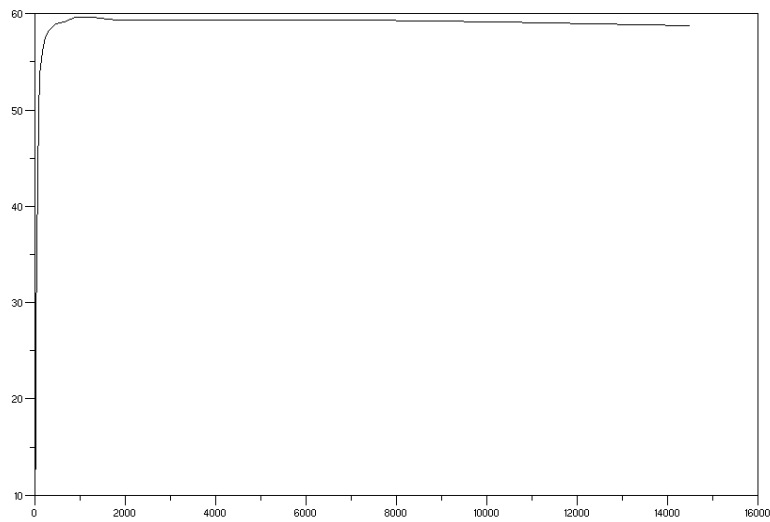


Figure 3 Measured TF of the pre-amplifier

3. DC-DC power supply

The DC-DC power supply was designed to convert a 5V power supply into 1.8V, with a high energy efficiency at the nominal current consumption of 200μA. The designed circuit is the one shown in figure 4, were several MOSFET switches connect/disconnect three capacitors to divide the original voltage by 3 [6].

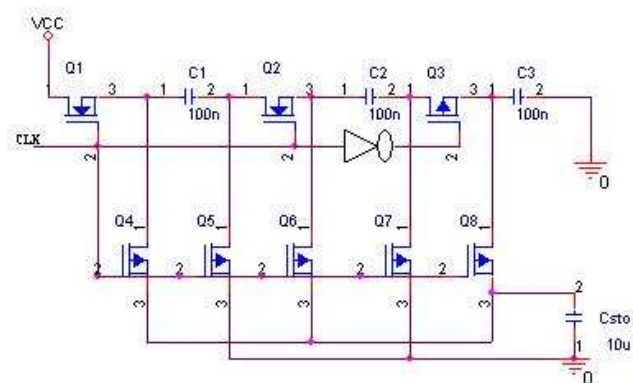


Figure 4. DC-DC power supply

With a VCC of 5,3 V and al CLK of 30KHz the expected simulated circuit output is 1,76V and the measured was 1,72 V, with a load current of 200uA. Measured energy efficiency was 80%.

4. Chopper pre-amplifier for ENG signals

The specifications of this ENG amplifier are close to that in circuit -1- but to achieve low noise, instead of using large area transistors for flicker noise reduction, chopper technique was employed. The design follows the guidelines in [7], with a minimum area oriented design. The topology of the preamplifier circuit is shown in figure 5.

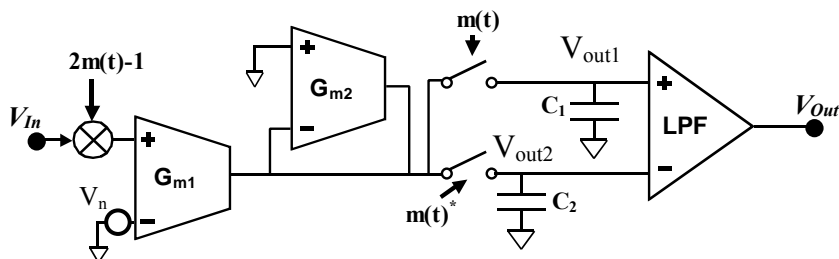


Figure 5: Topology of the proposed G_m -C amplifier. $m(t)$ is a square wave signal.

The circuit is intended to amplify ENG signals with amplitudes greater than $1\mu V_p$ in the band from 100 to 5 KHz. Low noise is critical, initially specified as less than $5 \text{ nV/Hz}^{1/2}$. Additionally, a high CMRR ($\sim 90\text{dB}$) is expected, gain of this first stage must be at least 50, while further amplification can be done in other stages.

Measurement results:

The total circuit area was 1mm^2 including internal low-pass capacitors. The topology, shown in figure 6, was used to measure the amplifier. An instrumentation amplifier INA116 (www.ti.com) was used to amplify the signal, because of it very low input current. The gain of the amplifier was set to 10 during normal measurements, and to 500 for the noise measurements. A 5000 Hz LPF was implemented by an 8th order Butterworth filter using the sallen-key topology and the LT1051 (www.linear.com) operational amplifier. A Tektronix TDS1002 oscilloscope was used for measurement and as a spectrum analyzer. A 20 KHz chopper frequency was used for all measurements.

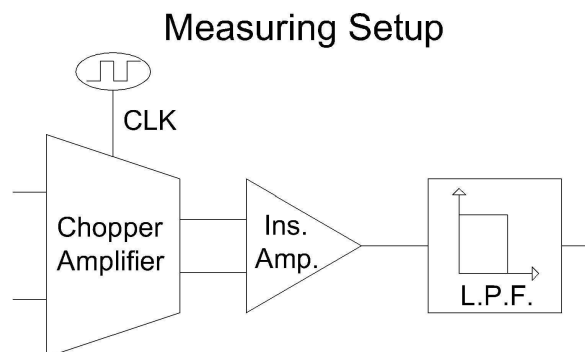


Figure 6: Measurements Setup.

In figure 7, a plot of Gain vs. Frequency is presented. It can be seen that the gain is flat in all the area of interest.

The measured input offset of the amplifier was approximately $2.5 \mu\text{V}$, in all five of the measured samples, suggesting that this is a systematic offset. A CMRR of 88 dB was also measured. The simulated noise was $4 \text{ nV}/\text{Hz}^{1/2}$. Our measurements showed a $1.13 \text{ nV}/\text{Hz}^{1/2}$ in the frequency band. The absence of flicker noise in baseband was observed as it was expected.

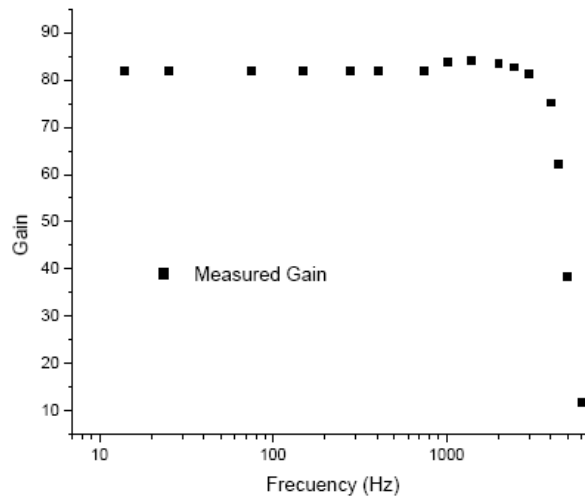


Figure 7: Amplifier Gain vs. Frequency.

Conclusion:

The circuit worked as expected. The designed chopper amplifier fulfils ENG signal acquisition specifications, and its performance is comparable to the circuits presented in [1,2,3] but shows a reduced area while even considering it was fabricated in a 1.5 microns technology.

References:

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