Integrated circuit for cardiac sensing

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Abbreviations

ASIC, application specific integrated circuit.
CMOS, complementary metal-oxide-semiconductor.
DIE, Departamento Ingeniería Eléctrica FIT-UCU.
ESD, electro static discharge.
FIT, Facultad Ingeniería y Tecnologías.
HV, high voltage.
LV, low voltage.
MI, moderate inversion.
SI, strong inversion.
TM, typical model.
UCU, Universidad Católica del Uruguay.
WI, weak inversion.
WP, worst slow model.
WS, worst power model.

Abstract

Microelectronics is an essential tool for the development of implantable medical devices which are being used in the treatment of a growing number of pathologies. The three most important areas in which microelectronics can offer improvements are: low power consumption to extend as much as possible the battery life, to reduce or even avoid the use of external components like resistors and capacitors reducing overall device size, and to develop safe and reliable circuits for the interface with the patient's tissue.

The aim of this project was to develop a complete integrated circuit for the detection of cardiac signals for pacemakers. The design must minimize the use of external components, while also keeping up with the safety requirements and low power consumption of implantable medical devices.

The work was developed using a high-voltage technology (HV, XC06 technology was selected [10]), which includes isolated transistors to better guarantee the safety requirements of the ASIC, and also to facilitate the technology transfer of innovation to the industry, as these technologies are regularly used in implantable medical devices.

In this work, a completely integrated high pass preamplifier, with 25db gain, 4.5µ V_{rms} input referred noise (70-200Hz), and 600nW power consumption was successfully designed. Afterwards, a 55-180Hz GmC filter for a cardiac sensing channel was presented. . It incorporates the ability to filter input signals with a high common mode input up to 15V. Moreover, a novel full wave precision rectifier was developed together to complete the cardiac sensing channel with a low power consuming comparator.

Resumen

La microelectrónica es una herramienta muy importante para el desarrollo de dispositivos médicos implantables. Existen tres áreas dentro de las cuales la microelectrónica ofrece avances relevantes: el bajo consumo (extender la vida útil de las baterías), reducir o evitar el uso de componentes externos y desarrollar circuitos seguros para la conexión con los tejidos de un paciente.

El objetivo de este proyecto fue desarrollar un circuito completamente integrado para la detección de señales cardíacas. Este diseño debe evitar el uso de componentes externos así como cumplir con los requerimientos de seguridad y consumo de corriente.

El diseño fue desarrollado usando una tecnología de alto voltaje (HV, XC06 [10]), la cual incluye dentro de los posibles diseños, transistores CMOS completamente aislados para garantizar los requerimientos de seguridad en el ASIC. A su vez, facilita la transferencia tecnológica hacia la industria ya que esta tecnología es la preferida por los fabricantes de dispositivos médicos implantables.

Se logró desarrollar un preamplificador pasa alto completamente integrado con una ganancia de 25dB, un ruido de referencia a la entrada de 4.5µ V_{rms} y un consumo de 600nW. A continuación, se diseñó un filtro GmC pasa banda (55Hz-200Hz). Finalmente, se desarrollaron un rectificador de onda complete de precisión y un comparador de bajo consumo.

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Chapter 1: Introduction

1.1 Background

Pacemakers sense the natural electric activity of both the atrium and the ventricle of the heart to determine whether is necessary to stimulate it or not [1]. Also modern pacemakers may perform intracavital electrocardiography (ECG) to record the patient's heart electrical activity for a later analysis by the physician. These features are based in a sometimes complex amplifier, filter and detector at the input stage. In a pacemaker, there is at least an amplifier for each chamber [1] [2] [3]. This circuit will be denoted as sensing amplifier.

Microelectronics steadily contributes to the development and improvement of medical devices. The three most important areas in which microelectronics can offer improvements in the design of implantable devices are: low power consumption to extend as much as possible the battery life, to reduce or even avoid the use of external components like resistors and capacitors reducing overall device size, and to develop safe and reliable circuits for the interface with the patient's tissue. In the case of amplifiers, combining low noise and low power becomes also a challenge [5].

A 2.8V (nominal) Lithium-Iodine battery normally power most modern pacemakers. To achieve the larger voltages required during operation, efficient voltage multipliers must be employed [6].

Regarding to the safety of an implantable device, it shall comply with the following rule: any single failure (for example a punctured gate in a MOS transistor) must not cause a catastrophic event. In the case of a circuit in contact with the tissue of the patient, a catastrophic event may be a significant (larger than few μA) DC current flowing to the tissue, or a too high artificial pace rate for the heart. In this work the focus will be on the former, which is closely related to the design of the analog circuits directly connected to the electrodes; a safe design is mandatory in a sensing channel directly connected to the heart. The traditional solution to attain safe circuits in a cardiac sensing amplifier is to include external capacitors in series with the amplifier's input [1] [2] [3] [4]. If any transistor at

the input of the amplifier fails, the series capacitor blocks the DC current. Series capacitors can also help to set a low frequency pole in the transfer function of the input filter-amplifier. But the use of external series capacitors (two for each amplifier) increases the number of external components, thus it will be valuable to develop inherently safe circuits that avoid them. In this work, a so called high voltage (HV) CMOS technology with fully isolated NMOS transistors will be combined with low noise and low power design techniques, to develop a preamplifier aimed for the input stage of a pacemaker that avoids the use of external capacitors. A 0.6μm HV-CMOS technology was employed for the circuit, which includes transistors capable of withstanding even tenths of volts. In spite of the existence of several techniques for the use of standard CMOS technology with relatively high voltages, HV technology is generally preferred because medical equipment manufacturers strictly follow the integrated circuit (IC) manufacturer rules. In the case of pacemakers that must be able to deliver stimuli of voltages up to 7.5V or even more. In the case of this work, the use of HV technology also allows the implementation of an inherently safe preamplifier without external components.

To complete the sensing channel, a relatively precise band pass filter and a negative/positive programmable comparator is required. To achieve minimum power consumption with a fully integrated filter, a transconductor-capacitor (GmC) filter technique was selected for the band pass. Because transconductance element's value suffers from a high degree of uncertainty due to technology parameters dispersion, a detailed analysis was performed to keep the filter response within the 5% boundary that is imposed by common pacemaker regulations. Finally, a novel precision voltage rectifier was developed in conjunction with a single comparator for signal detection.

1.1.1 Research work-group.

Since 2004, the microelectronic's research group of UCU, micro-DIE (http://die.ucu.edu.uy/microdie), has been developing several activities including research, design and consultancy in the area of microelectronics. Within this area of research, the group has been focused in analogical and mixed design for implantable medical devices, low noise design, low power consumption design and low noise amplifiers. In the past few years the group has emphasized the use of high-voltage technologies (HV), as these are used by the

industry. Nowadays, the research group has appropriate work environment for design, which includes CAD design tools and measurements laboratory. This allows the design and characterization of ASICs. Thanks to the MOSIS program and the cooperation of Argentinean and Brazilian universities, the group has already fabricated eight different ASICs, using several technologies (1.6µ, 0.6µ-HV, 0.35µ, 0.35µ-HV and 0.5µ).

µDie also has tight academic relationship with the Federal University of Santa Catarina (LCI-UFSC), the Microelectronic group of the Universidad de la República del Uruguay, the Electric Engineering Department of the Universidad de Rio Grande do Sul – Brazil (PUCC), the Computer Department and the NASCAD project of the Universidad Federal de Rio Grande do Sul – Brazil (UFRGS), the Departamento de Ingeniería Eléctrica de la Universidad Católica de Córdoba – Argentina (UCC), the Departamento de Ingeniería Eléctirca de la Universidad Nacional del Sur – Argentina (UNS) and the Instituto Favoloro de Buenos Aires - Argentina.

1.2 Specifications

The aim of this project is to develop a complete integrated circuit for the detection of cardiac signals for pacemakers. The design must be developed without the use of external components, while also keeping up with the safety requirements and low power consumption of implantable medical devices.

The work was developed using a high-voltage technology; XC06 technology was selected [10], including the ability to implement NMOS isolated HV transistors to better guarantee the safety requirements of the ASIC being developed.

The circuit block for sensing the cardiac activity is one of the main blocks of a pacemaker. The task of the circuit is to amplify natural electric signals form a cardiac chamber, and provide a single bit digital output that indicates when this signal is above a given programmed voltage level (the output of the sensing channel normally triggers an interruption, a sense event in the pacemaker´s microcontroller). This block generally consists of a preamplifier, a band pass filter, and a programmable voltage detector [1] [2] [3]

[4]. In our case it includes a band pass filter with two cut off frequencies, the low one around 70Hz and the high one at 200Hz approximately, followed by a full-wave precision rectifier and a comparator that perform the signal detection [2]. Usually, the lower cut off frequency is set using an external capacitor, but in this work a complete integrated ASIC without external components is designed. Commonly, the cardiac sensing is made directly over the electrodes connected to tissue; therefore the designer must be aware of possible failures and shall prevent them. For example, if the gate of an input MOS is punctured, a DC current must not circulate through the tissue, because this could cause an irreparable damage to the patient.

The general architecture of the whole proposed system to sense cardiac signals is shown in Fig 1.1. It includes a 25dB gain input stage (the preamplifier), a band pass filter-amplifier between 75Hz and 200Hz, a full wave precision rectifier and a low offset programmable comparator to trigger cardiac activity detection [5]. Apart from the DAC, the design of all the elements in Fig.1.1 will be presented in this work.

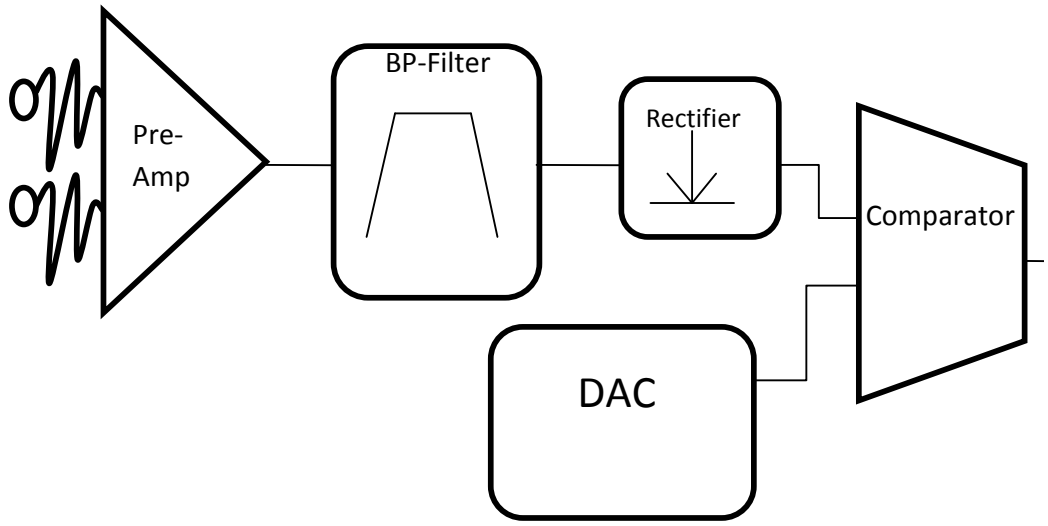


Figure 1.1 System's Architecture.
(The DAC is not part of this work)

The first part of the project was to design an ASIC with a fully integrated preamplifier capable of sensing cardiac activity. This design has three main objectives:

- Reduce as much as possible the number of external components (none if possible).

- Develop the ASIC taking into consideration all the safety specifications and requirements for implantable medical devices.

- Minimize the power consumption.

The second part consisted of developing a biomedical G_mC filter, which would also work as a second stage amplifier. As a second stage is used, the preamplifier can have a larger bandwidth to enable both traditional sensing and intracavital electrocardiography recording with the same preamplifier (not shown in Fig.1.1). Low power consumption and low noise where the two most important aspects taken into consideration when designing this stage. Because transconductance element's value suffer from a high degree of uncertainty due to technology parameters fluctuations between an IC to another (and a fabrication batch to another), a detailed analysis was performed to keep the filter response within the 5% boundary imposed by common pacemaker standards.

Finally, a full wave precision rectifier and a low offset comparator were designed in order to complete the cardiac sensing channel. By rectifying the signal, the detection can be completed in a single comparator for both positive and negative voltage peaks.

The wave used to simulate and test pacemaker devices is the so called Tokyo wave [1][2][14]. Figure 1.2 presents this wave (consecutive positive-negative pulses). It is important to highlight that the signal to detect has an amplitude between a minimum of 200μV and maximum of 10mV approximately. The information necessary for cardiac activity detection is contained in the frequency band from 80Hz to 200 Hz [1] [2] [3] [4].

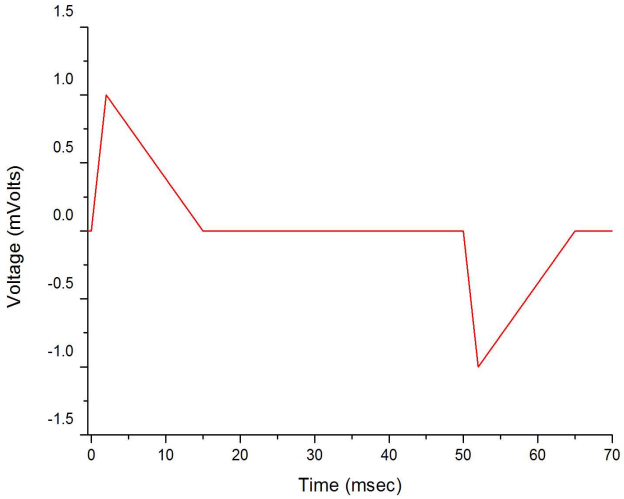


Figure 1.2. Tokyo signal

Chapter 2: Pre-amplifier

The preamplifier is a high pass filter, with a cut off frequency at 75Hz and a 25 dB gain. In Table 2.1, detailed specifications are shown. Additionally, the preamplifier is able to sense signals with a high common mode voltage, up to 8V. The objective is to be able to sense signals around a high voltage V_{DD} if necessary. High voltages are regularly employed for the electrical stimulation of tissue. In the case of a pacemaker the high supply voltage V_{DD} used is generated from the battery with a x2 or x3 charge pump voltage multiplier. (see [6] for example). This high voltage supply is used because medical equipment manufacturers strictly assure in their device's specifications that pacemakers must be able to deliver voltage stimuli up to 7.5V.

Table 2.1

	Requirement
Supply Voltage	6-8V
P. Consumption	<1µW
Cut off Freq	75Hz
Gain	>25dB
Area	<2mm^2
Noise	< 10µV$_{rms}$

In Table 2.1, initial specifications are shown for the preamplifier. Power consumption shall be lower than 1uW to make it negligible in comparison to the overall power consumption of a standard pacemaker [2] [3]. Specified noise floor of 10µVrms is selected; 20 times lower than the minimum atrial signal to be detected.

2.1 HV Technology

Introducing new process layers, a HV CMOS technology allows the fabrication of devices that can support elevated voltages. Regular 5V core CMOS can also be fabricated, as well as double poly capacitors and high-resistivity poly resistors in the target process. In Figure 2.1 a HV NMOS transistor (named NHV) vertical cut is shown. NHV has the usual structure of a HV transistor, incorporating a thick gate oxide that enables up to 18VV_{GS},V_{GB} and the drain diffusion is growth into an N-Well to complete a diffused drain to support elevated V_{DS} voltages.

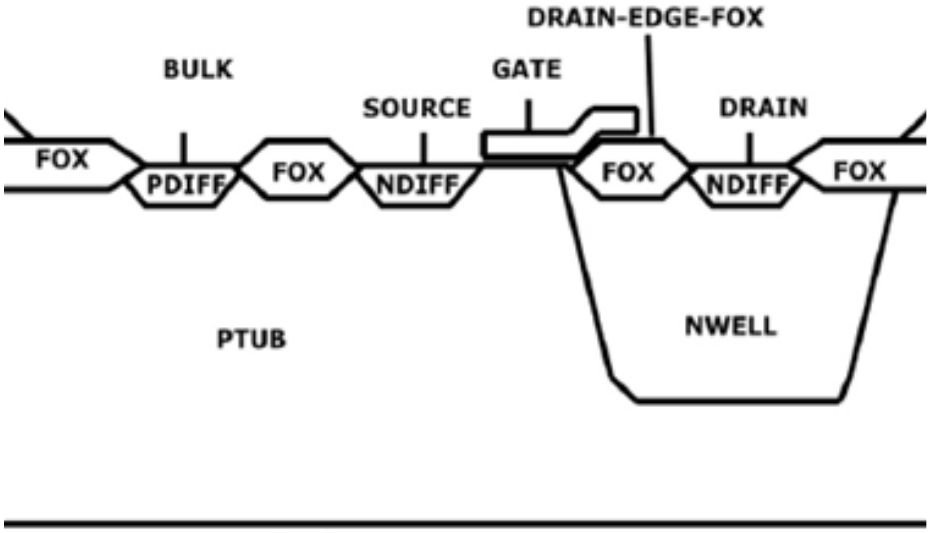


Figure 2.1. Vertical cut of a typical HV NMOS [7].

Apart from regular low-voltage ones, the proposed design included the following types of MOS transistors:

- PHV: This HV-PMOS uses thick gate oxide and a diffused drain to withstandV_{GS}, V_{DS} voltages up to 18V and 40V respectively.

- NHV: The equivalent, HV-NMOS can withstand V_{GS}, V_{DS} voltages up to 18V and 30V respectively.

- NISO: This is a completely isolated HV-NMOS transistor. It withstands V_{GS}, V_{DS} voltages up to 18V and 50V respectively. Its bulk may be connected to different voltages.

To help the interpretation of the circuits in this work (different kinds of HV, LV, transistors are used) in Figure 2.2 the symbols used for each type of transistor are shown. HV transistors are not symmetrical, the drain which is designed to withstand the highest voltage, is marked with a double line.

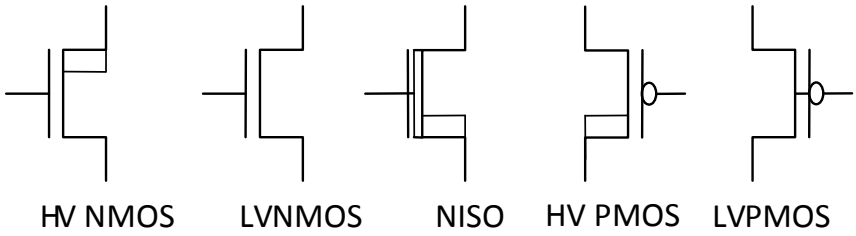


Figure 2.2. Symbols for different kinds of CMOS

2.2 Preamplifier Design

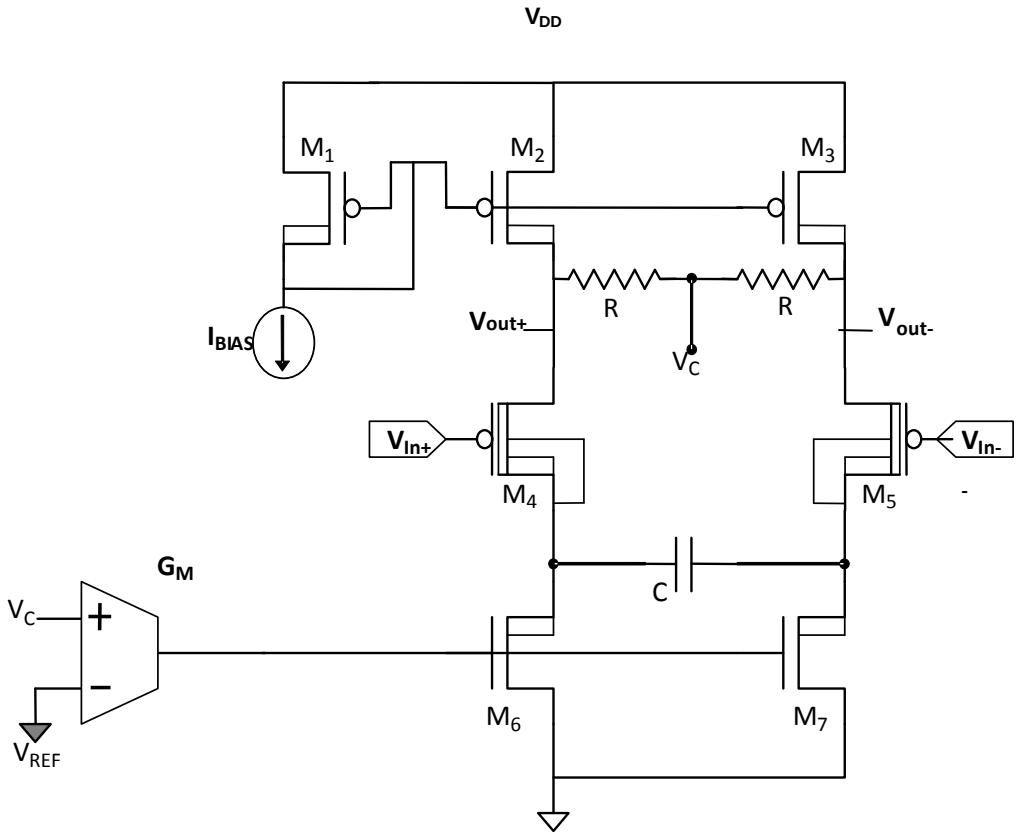


Figure 2.3. First stage: high pass filter-amplifier. Specifications of M1:M7 are shown in Table 2.2

The preamplifier schematic is shown in Figure 2.3; it has a high-pass characteristic. It has a differential input V_{in} directly connected to the electrodes, and a differential output V_{OUT}. It consists of a PHV current mirror, a NISO differential input pair, a NHV current mirror and a symmetric transconductance (OTA)Gm.

The circuit is a variation of the one presented in [8, 9] but uses a symmetric OTA in a common mode feedback loop to set the common mode of the output V_C. By controlling the current through M_6 and M_7, the OTA responds to variations of V_C and fixes it equal to a reference voltage V_{REF}.

Table 2.2

	Type	W-L(µm)
M_1:M_3	PHV	40-20
M_4:M_5	NISO	50-9
M_6:M_7	NHV	40-20

Conducting a small signal analysis of the high-pass filter-amplifier (shown in Figure 2.4), the high pass filter's transfer function $H_1(s)$ was determined in eq(2.1) to eq(2.5).

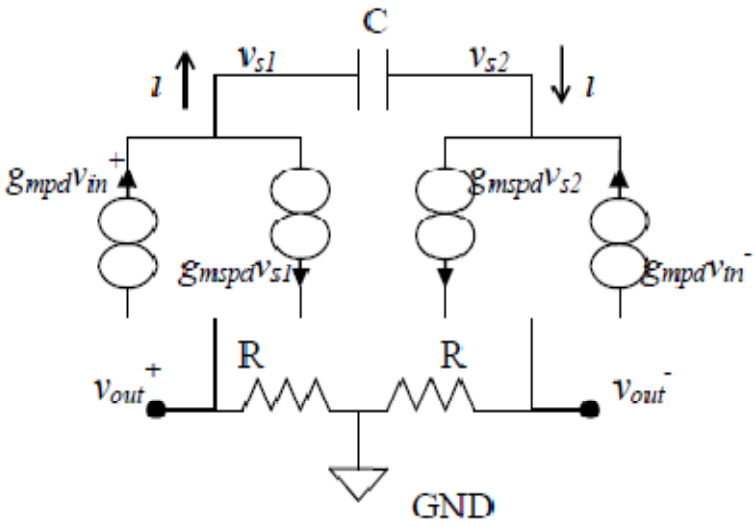


Figure 2.4. High pass filter small signal model. [11]

$$i = g_{mpd} \cdot v_{in}^{+} - g_{mspd} \cdot v_{s1} \tag{2.1}$$

$$g_{mspd} = \eta g_{mpd} \tag{2.2}$$

$$i = -g_{mpd} \cdot v_{in}^{-} + g_{mspd} \cdot v_{s2} \tag{2.3}$$

$$i = (v_{s1} - v_{s2}) \cdot Cs \Rightarrow v_{s1} - v_{s2} = \frac{1}{Cs} \tag{2.4}$$

$$\boxed{H_1(s) = \frac{Rg_{mpd} \cdot s}{s + \dfrac{\eta g_{mpd}}{2C}}} \tag{2.5}$$

where R, C are those in Figure 2.4, g_{mpd} , g_{mspd} are the gate and source transconductances of the differential input pair respectively and $\eta = 1 - 1.5$ is the slope factor [12].

According to the available area budget, the largest capacitor that could be used was a 400pF poly-poly one, occupying an area of

0.22mm^2. To set the gain at 25dB and the cut off frequency at 75Hz, and selecting C = 400pF:

$$g_{mpd} = \frac{4\pi \cdot C \cdot f}{\eta} = 0.27\,\mu S \tag{2.6}$$

$$\frac{G}{g_{mpd}} = R = 56.6 M\Omega \tag{2.7}$$

being G the total gain.

Due to the low values of g_{mpd} required, a relatively low bias current will be employed in the differential pair. Also the input MOS transistors will be biased in weak inversion to reduce noise and input offset. An all region model was used for the design space exploration [12] but the final transistor size was selected as a multiple of the HV unitary transistor standard cell (it should be pointed that HV transistors has a fixed or little flexible layout given by the manufacturer). An extremely low bias current is consistent with power consumption reduction because the preamplifier can be connected to a high V_{DD} voltage. The bias current I_{BIAS} is only 16nA to preserve reduced power consumption. The total input referred noise of the preamplifier is estimated in $4.5\ \mu V_{rms}$ including flicker noise, a value several times lower than the minimum atrial signal that would be detected. Noise was approximated using standard thermal noise model, and empirical flicker noise model; parameters were obtained from manufacturer's data. Detailed calculations are omitted for the sake of simplicity.

2.2.1 Safety Considerations

Regarding safety, the amplifier in Figure 2.3 does not deliver a DC current to the tissue in the case of a single failure. In effect the electrodes are connected to the gate of M_4 and M_5, in the case of a punctured gate, or gate to source (drain) conductive path, the current through the mirrors is limited to the 20nA I_{bias} copy. Thus no external decoupling capacitors are required. To complete the safety analysis it should be pointed that the OTA (GM) is also HV, and that under regular operation (no extra failures) the bias voltage of the electrodes is such that all parasitic diodes in the MOS transistors are reverse biased. Also special electrostatic discharge (ESD) protections were included, but the discussion of ESD is developed in forward sections.

2.2.2 Symmetric OTA.

The OTA's aim was to set the common mode of V_C in Figure 2.3 by acting as a common mode feedback loop. This ensures the amplifying stage works correctly despite current variations. Figure 2.5 shows the OTA schematic. It has a current consumption of 16nA ($I_{BIAS} = 4nA$).

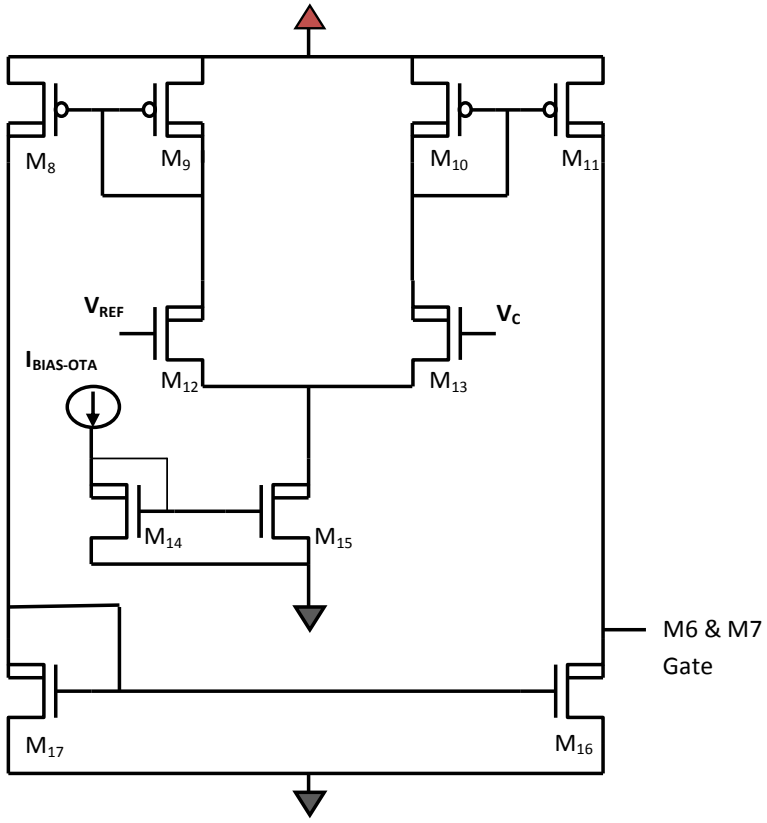


Figure 2.5. OTA's design. Specifications of transistors M8:M17 are shown in Table

Table 2.3

	Type	W-L(µm)
M_8:M_{11}	PHV	40-20
M_{12}:M_{13}	NHV	20-10
M_{14}:M_{17}	NHV	40-20

The OTA's transconductance exactitude is not a must. Thus, transistor sizes in Table 2.3, as well as the bias current, were selected to reutilize as much as possible the layout of the previous block. In spite of the fact that the resulting Gm area is quite large, large area transistors help to preserve a reduced circuit offset to set a precise V_C voltage. The large Gm area is still much smaller than the large resistor and capacitor of the previous block.

2.3 Auxiliary designs

In order to test the correct operation of the preamplifier system it was necessary to design several elements including:

- Test Buffer: This element was designed to allow the measurement of the preamplifier output using standard equipment load (Oscilloscope probes 1MΩ - 10pF).

- Current distribution: A circuit block to copy and distribute current references for all the circuits from just one single current reference.

- Analog switch: Four analog switches weere developed to choose whether to enable or not the output buffers

Figure 2.6 shows the complete block diagram, including the auxiliary devices.

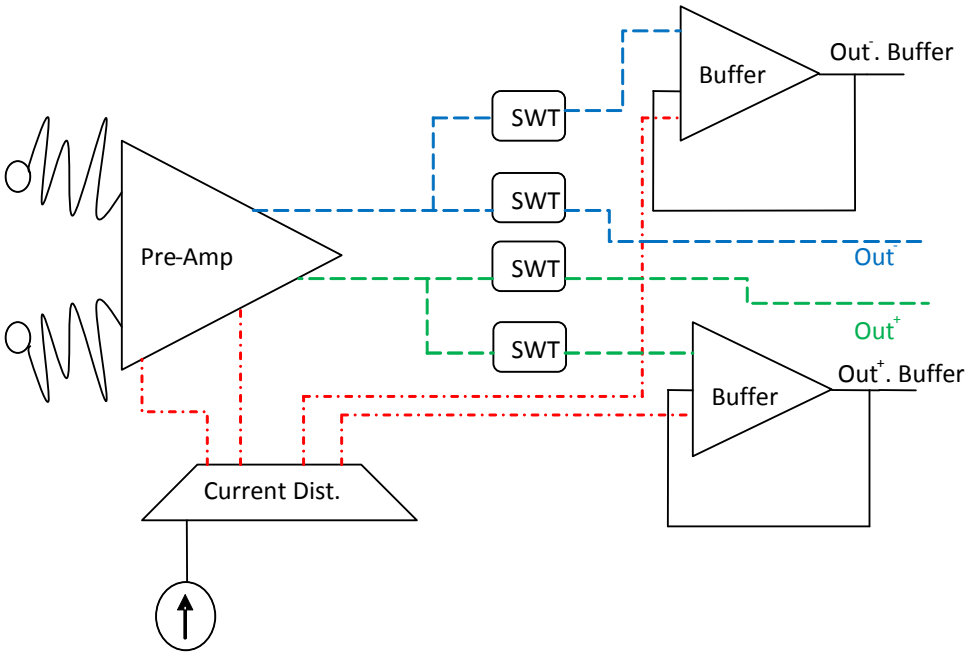


Figure 2.6. Stage one block diagram

2.3.1 Current distributor

This circuit supplies the feedback transconductor, the two buffers and the preamplifier with their respective current reference. The references are derived from an Ip = 48nA single external one The distributor divides the current Ip by three to feed the amplifying stage and both buffers, and divides the current by twelve to supply the OTA.

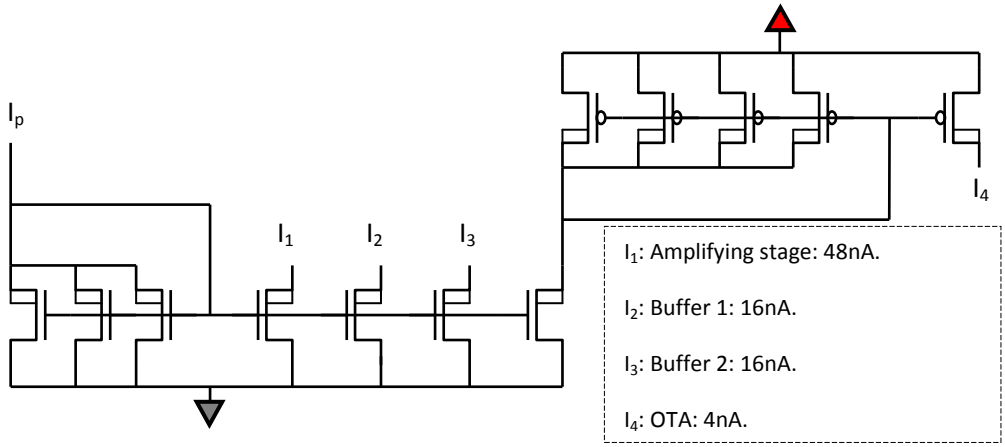


Figure 2.7. Current distributor schematic.

2.3.2 Buffers

This circuit was developed to increase the charge capacity of both preamplifier outputs in order to facilitate measurements using standard equipment. As Figure 2.6 shows, the actual outputs, without going through the buffers are also available. Figure 2.8 shows the schematic of one buffer.

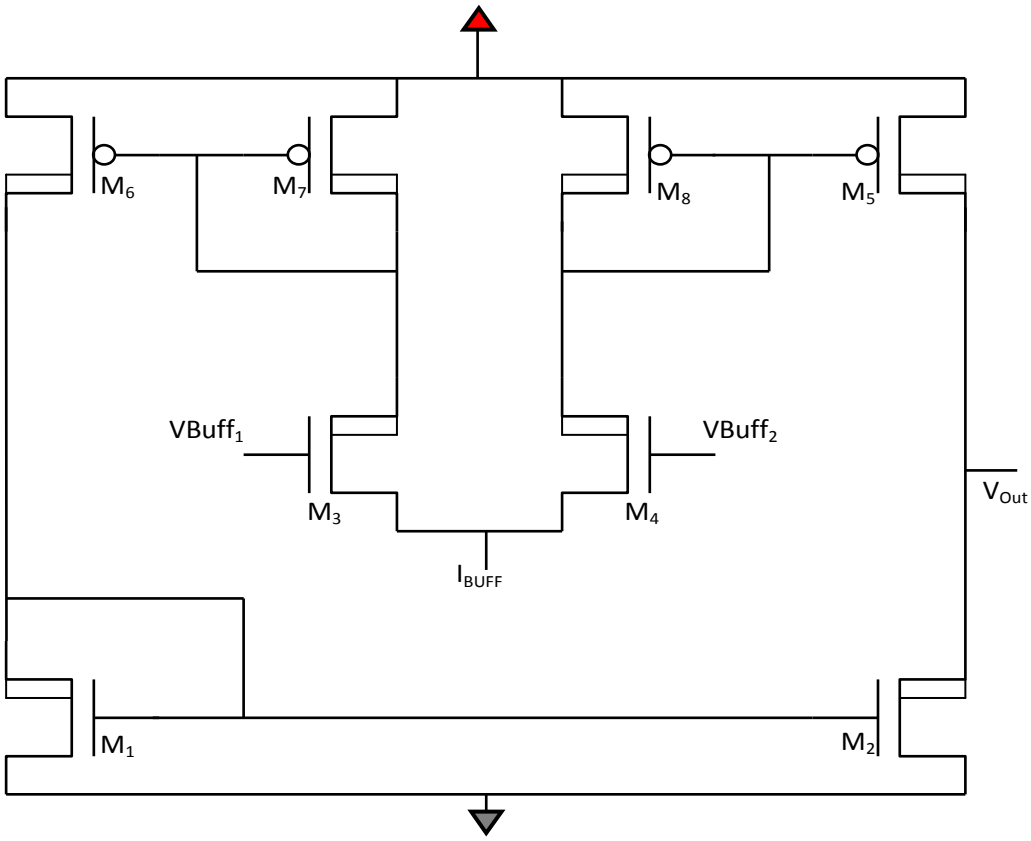


Figura 2.8. Buffer's schematic design.
Specifications of transistors M1:M8 are shown in Table 2.4.

Table 2.4

	Type	W-L(µm)
M_1:M_2	NHV	25-50
M_3:M_4	NHV	20-10
M_5:M_6	PHV	100-60
M_7:M_8	PHV	10-60

$VBuff_1$ corresponds to the Buffer proper feedback. $VBuff_2$ corresponds to the signal for buffering. I_{BUFF} is the polarization current supplied by the current distributor. V_{Out} is the amplified output.

2.3.3 Analog Switches

The analog switches are used to enable the use of the buffer to improve the outputs. They were developed by using only one CMOS-PMOS transistor.

2.4 Pads

The PAD is a very important element to take into consideration when developing an ASIC. It connects the integrated circuit through wires to the different outputs (to the PCB). Apart from the physical connection, a very important task of the PAD is to protect the inner circuit from electro-static-discharge (ESD) current spikes that may damage it.

The ESD protection circuit limits the voltage between internal nodes and provides a discharge path to avoid current spikes. The ESD protection must comply with the following rules:

- Discharging paths capable of bypassing any ESD stress.
- Provide a high protection with minimum layout area.
- Capability of protecting themselves against ESD damage during a discharge.
- Remain inactive during a normal operating condition.
- Cause minimum signal delays.

In the case of a medical device connected to biological tissue, safety considerations involve also ESD protection devices.

XC06 allows the stacking of low voltage ESD protection devices to achieve higher break down voltages to use as a high voltage ESD protections device. Figure 2.9 shows the high voltage I/O protection pad used for this ASIC.

If a positive ESD event occurs, the discharge will be through the stacked NPN snap-back parasitic bipolar transistor. If a negative ESD event occurs, the discharge is through the stacked diodes. The transistors layout and sizes were determined following the manufacturer's guideline [13].

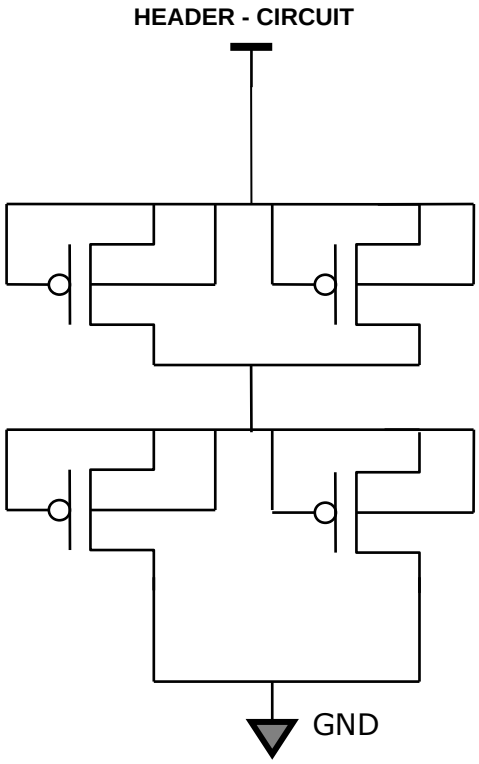


Figure 2.9. High voltage pad. All MOS have the same size (L=0.7µm & W=500µm)

Thirteen PADs were implemented so as to connect the circuit to the exterior. The inputs and outputs used for stage 1 are detailed in Table 2.5.

Table 2.5

PAD	Comments
V_+	Positive differential preamplifier input.
V_-	Negative differential preamplifier input.
V_r	Reference voltage used by the OTA inside the preamplifier to set the common feedback voltage V_c
V_{DD}	Supply voltage.
I_p	Polarization current used by the current distributor to supply all the devices with current.
G-PMOS	Controls the inverter's gate.
B-PMOS	Controls the inverter's bulk.
$V_{DD}B$	Buffer's supply voltage.
$V_{out-}B$	Negative differential output through the buffer.
$V_{out+}B$	Positive differential output through the buffer
V_{out-}	Negative differential output
V_{out+}	Positive differential output
GND	Ground

2.5 Layout

In this section, the first-stage layout design, including the pads, is shown.

2.5.1 OTA

Figure 2.8 shows the OTA's layout. A part of the preamplifier's layout may also be seen in Figure 2.10. The second group of MOS transistor from the bottom right corner, the current mirror of the OTA that bias the input pair, was located (red rectangle). In the centre of the Figure, the input pair of the OTA was drawn(blue rectangle). In the left part of the Figure the current mirrors (PHV-MOS) are shown(green rectangle) and in the bottom right corner the NHV-MOS current mirrors may be distinguished(yellow rectangle). All other devices are part of another neighbouring circuit. Total area: 0.52mm^2.

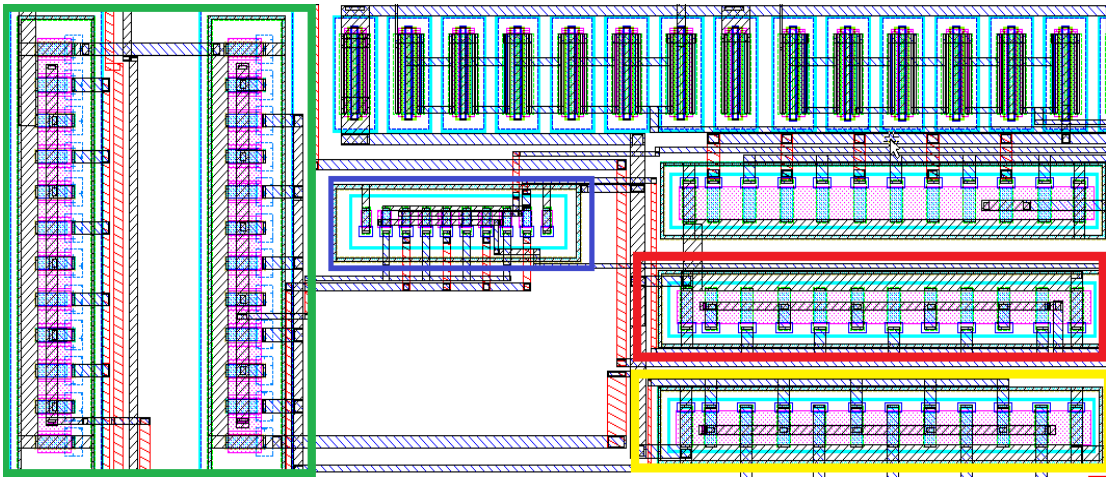


Figure 2.10. OTA Layout

2.5.2 Buffer

Figure 2.11 shows the layout of both buffers. In the top and bottom part of the image the two PMOS mirrors can be distinguished (green rectangle). In the centre, the NMOS mirror was placed (blue rectangle). Next to it, the NMOS input pair was placed (red rectangle). Total area: 0.185mm^2 each.

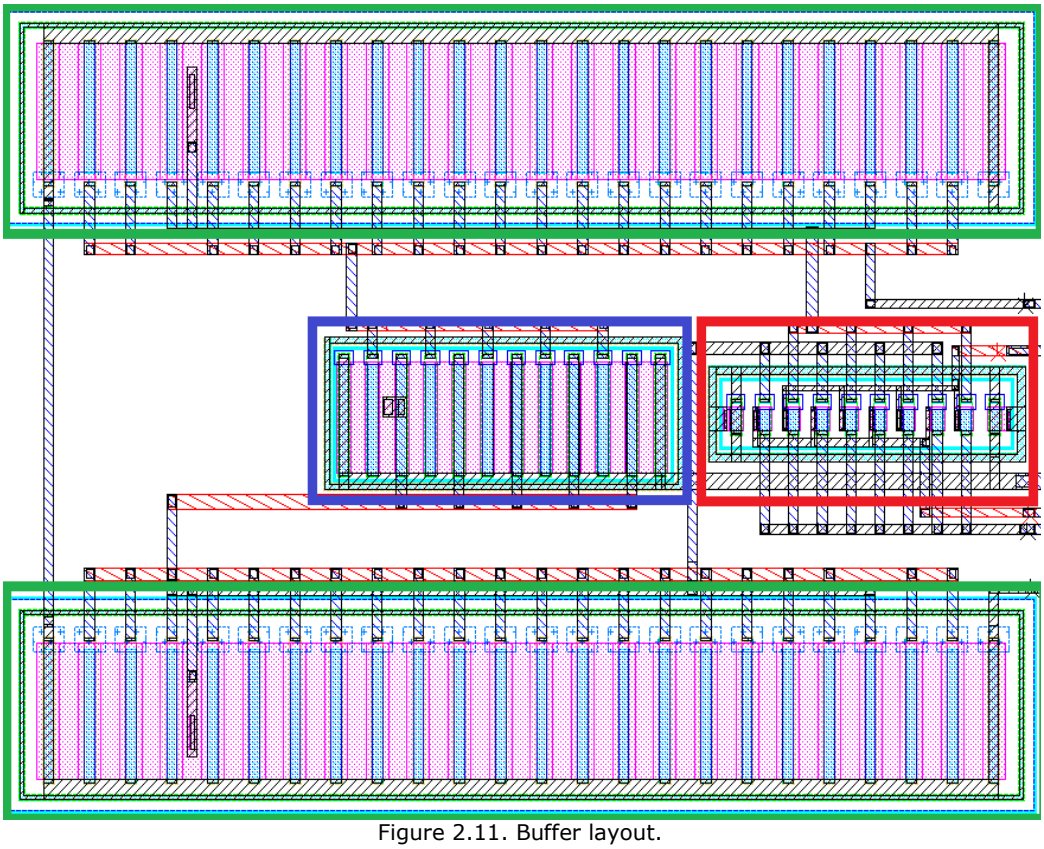


Figure 2.11. Buffer layout.

2.5.3 Current distributor

In Figure 2.12 the current distributor's layout can be observed. In the top part of the Figure the PMOS current mirror which supplies the OTA is shown (red rectangle). In the bottom part of the image the NMOS current mirror that supplies the buffers and the preamplifier is depicted (blue rectangle). Total area: 0.027 mm^2.

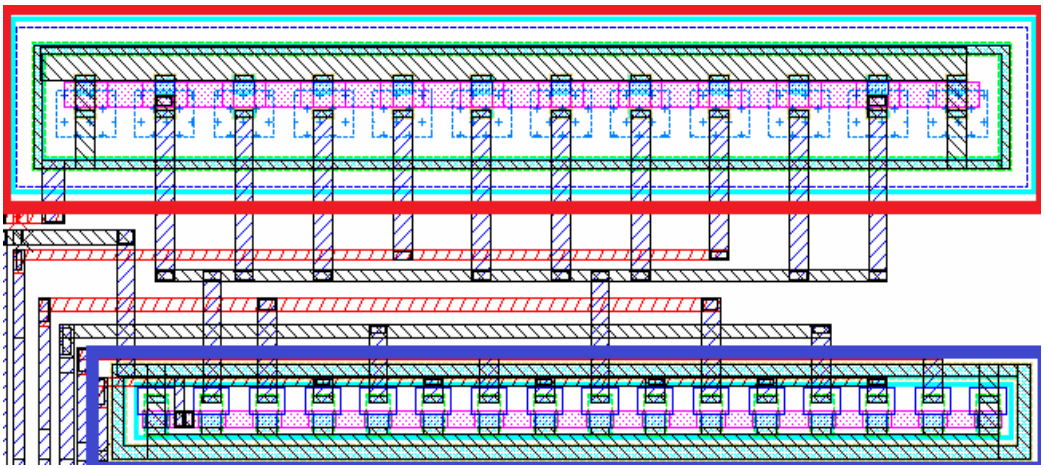


Figura 2.12. Current distributor layout.

2.5.4 Amplification stage

Figure 2.13 shows the preamplifier's layout. At the top centre part of the figure the resistance's layout can be seen (blue rectangle). Next to the right the 400pF capacitor is shown (red rectangle). In the left part of the image the PMOS mirror was drawn (green rectangle). At the bottom part the NISO differential input pair was placed (orange rectangle). Total area: 0.480mm^2.

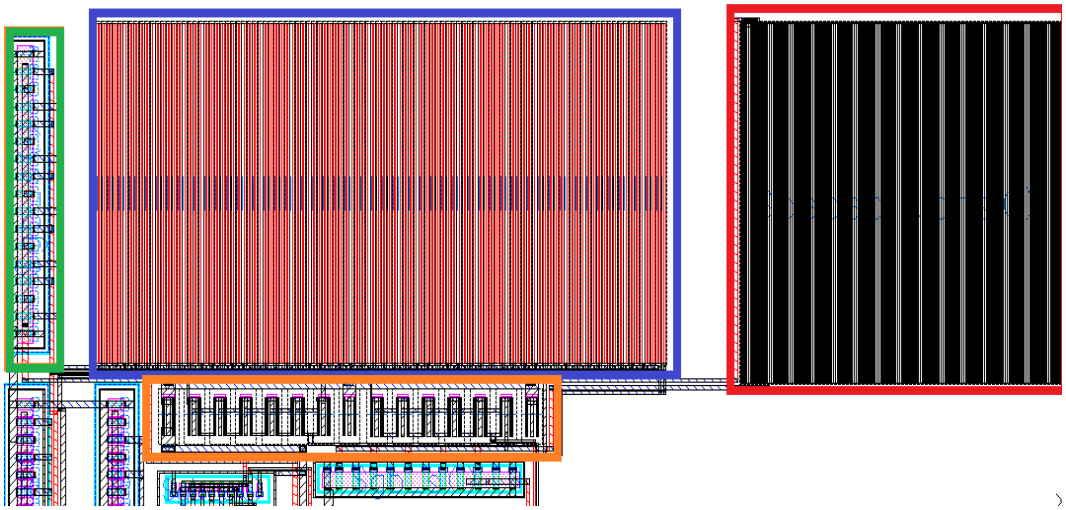


Figure 2.13 Amplification stage layout.

2.5.5 Complete design

The whole system's layout design is shown in Figure 2.14. In the bottom part one buffer (red rectangle) and the current distributor (blue rectangle) is presented. At the centre-right part the other buffer (red rectangle) and the four switches were drawn (green rectangle). The design is completed with the OTA and the amplification stage (pink rectangle). Total area: 1.53mm^2 with auxiliary devices, 1.13mm^2 without auxiliary devices.

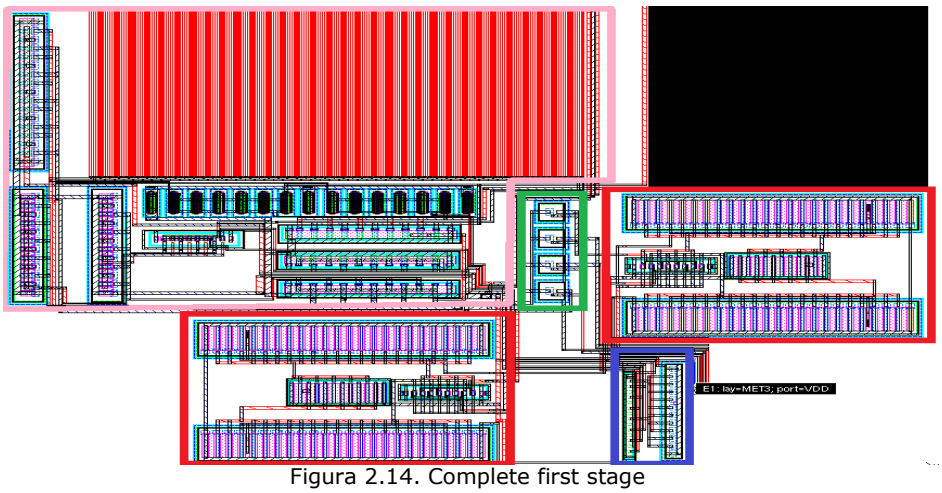


Figura 2.14. Complete first stage

2.5.6 PADS

The layout of the PADS is shown in Figure 2.15. The top part of the design is the header of the PAD and each strip resembles each pair of ESD-PMOS transistor. Each PAD has a total area of: 0.04mm2.

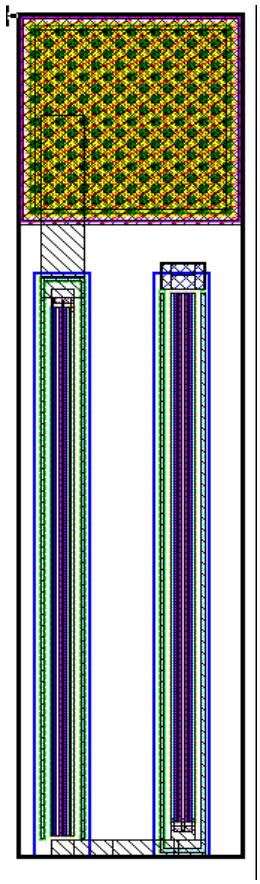


Figure 2.15. PAD's Layout.

2.6 Simulations

All the simulations presented in this section are post-layout ones, including parasitic effects (without PADS). BSIM3v3 models are provided by the manufacturer.

In Figure 2.16, the AC transfer function of the preamplifier is presented. The simulated gain is 26dB and the cut off frequency (-3dB) is 75Hz. It should be noted that the filter acts as a pass band filter because it is powered by a very low current, and the parasitic capacitors of the large transistors employed result in a low pass pole at approximately 1KHz, which is much greater than the largest frequency of interest. The effect can be exploited also as an antialiasing filter in the case of a possible switched filter second stage.

Simulations were also carried for corner cases using the different transistor and resistor models provided by the foundry. The results can be seen in Table 2.6.

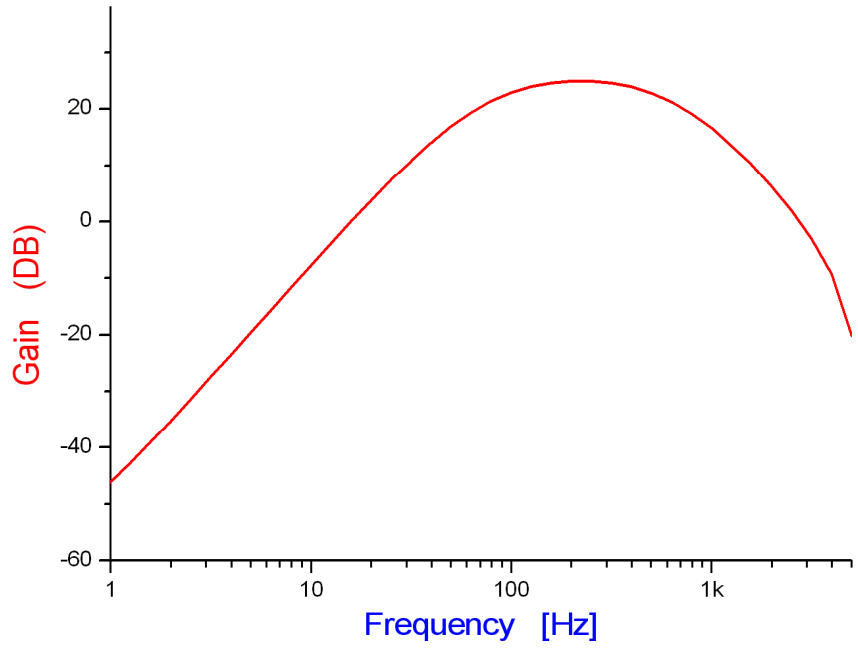


Figure 2.16. AC Simulation

Table 2.6

	TM	WS	WP
Gain(dB)	26	24	27.5
Cut off Freq(Hz)	75	97	66.5
Consumption(µW)	0.60	0.60	0.60

Two more simulations were also carried out which are presented in Figure 2.17 and Figure 2.18. Figure 2.17 presents the result for a sine wave input of $Vmax = 1.2mV$ and $freq = 100Hz$. In Figure 2.18 the output of the system is shown, when the so called Tokyo wave was used as the input signal. This wave is the standard one defined to test sensing amplifiers for cardiac pacemakers [14]. Both positive and negative Tokyo signals with $Vmax = 2.9m$, $t_{positive} = 3ms$ and $t_{negative} = 42ms$ were simulated.

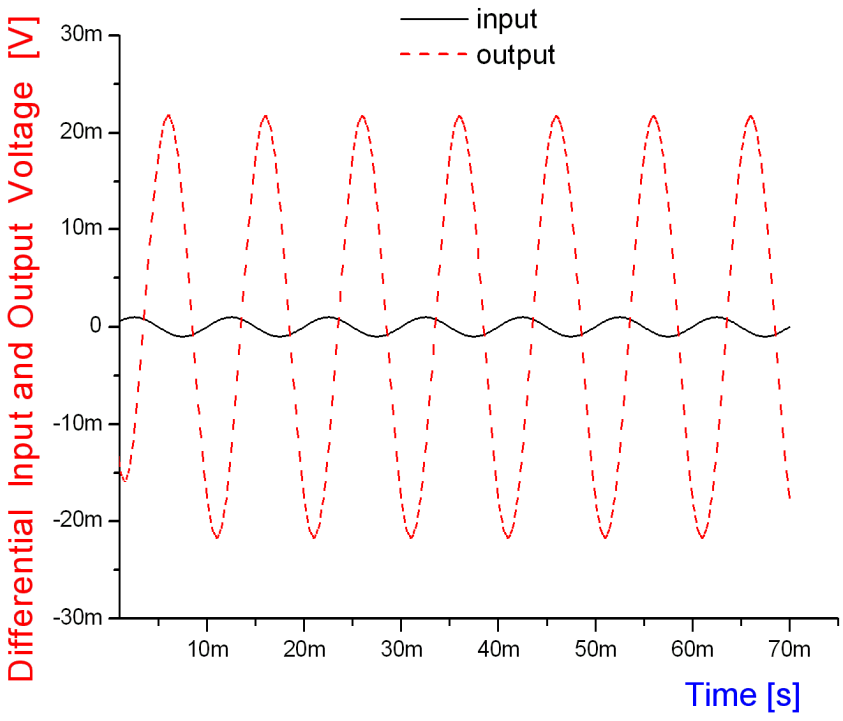


Figure 2.17. Transient analysis with sine input.

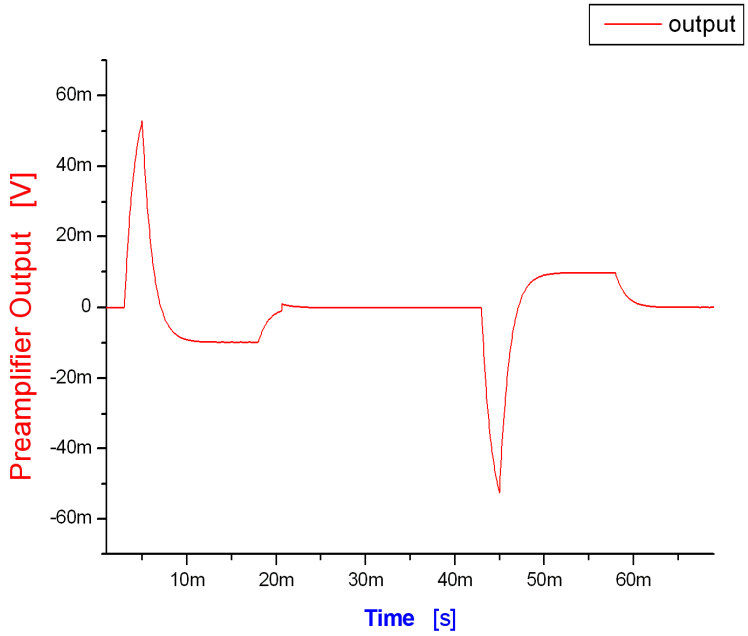


Figure 2.18. Output for a positive and negative Tokyo input with an amplitude of 2.9mV.

Table 2.7 presents the simulated specifications of the preamplifier.

Table 2.7

Specification	Requirement	Simulated
Supply Voltage	6-8V	6-8V
P. Consumption	<1µW	0.60 µW
Cut off Freq	75Hz	75Hz
Gain	>25dB	26dB
Area	<2mm^2	1.53mm^2
Noise	< 10µV$_{rms}$	4.5 µV$_{rms}$
Offset	ND	1.4mV
C. Mode Voltage(+)	ND	V_{DD} + 0.2V
C. Mode Voltage(-)	ND	800mV

Chapter 3: G_m-C Filter

The second stage is a GmC filter to remove undesired spectral components, which also work as a second stage amplifier. As pointed in [2] the information to detect natural electrical cardiac activity is most contained in the band from 70 to 200Hz, thus the GmC filter shall be a band pass one approximately in that range. In this chapter the complete design of a GmC filter compliant with the previous stage is presented, particularly investigating the spread in its transfer function due to the variability of the technology parameters of the integrated circuit (no trimming or filter tuning is assumed).

In [4] [6] a discrete time switched capacitors filter is proposed for a similar task, while in [3] [15] a continuous time RC one is presented but the circuit requires precise external components. In comparison to the mentioned approaches, GmC filters may result in minimum power consumption, and a fully integrated solution. But while filter accuracy is not crucial for the application as cardiac sensing level is adjusted by the physician in a pacemaker therapy; the standards may impose certain minimum accuracy in the response of the circuit. Therefore to avoid individual trimming of the devices, the GmC filter must be precise. The standard in [14] for example, uses the so called Tokyo signal as the normalized test signal; and defines a mandatory 5% accuracy in the detection. But note from the Tokyo signal Fourier transform in Figure 3.1 and the analysis of Figure 3.2 that the high frequency pole does not necessarily have to be accurate (a 10% variation in it results in much less than ±5% variation of the signal amplitude at the output); and the position of the low frequency pole has a limited yet still significant impact (around 8% for a maximum expected. Both results (Figure 3.1 and Figure 3.2) were obtained using a MATLAB script that filters an ideal Tokyo signal with a band pass varying the position of the poles.

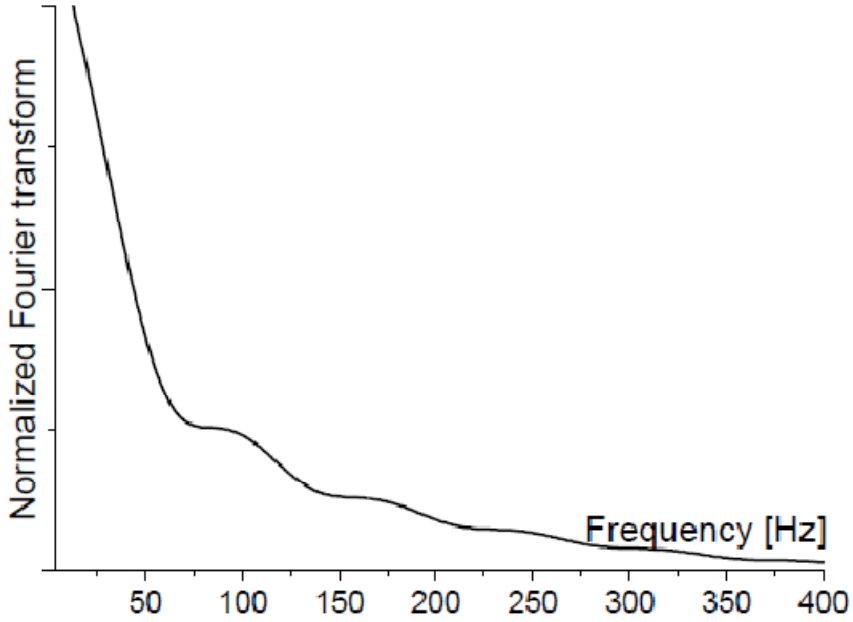


Figure 3.1 Fourier transform of the Tokyo signal.

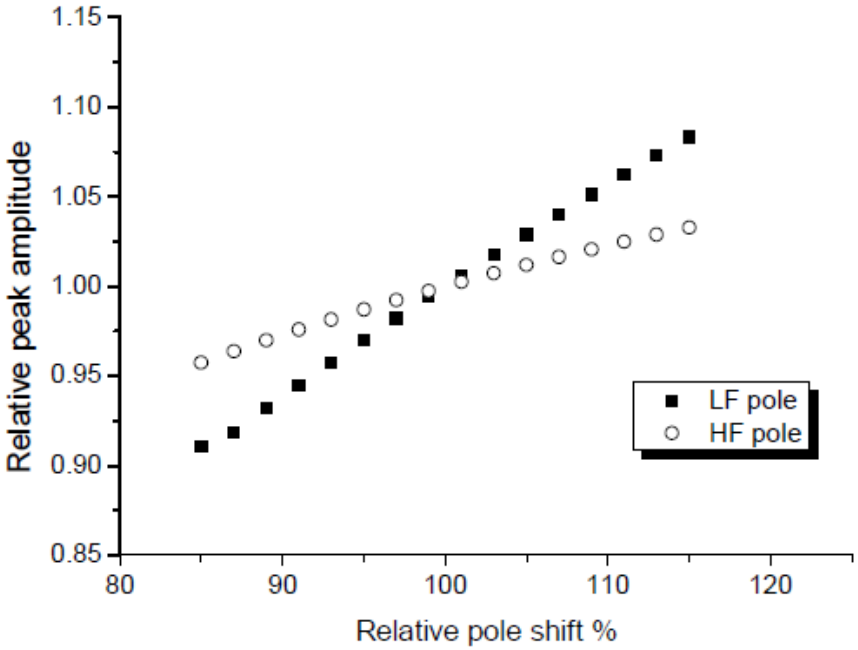


Figure 3.2 Estimation of the overall channel sensing accuracy.

With the addition of some previous experience showing that the measured transfer function of a GmC approximately fits the typical expected curve, it is possible to conclude that the effort in the design shall be in the adjustment of an accurate gain within 5% instead of an accurate position of the poles.

3.1 Circuit description

The proposed GmC is shown in Figure 3.3 and Table 3.1. The selected band pass filter topology in the picture has a total stage gain of $G = 22\,dB$. The filter is composed of a low pass gain structure (given by Gm_1, Gm_2, C_2 similar to that proposed in [16] for a capacitive microphone, and a DC cancellation loop (given by Gm_3,C_1). Capacitors are of the double poly type.

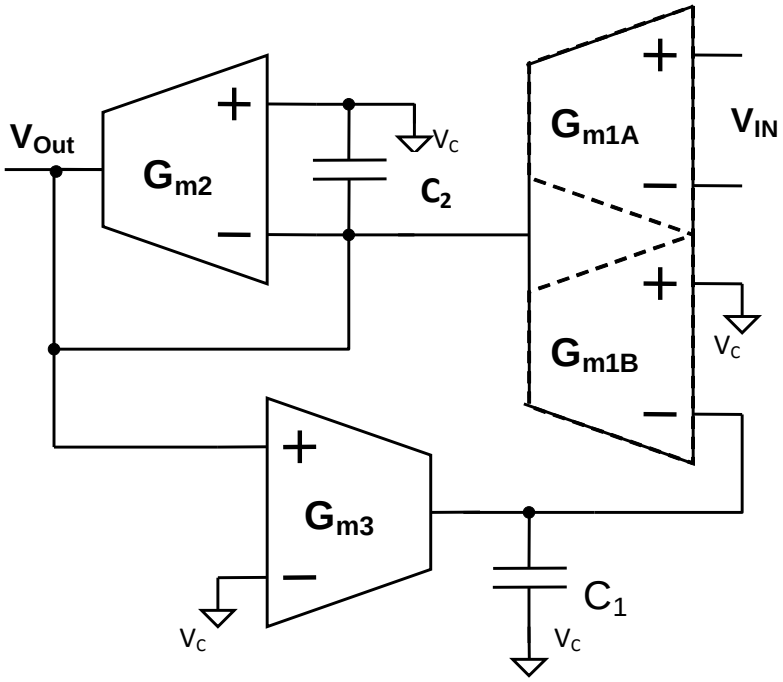


Figure 3.3. A schematic of the designed G_mC filter for the sensing cannel.

The same 0.6µm-HV technology was employed in the design (as in the first stage). Two different supply voltages (V_{DD} and $HighV_{DD}$) were used to allow the GmC to be connected to a high voltage differential input signal (the output of the previous stage), but the rest of the filter is powered from the battery V_{DD} for the sake of a reduced power consumption.

Table 3.1

	Value	Comments
G_{m1}	1µS	Dual input. HV input capacity on one side.
G_{m2}	80nS	Resistor-linearized OTA. ±500mV range
G_{m3}	1.6nS	Resistor-linearized OTA. ±500mV range
C_1	105pF	Poly-Poly Capacitor
C_2	45pF	Poly-Poly Capacitor

To determine the values detailed in Table 3.1 the circuit was analyzed. The filter's (Figure 3.3) transfer function is:

$$H_2(jw) = \frac{jwA_0}{jw(1+{}^{w}/_{w_l})+A_0k} \qquad \text{eq(3.1)}$$

Where w_l is the cut off frequency of the low pass filter and $A_0 = \frac{G_{m1}}{G_{m2}}$. The transfer function may be better expressed in the form of a second order stage using centre frequency w_0, and quality factor Q:

$$H_2(jw) = \frac{jww_0/Q}{{w_0}^2+jww_0/Q-w^2} \cdot \frac{Qw_0}{k} \qquad \text{eq(3.2)}$$

With ${w_0}^2 = {A_0}^2 k w_L \; and \; Q = \sqrt{\frac{A_0 k}{w_L}}$. The roots of the polynomial denominator of eq(3.2) are:

$$w_{p1} = -jw_0\left[\frac{1}{2Q} - \sqrt{\frac{1}{4Q^2}-1}\right]$$

$$w_{p2} = -jw_0\left[\frac{1}{2Q} + \sqrt{\frac{1}{4Q^2}-1}\right]$$

An excel calculation sheet was used to determine the values presented in Table 3.1. The values that were firstly imposed were the ones of the Capacitors, using an area criterion. Afterwards, all the other values came up by using the equations.

3.2 G_m1

Gm_1 is a double differential input transconductor. The first input is connected to the preamplifier stage thus shall support a high voltage common mode input. The second input is used as a feedback port for DC cancellation in the scheme of Fig.3.3. Only the first OTA input is connected to a high voltage supply ($HighV_{DD} = 8V$); the feedback input is powered by a lower V_{DD} to preserve reduced power consumption. Therefore the 1µS double input OTA, shown in Figure 3.4, is divided in two parts.

- The HV part has a HV-NMOS differential pair input that was implemented with complete isolated transistors (NISO) biased in Weak Inversion with an 80nA current. The two MOS transistor that bias the input mirror (HV-NMOS) and the four PMOS transistor located at the top part of the circuit are also high voltage ones (HV-PMOS). The remaining MOS transistors are standard NMOS.

- The low voltage part has a standard PMOS differential input pair also biased in weak inversion with an 80nA current. The mirror was also implemented with standard PMOS transistors.

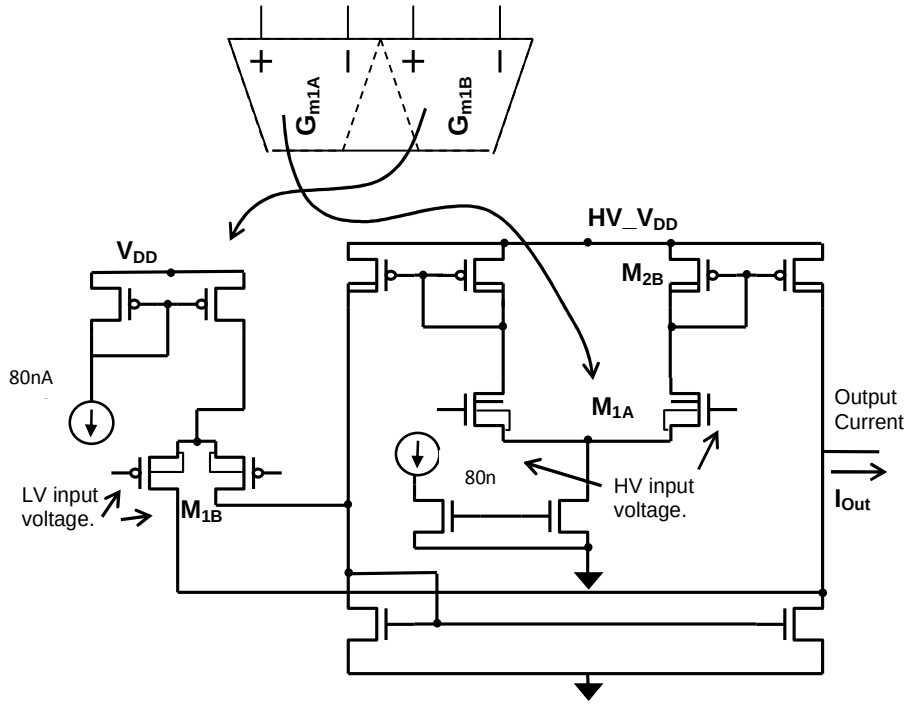


Figure 3.4. Double input Gm Schematic. The characteristics of both input pairs are detailed in Table 3.2. The total current consumption reaches 320nA.

Table 3.2

	Type	W-L(µm)
$M_{1A}(2)$	PMOS	50-3
$M_{1B}(2)$	NISO	20-10

3.2.1 Layout

Figure 3.5 points out the double input Gm's layout. In the bottom part of the image the HV-NMOS mirror was situated (blue rectangle). Next to it, the NMOS mirror can be seen (red rectangle). At the centre of the figure, the NISO input pair was located (green rectangle). To the right and to the left of it the HV-PMOS mirrors were drawn (orange rectangle). In the left part of the image the low voltage part of the Gm was situated (purple rectangle); in the top part the PMOS mirror and in the bottom part the PMOS input pair. Total area: 0.35mm^2.

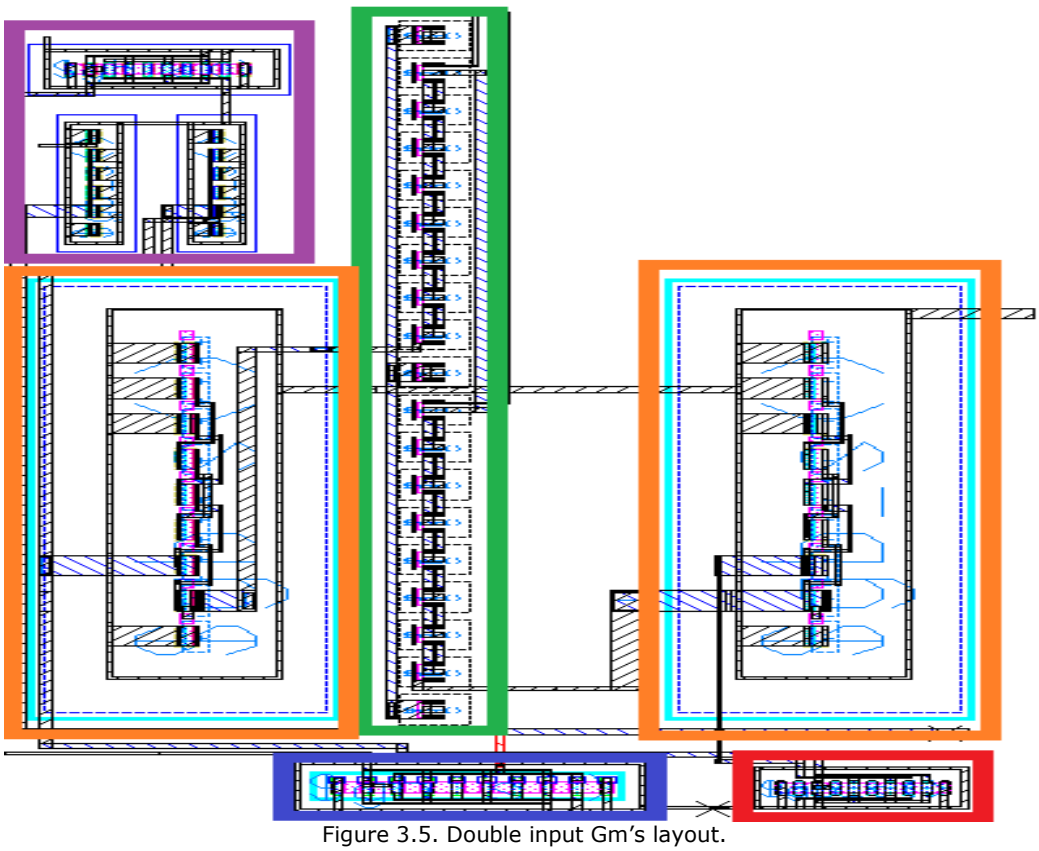


Figure 3.5. Double input Gm's layout.

3.2.2 Simulations

A simulation was carried out to verify the correct operation of the Gm, it's value and to check the linear range of the circuit. Figure 3.6 shows the current at the double input Gm's output. The slope is 0.98μS and the linear range reaches the 180mV.

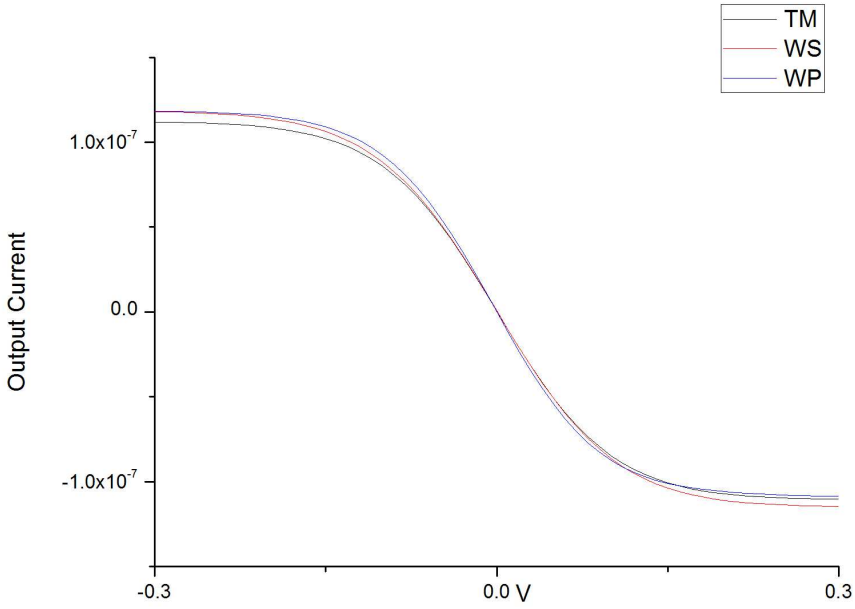


Figure 3.6. Output Current when varying the high voltage input.

3.3 G_m2 and G_m3

To complete the full GmC filter, two resistor linearized trasnconductors were designed using the same topology, and only slight changes in the length and width of transistors. A schematic is shown in Fig.3.7

The input pairs were biased in moderate inversion (MI) and the resistor's value is 7MΩ. The total current consumption of each transconductor is 160nA.

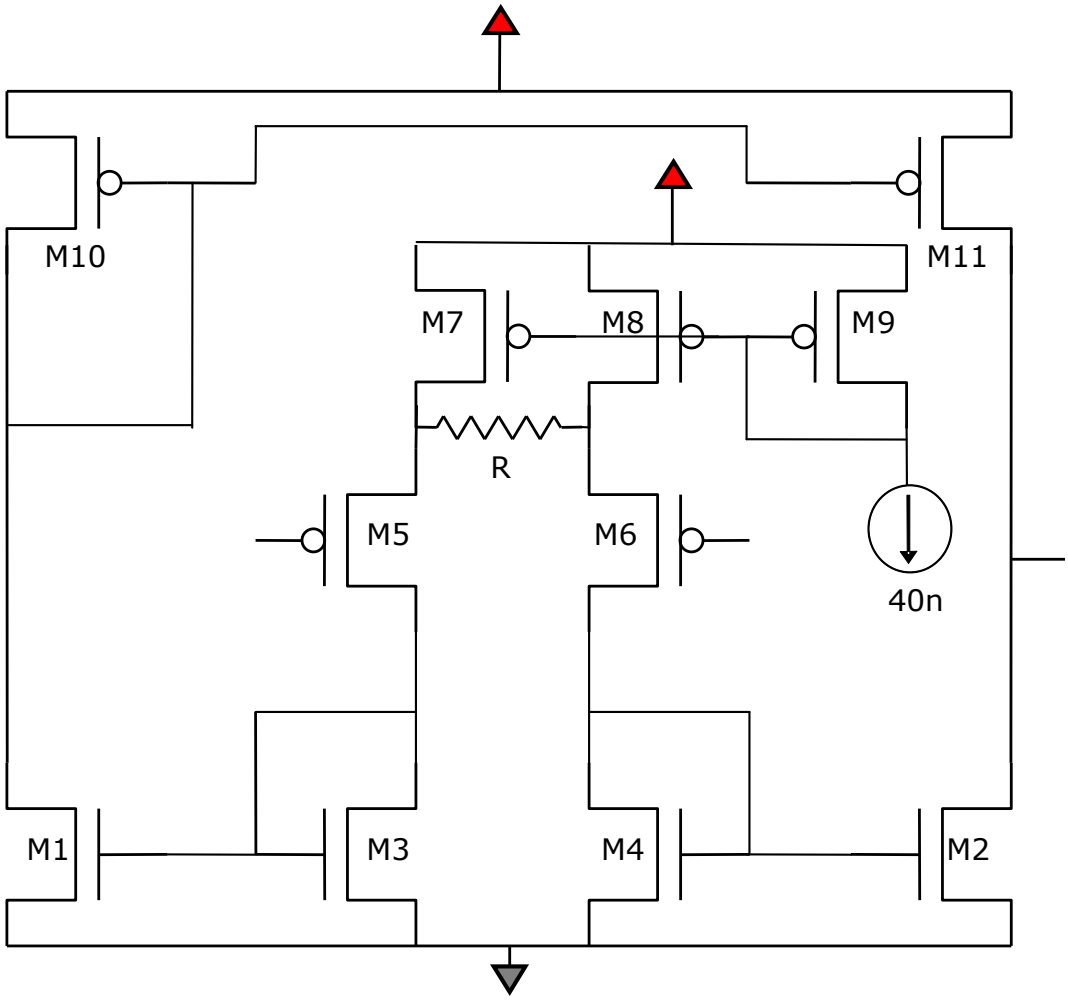


Figure 3.7. Schematic of Gm2 and Gm3. Specifications of transistors M1:M11 are shown in Table 3.3 for Gm2 and in Table 3.4 for Gm3.

Table 3.3

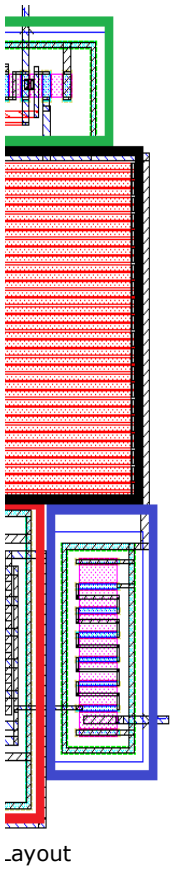
	Type	W-L(µm)
M_1:M_2	NMOS	24-10
M_3:M_4	NMOS	28-10
M_5:M_6	PMOS	2-120
M_7:M_8	PMOS	4-30
M_9	PMOS	8-30
M_{10}:M_{11}	PMOS	2-100
R	POLYH	7MΩ

Table 3.4

	Type	W-L(µm)
M_1:M_2	NMOS	4-80
M_3:M_4	NMOS	28-10
M_5:M_6	PMOS	2-120
M_7:M_8	PMOS	4-30
M_9	PMOS	8-30
M_{10}:M_{11}	PMOS	2-100
R	POLYH	7MΩ

3.3.1 Layout

Figure 3.8 and Figure 3.9 present both Gm's layouts. Figure 3.8 corresponds to Gm_2 and Figure 3.9 to Gm_3. Both layouts have the same topology due to the similarity of the design. In the bottom center part of the image both NMOS mirror were situated (red rectangle). The two mirrors stand between the PMOS mirror that bias the input pair (blue rectangle). In the center part of the figure, the resistor (black rectangle) and the input pair (orange rectangle)were presented. At the top part of the image, the remaining PMOS mirror can be seen (green rectangle).



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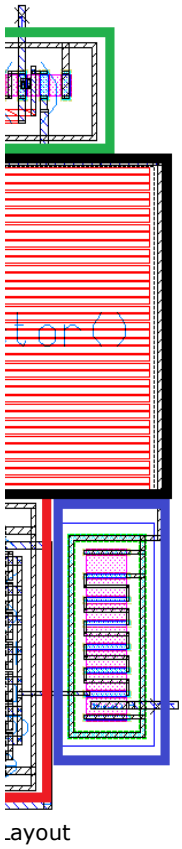

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3.3.2 Simulations

A simulation was carried out for each Gm to verify its value and to check the linear range of the circuit. Figure 3.9 and Figure 3.10 shows the output current of the Gm. Figure 3.9 corresponds to Gm_2 and Figure 3.10 to Gm_3. The slope in Figure 3.9 is 80nS and the linear range reaches 500mV. The slope in Figure 3.10 is 1.6nS and the linear range reaches 500mV. The offset of Gm_2 was also simulated and it reached 3.6mV.

A 5% variation is expected (simulation based) while varying the transistor model between the manufacturer's given corners. This spread is however compensated because the gain depends on a ratio between transconductances. Note that very similar transistor parameters are expected inside a single IC, thus the transconductances are expected to be proportional with a high degree of accuracy.

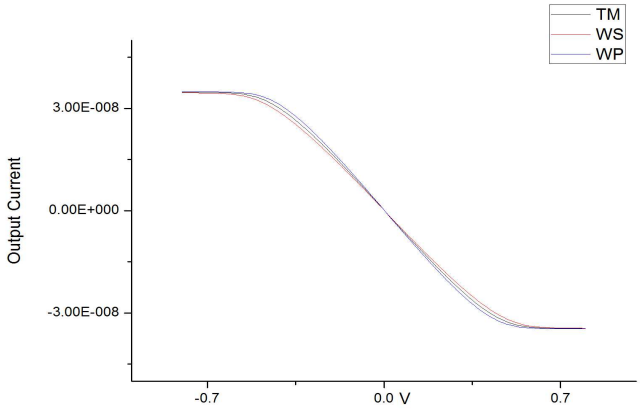


Figure 3.9. Gm_2Output Current

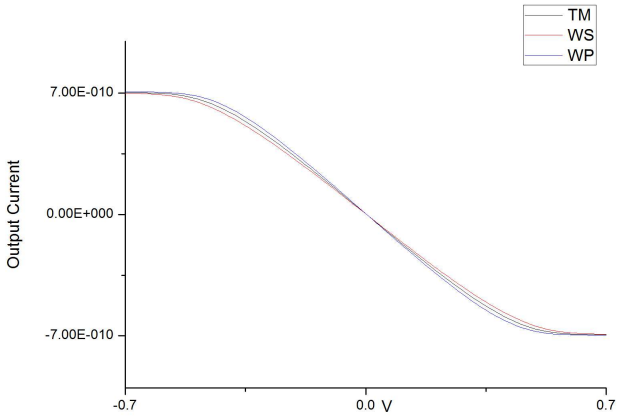
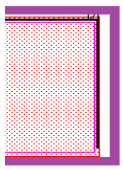


Figure 3.10. Gm_3Output Current

3.4 The Complete filter

After checking each OTA , the complete GmC circuit was simulated. In this section various simulations and the complete layout are presented.

3.4.1 Layout



In the left part of the Figure the Double GmC is presented (red rectangle). In the top centre part C_1 can be seen (blue rectangle). In the upper right part, Gm_2 (green rectangle) is presented and under it, Gm_3 (yellow rectangle). The remaining item is C_2 (purple rectangle). Total area: 0.71mm^2.

3.4.2 Simulations

The complete GmC filter was simulated using as input the preamplifier's differential output. The first aspect that was simulated was the Gain and the positions of the cut off frequencies. Figure 3.11 points out the simulated AC transfer function of the complete band pass filter for TM.

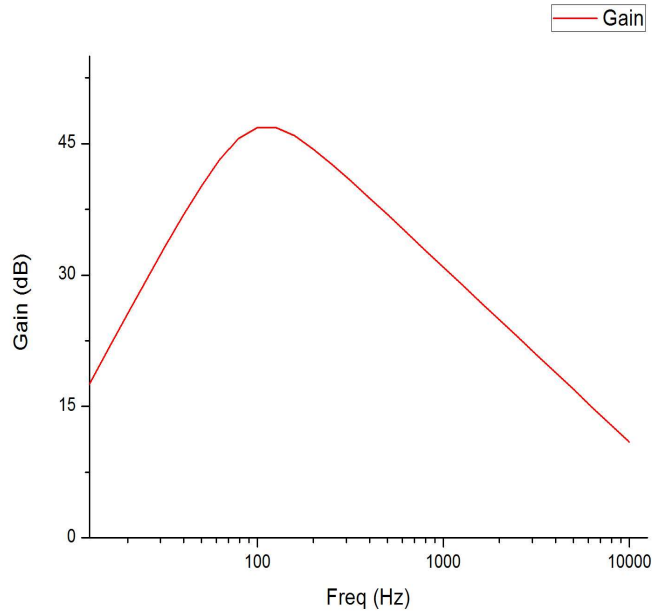


Figure 3.11. AC transfer function (TM)

In Figure 3.12 another AC transfer function is presented. In this case the simulations results of the variation of the transistor's models (TM, WS, WP), the resistors and the capacitors values within the range provided by the manufacturer.

As it can be seen in the image, only a 0.42dB gain difference, a 6Hz difference in pole1 and a 13Hz difference in pole2 are observed between the worst case curves. In Table 3.5 the different results are detailed.

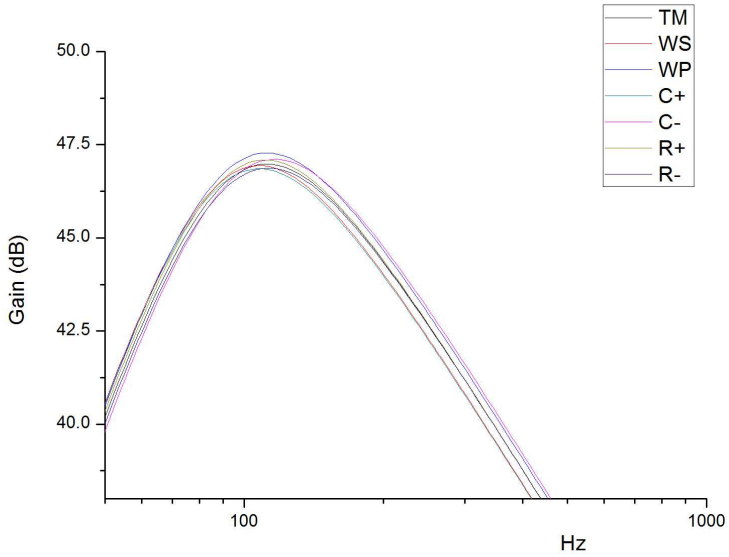


Figure 3.12. AC simulation varying several parameters.

Table 3.5

	TM	WS	WP	C+	C-	R+	R-
Gain(dB)	46.97	46.91	47.28	46.82	47.12	47	46.86
Low Pole(Hz)	67	64	67	65	70	66	67
High Pole(Hz)	212	203	210	204	216	209	213

Figure 3.13 shows the response to the Tokyo Test Signal (positive-negative) with amplitude 1mV.

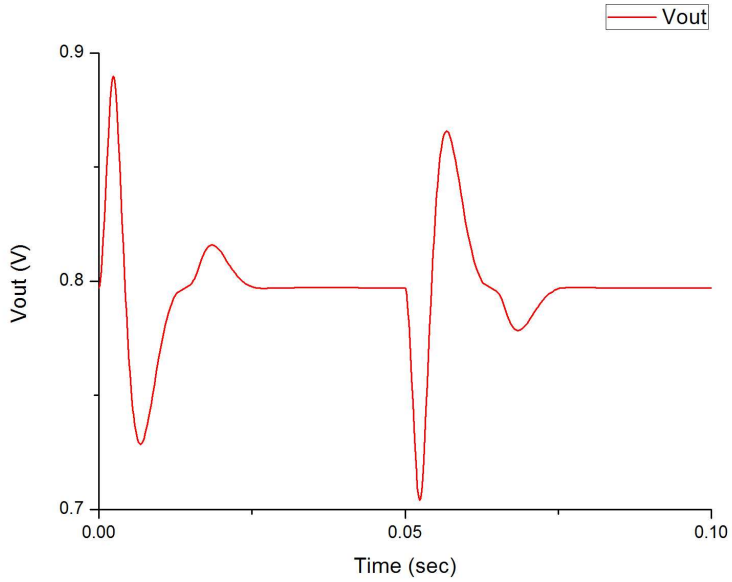


Figure 3.13. Transient response for a Tokyo signal with amplitude A=1mV.

A different transient analysis was conducted. In this case the simulations results of the variation of the transistor's models (TM, WS, WP), the resistors and the capacitors values within the range provided by the manufacturer. Only the positive signal is presented in order to distinguish more easily the differences between the graphs. Figure 3.14 shows these results.

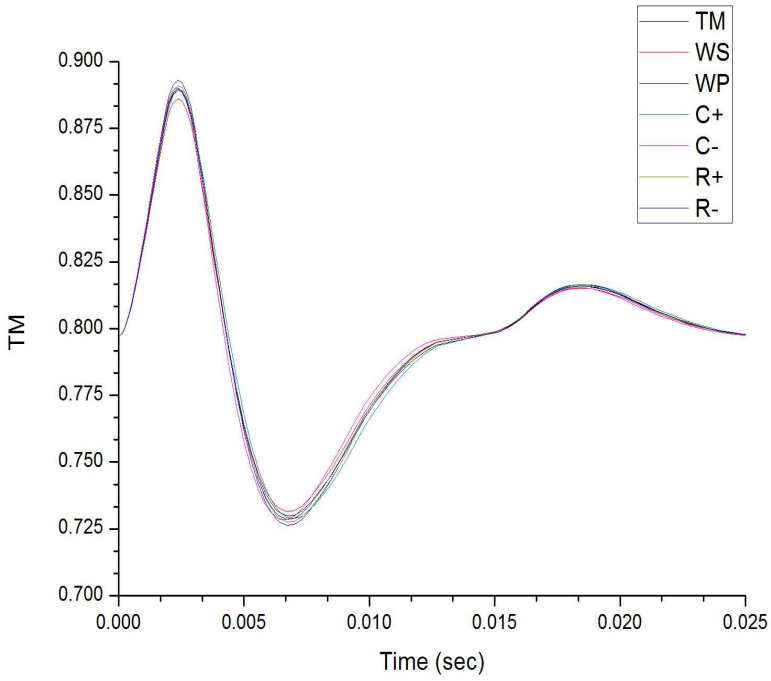


Figure 3.14 Transient simulation varying parameters. Input's amplitude:1mV.

The difference between the worst cases gain is just 7(Magnitude). In Table 3.6 the different results are detailed.

Table 3.6

	TM	WS	WP	C+	C-	R+	R-
Gain(Mag)	94	90	97	93	94	95	93

Figure 3.15 presents an analysis concerning the input amplitude. It shows the relation between input amplitudes from 200μV to 8mV (typical atrial signals amplitude) and the output peak voltage; each point in Fig.3.15 corresponds to a single transient simulation. The output has a high degree of linearity with the input.

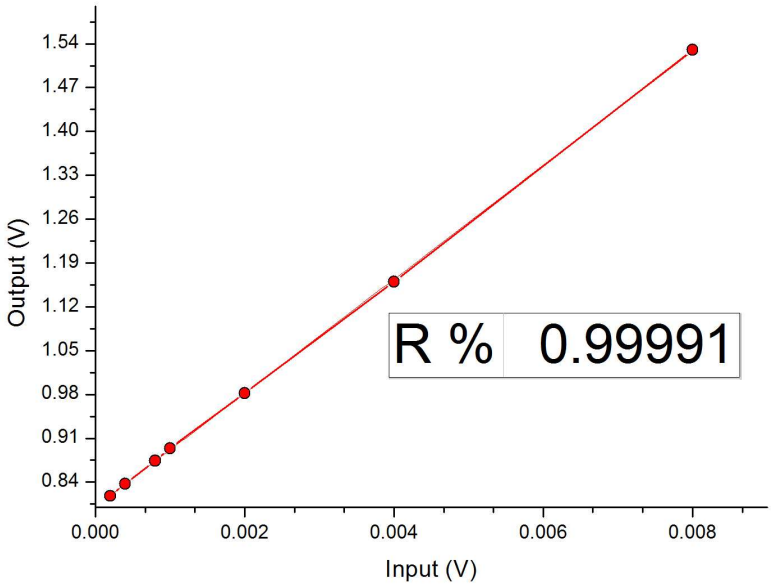


Figure 3.15. Output amplitude, when an input (Tokyo) signal is applied. Note the high degree of linearity.

Although the designed filter is likely to be close enough to the typical curve, if still necessary to tune the circuit at the GmC level, it can be easily adjusted by varying the global reference current of the OTAs (the global reference is a current copied with different weights to bias al the OTAs). In effect, Figure 3.16 shows the peak response of Figure 3.14 by varying the global reference current. The result is a monotonic gain increase. Thus to make the filter compliant with the standards it is necessary to adjust a single parameter.

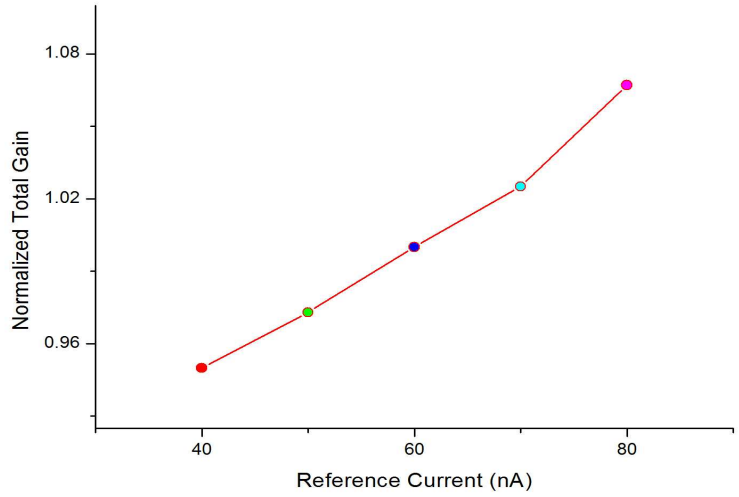


Figure 3.16 Peak response to current variation

Chapter 4: Comparator and full wave precision rectifier

The final elements of the cardiac sensing channel are the comparator and the full wave precision rectifier.

The reasons the rectifier was included in the channel design are the following:

- As the cardiac signal may be either positive or negative, two different comparators were required. One for each possibility.

- Because of the previous point, also two DACs were going to be needed. One for each comparator.

Since both positive/negative trigger level are the same in a cardiac sensing channel, another possibility was to use a full wave precision rectifier between the GmC filter and the comparator.

This section presents the design and simulations results of both the comparator and the rectifier designs. Figure 4.1 presents the block diagram of the final stage.

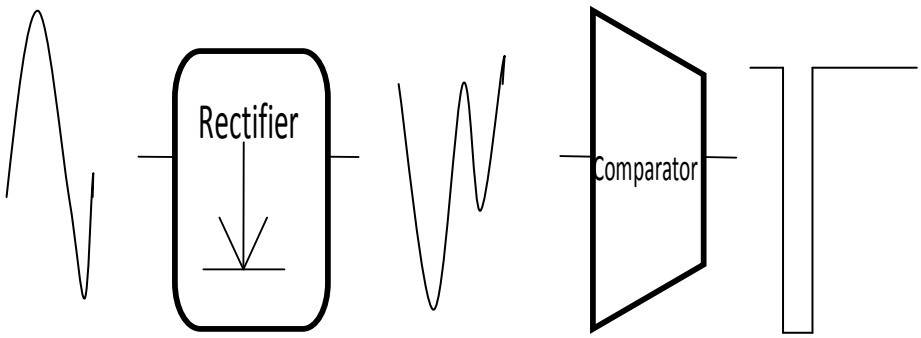


Figure 4.1. Final stage block diagram.

4.1 Comparator

Figure 4.2 shows the schematic of the comparator. The topology includes a simple OTA and three inverters. This topology was already developed and tested by the research group.

When the voltage difference at the input pair is positive, the current at the OTA's output increases and the voltage goes up. The two inverters attached to the OTA's output were included to make the slope output greater when there is a change at the input. The resistor's mission is to decrease the effect of the current peaks when the inverters are changing its state. The circuit has a current consumption of 60nA.

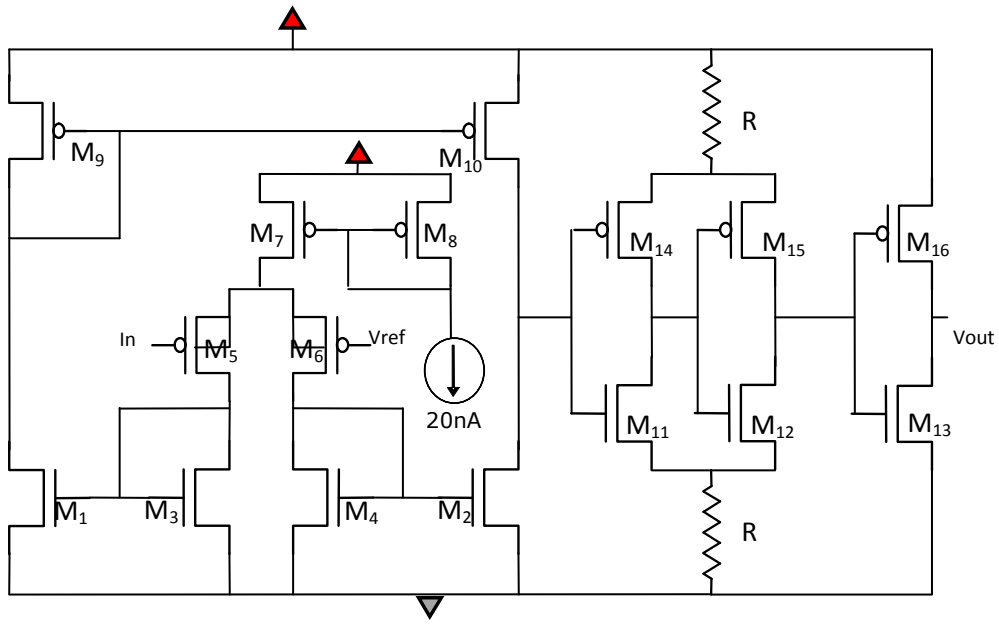


Figure 4.2 Comparator's Schematic.
Specifications of transistors M1:M16 and R are shown in Table 4.1(b).
Comparator's Specifications in Table 4.1(a).

Table 4.1(a)

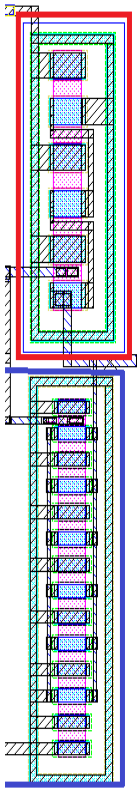
	Value
Supply Voltage	1.8-5V
Response	220µsec
Offset	2.23mV

Table 4.1(b)

	Type	W-L(µm)
M_1:M_2	NMOS	24-10
M_3:M_4	NMOS	28-10
M_5:M_6	PMOS	2-120
M_7	PMOS	4-30
M_8	PMOS	8-30
M_9:M_{10}	PMOS	2-100
M_{11}:M_{13}	NMOS	24-10
M_{14}:M_{16}	PMOS	8-30
R	POLYH	100kΩ

4.1.1 Layout

Figure 4.4 shows the comparator's layout. From right to left the different elements are presented: The output inverter (red rectangle), the remaining two inverters (blue rectangle), the two resistors (green rectangle), one of the PMOS of the input pair (yellow rectangle) at the bottom and the mirror that bias the input pair at the top (purple rectangle), both NMOS mirrors at the bottom (orange rectangle) and the PMOS mirror at the top (pink rectangle) and finally the other PMOS of the input pair (yellow rectangle). Total area: 0.078mm^2.



4.1.2 Simulations

In the case of the comparator a simulation was carried out. The only aspect that was needed to check was the correct operation of the system when the input voltage went under or over the reference voltage. Figure 4.3 shows the simulation's result. The reference voltage was set to 0.8V.

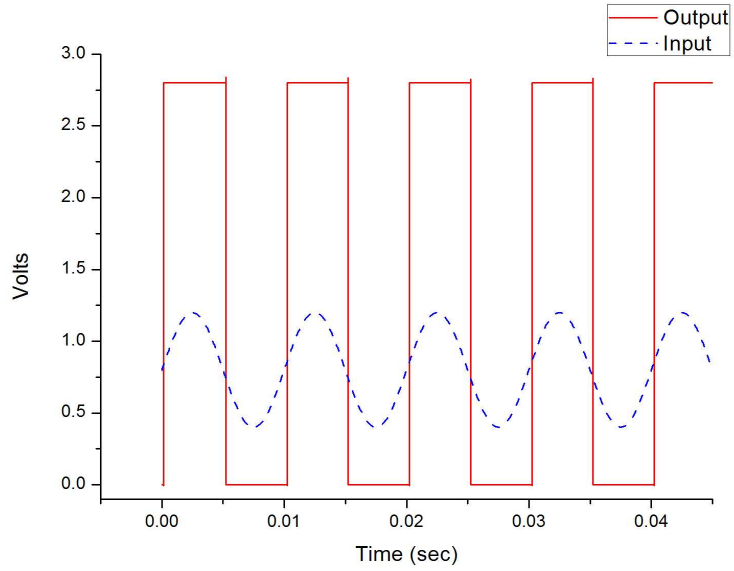


Figure 4.3. Output for a Sine input

4.2 Full wave precision rectifier

A new design was developed for a full wave precision rectifier. Figure 4.5(a) presents the proposed design scheme.

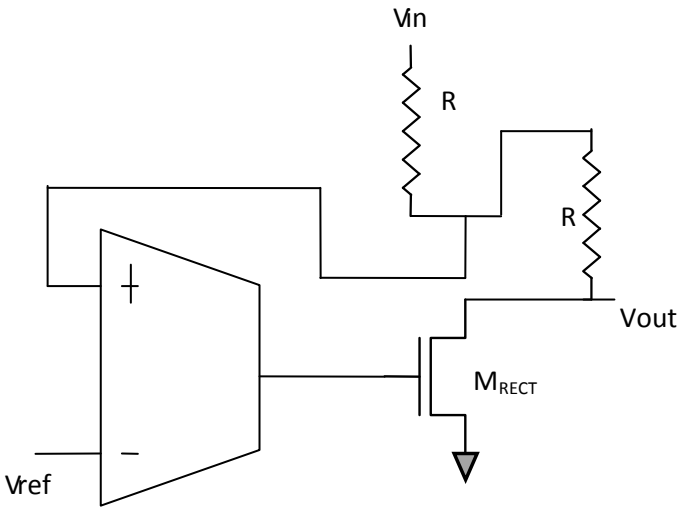


Figure 4.5(a). Full wave precision rectifier's schematic. The OTA's schematic is shown in Figure 4.5(b). All MOS specifications are shown in Table 4.2

When $V_{in} < V_{ref}$, the transistor is cut-off. Because of this, $I = 0$. In consequence: $V_{out} = V_{in}$.

In the case that $V_{in} > V_{ref}$ the NMOS transistor conducts. Therefore, a feedback loop is established and $V_+ = V_-$. As both resistors have the same value: $V_{out} = V_{ref} - (V_{in} - V_{ref})$.

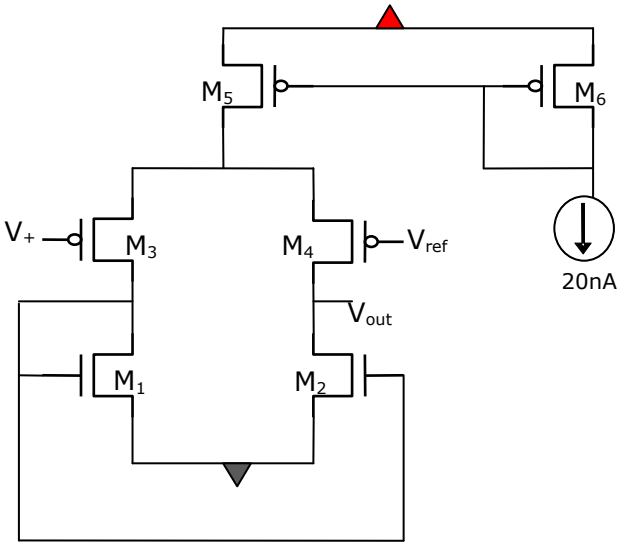


Figure 4.5(b). OTA's Schematic.

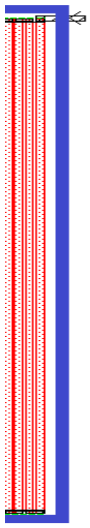
Table 4.2

	Type	W-L(µm)
M_1:M_2	NMOS	48-20
M_3:M_4	NMOS	3-100
M_5:M_6	PMOS	4-20
M_{Rect}	NMOS	8-120
R	POLYH	7MΩ

M_1 and M_2 were designed with big areas so as to minimize the offset. The reason for the width and length of M_3 and M_4 are the same that M_1 and M_2. M_5 and M_6 were designed indistinctly. M_{RECT} must behave as a virtual resistance. R needed to be as big as possible to reduce current consumption, and the 7MΩ value was selected because we have already design some others with the CAD that had the same value.

4.2.1 Layout

Figure 4.7 shows the layout of the full wave precision rectifier. In the right part of the image both resistors are presented (blue rectangle) and in the bottom, the NMOS output transistor (red rectangle). From the centre to the left, the OTA was drawn (green rectangle). Total area: 0.11mm^2.



4.2.2 Simulations

A simulation was carried out to check the circuit performance. Figure 4.6 presents the simulation's result. The reference voltage was set to 0.8V.

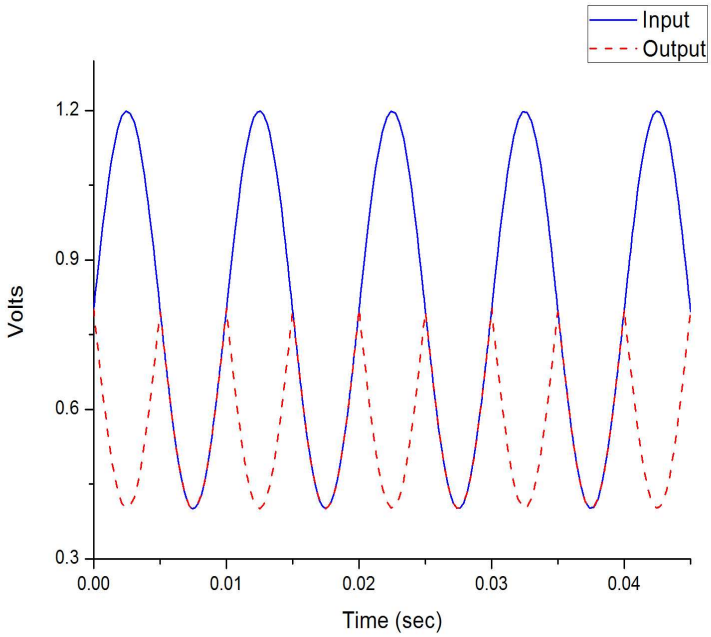
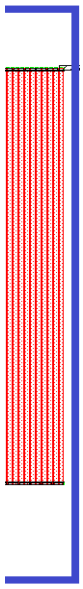


Figure 4.6. Output for a sine input

4.3 Full wave precision rectifier + Comparator

Figure 4.9 shows the layout consisted of the two elements. In the right part of the image the rectifier can be distinguished (blue rectangle) and in the left part the comparator (red rectangle). Total area: 0.20mm^2.



After checking each element's operation, it was time to check that both elements also worked correctly together. A simple simulation was carried out. This simulation includes the parasitic effects of the layout design. Figure 4.8 presents the analysis results.

Chapter 5: Conclusions

5.1 Complete System Operation

The complete sensing channel operation was verified by means of simulations. A typical signal detection is shown in Figure 5.1.

Figure 5.1(a) shows the preamplifier's output; Figure 5.1(b) presents the G_mC's output, Figure 5.1(c) presents the rectifier's output and Figure 5.1(d) the system's output. The input signal was a positive-negative Tokyo signal with amplitude of 1mV. The reference voltage of the rectifier was set to 0.8V and the reference voltage of the comparator was set to 0.73V.

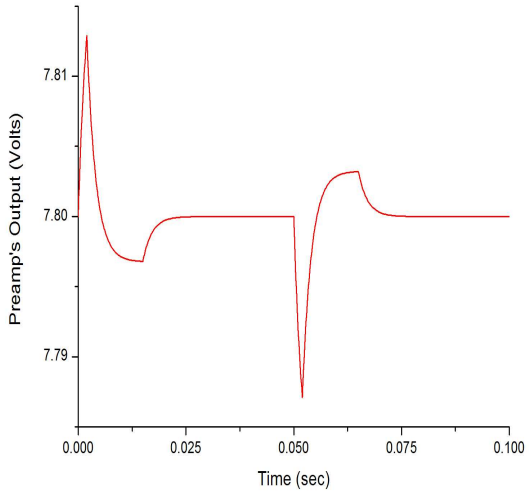


Figure 5.1 (a).

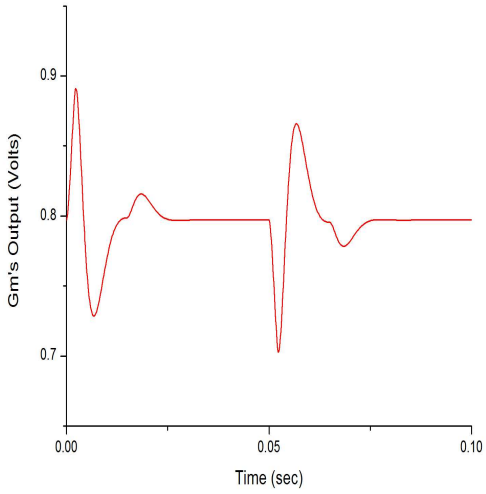


Figure 5.1 (b).

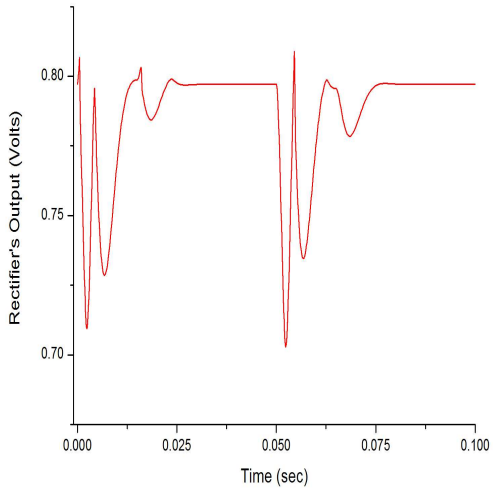


Figure 5.1 (c).

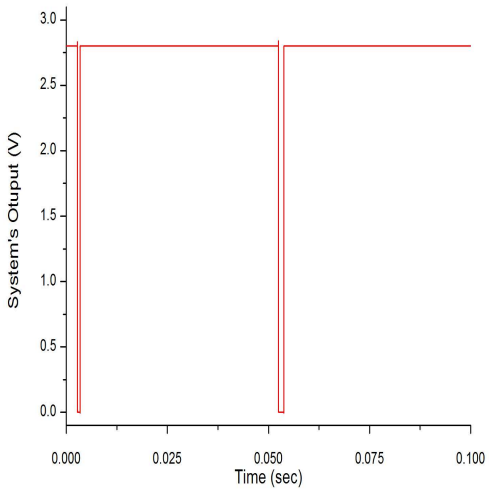


Figure 5.1 (d).

5.1.1 PADS

In order to connect the whole circuit to the chip legs, several pads were used. Within these PADS, two different topologies were used. One for the high voltage inputs and another for the low voltage ones. The first one was already described in chapter 2. The second design is shown in Figure 5.2.

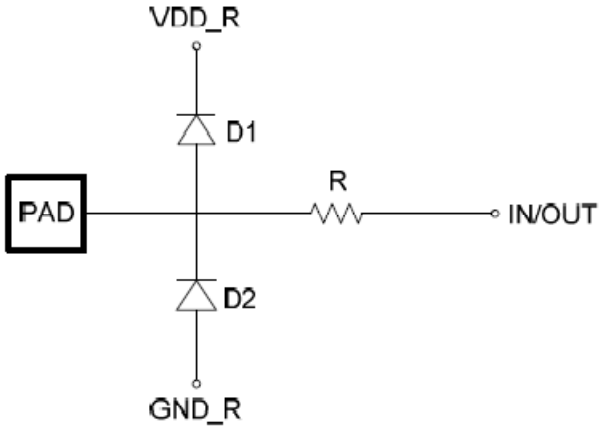


Figure 5.2. Low voltage PAD.

Table 5.1 details the PADS that were used for the complete system. Table 5.2 presents the specifications of the complete system.

Table 5.1

PAD (Type)	Comments
V_+ (HV)	Positive differential system's input.
V_- (HV)	Negative differential system's input.
V_r (HV)	Reference voltage used by the OTA inside the preamplifier to set the common feedback voltage V_c.
V_{DDH} (HV)	High Voltage supply.
I_p (HV)	Polarization current used by the current distributor.
V_{DDL} (LV)	Low Voltage supply.
GND(LV)	Ground.
V_C(LV)	Common voltage for GmC.
V_{RR}(LV)	References voltage for rectifier.
V_{RC}(LV)	Reference voltage for comparator.
V_{out}(LV)	System's output.

Table 5.2

	Value
Supply Voltage	2.8-8V
C. Consumption	740nA
C. Off Frequency(1)	67Hz
C. Off Frequency(1)	212Hz
Gain	47dB
Area	2.0mm^2

5.2 Conclusions

In this work the design of a fully integrated sensing channel for cardiac pacemakers has been presented, including a few innovative circuit techniques. A study to determine the accuracy of the transfer function has been presented, to determine the strategy to include this fully integrated but untrimmed circuit in a real medical device. The circuit has been designed in XC06, a 0.6μm CMOS technology with HV capabilities from Xfab (www.xfab.com), and it is scheduled for fabrication in September's MPW run. This is possible because the found granted by Fondo María Viñas, "PR_FMV_2009_1_3224 - Integrated circuit for cardiac sensing".

A sensing channel continuously monitors natural cardiac activity, an electrical signal ranging from approximately 200μV to 15mV peak amplitude, and triggers a pulse to a microcontroller when the signal passes a programmed reference voltage level. The sensing channel is composed of a continuous time preamplifier at the input, a GmC filter and gain stage in the middle, and a rectifier and comparator at the output. The rectifier is included to compare with a negative/positive reference with a single comparator at the output.

Apart from the accuracy study in the transfer function of the filter, the main original contribution of this work is the use of a novel nano power rectifier topology, and the development of a preamplifier that exploits HV transistors to avoid the use of safety capacitors. Finally it should be mentioned that most of the design (most transistors operate in deep weak inversion) was carried with LT-Spice [16], a free CAD tool. BSIM foundry models were adapted without major problems.

A completely integrated 25db gain high pass preamplifier, with only 4.5µ $Vrms$ input referred noise, and 600nW power consumption was designed and simulated .Due to the low bias current and the use of HV and isolated input transistors, the preamplifier does not necessarily require the use of decoupling capacitors. Although a specific safety analysis must be completed on each circuit specially taking into account the bias voltage of the electrodes when sensing, the proposed technique enables to remove all external decoupling capacitors.

A continuous time GmC filter is the second stage in the sensing channel. The filter provides 22db gain in the band from 70 to 200Hz (together with the preamp). The proposed filter can withstand input signals with a high common mode input up to 15V. Fully integrated GmC circuits offer an excellent power consumption option but on the other hand the transfer function may present a certain variation from one chip to another (or from one fabrication batch to another). A detailed study was conducted to investigate the accuracy of the filter, particularly to determine if the response to a Tokyo test signal has the required precision without the aid of tuning or trimming.

Simulations show an excellent linearity for the filter, and only in a very worst case the circuit response may not be within the 5% barrier. The circuit will be fabricated to test the transfer function at least in a single fabrication batch. If still necessary for a real application to tune the filter it can be done by just changing a single parameter: the global reference current of the OTAs.

A novel micropower, full wave precision rectifier for a cardiac sensing channel was developed (not yet fabricated). Simulations show that the circuit works correctly. This element will also be fabricated apart from the entire channel so as to enable independent testing. It should be pointed that the realization of micro power integrated precision rectifiers is a challenging task because most manufacturers do not allow to include floating diodes (to avoid latch up) in the Ics. Even taking into account that micro-ampere range current would hardly trigger a latch up event, traditional full-wave precision rectifiers include apart from several resistors, two opamps that greatly increase power consumption. Most reported integrated, micropower, rectifiers include a comparator that changes the structure of a buffer/amplifier to inverting or non-inverting depending

on the input sign. An example is the patent in [18], or the previous work in [17].

Finally, a 200nW power comparator was developed (based on a previous design at μDIE).

5.3 Publications

The results of this work were presented in two different conferences papers:

- "A Fully Integrated Amplifier for Cardiac Sensing in a HV – CMOS Technology" – Jose Lasa, Alfredo Arnaud, Matías Miguez – EMBC 2010 – Buenos Aires, Argentina..

- "Reliable ultra low power GmC filters for medical devices" – Jose Lasa, Alfredo Arnaud, Matías Miguez, Joel Gak – SBCCI 2011 – João Pessoa, Brazil.

5.4 Future work

Some aspects that may be considered to improve future versions of this system are:

- Improve the preamplifier's design so as to reduce the capacitors and the resistor's value and as a consequence reduce the area.

- Redesign of the double Gm at the second stage to reduce the bias current from 80nA to at least 40nA. A preliminary analysis indicates it is possible while keeping the same circuit performance.

- To include an auto-zero technique for the comparator and rectifier stage, to further enhance overall circuit precision.

Future work on this circuit includes precise noise measurements, and intracavital ECG signal recording capability.

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