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**Integrated switches for  
implantable medical devices,  
in HV-MOS technology**

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## **Safety note:**

**Medical device manufacturer, that employs any of the designed switches on this document, shall guarantee that when not stimulating all the electrodes are either in high impedance, or connected to GND. GND shall be the common mode voltage for biological tissue.**

## Abbreviations

The following abbreviations were used along this document.

UCU, Universidad Católica del Uruguay.

FIT, Facultad de Ingeniería y Tecnologías.

CMOS, complementary metal-oxide-semiconductor.

SIO, Silicon on insulator.

MOS, metal-oxide-semiconductor.

CCC, Centro de Construcción de Cardioestimuladores del Uruguay.

ESD, electro static discharge.

DIE, Departamento de Ingeniería Eléctrica, FIT-UCU.

$\mu$ DIE, grupo de microelectrónica de la UCU.

HV, high voltage.

ASIC, application specific integrated circuit.

LV, low voltage.

EMI, electro magnetic interference.

PHV, PMOS high voltage.

NHV, NMOS high voltage.

TG, transmission gate.

## Resumen

Los dispositivos médicos implantables se utilizan en el tratamiento de un número cada vez mayor de patologías. La microelectrónica es una herramienta esencial en el desarrollo de los mismos. Un aspecto importante del diseño, son los circuitos que controlan los estímulos eléctricos hacia el tejido biológico.

En este trabajo se diseñó, fabricó, midió, y comparó, tres tipos de llaves (Llave A, B y C) integradas, capaces de dejar pasar o cortar estímulos tanto en tensión (100mV-16V) como en corriente (100 $\mu$ A-30mA). Los circuitos fueron fabricados en una tecnología CMOS de alto voltaje sobre un waffer de SOI (XT06 de Xfab) [3].

Las especificaciones para las llaves fueron obtenidas en conjunto con la empresa CCC del Uruguay [12], acorde a su experiencia en la ingeniería de dispositivos médicos implantables. El objetivo es cumplir con un amplio espectro de posibles aplicaciones, para servir de llave de estímulo de uso genérico en prototipos y pequeñas series de dispositivos innovadores para diversas terapias. Las llaves diseñadas incluyen transistores de paso MOS de gran tamaño, y una compleja circuitería para el manejo de la conmutación y adaptación de los niveles de voltaje. Deben cumplir con las siguientes especificaciones:

1. Impedancia menor a 5 $\Omega$ , cuando están conduciendo.
2. Tensión de alimentación  $V_{CC}$  entre 2v y 5V para los circuitos lógicos y drivers.
3. Consumo estático despreciable (máximo decenas de nA).
4. Corrientes de fugas despreciables (debajo de 20nA).
5. Tiempo de cierre y apertura menor a 1 $\mu$ s.
6. Capacidad de conmutar estímulos en tensión, desde 100mV hasta 16V
7. Estímulos en corriente, desde 100 $\mu$ A hasta 30mA
8. Llave completamente simétrica, esto significa que los nodos de entrada/salida ( $V_{IN}$  ,  $V_{OUT}$ ) pueden ser intercambiables y las llaves deben funcionar sin degradar su performance.
9. Frente a una falla simple (por ejemplo ruptura de un GATE), no entregar corriente continua a tejido o en caso de hacerlo que no supere unos pocos  $\mu$ A ya que se puede poner en riesgo al paciente.
10. Minimizar Crosstalk, esto es los picos de corriente parásitos a través de la llave cuando está abierta, pero la salida cambia abruptamente de potencial. Idealmente no debería entrar corriente a la llave, sin embargo no es posible hacer una llave libre de crosstalk debido a capacidades parásitas, este efecto debe ser el mínimo posible.
11. Inyección de carga hacia la carga cuando se abre y se cierra la llave debe ser la mínima posible.
12. Protección contra descarga electrostática (ESD).

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Las medidas realizadas, muestran que se cumplió de forma satisfactoria con estas especificaciones.

## Abstract

Implantable medical devices are being used in the treatment of a growing number of pathologies. Microelectronics is an essential tool for the development of these devices especially novel applications. An important aspect of the design, is the capability of controlling electrical stimuli delivered to biological tissue.

In this work, three different integrated switches (Switch A, B and C) were designed, fabricated, measured and compared, to control either voltage (100mV-16V), or current (100 $\mu$ A-30mA), stimuli. The circuits were fabricated in a high voltage CMOS technology over a SOI wafer (XT06 from XFAB) [3].

For this research, the specifications were determined with the aid of CCC-Uruguay [12], because of their experience in the engineering of implantable medical devices. The objective is to be able to use the designed switches in a wide spectrum of devices, either at prototype level, or in small production batches. The designed switches are composed of large size MOS pass transistors and a complex circuitry for MOS gates control and voltage level adaptation. The switches shall comply with the following specifications:

1. On resistance below 5 $\Omega$ .
2. Power supply  $V_{CC}$  from 2V to 5V for logic circuits and drivers.
3. Negligible static power consumption (few tens nA maximum).
4. Negligible leakage currents (below 20 nA at any pin).
5. On/Off time below 1 $\mu$ s.
6. Support voltage stimuli from 100mV to 16V.
7. Support current stimuli from 10 $\mu$ A to 30mA.
8. The switches must be symmetrical, that means the input/output ( $V_{IN} - V_{OUT}$ ) pins can be exchanged at any circuit configuration and the switch must operate with no further changes or significant performance degradation.
9. Safety, the failure of a single circuit element (for example a punctured MOS gate) must not cause a DC current flow through to the electrodes in contact with the tissue, larger than a few micro-amperes because otherwise it may be a risk for the patient.
10. Crosstalk shall be the minimum possible: when the switch is off, in the case of a voltage pulse in the output, ideally no current peaks flow into the switch. Although it is not possible to develop a crosstalk-free device because of the parasitic capacitance in the output node, the effect shall be the minimum possible.
11. Charge injection to the load when the switch is turned on or off, shall be the minimum possible.
12. Electro static discharge (ESD) protection shall be included on every circuit pin.

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A rough conclusion after fabrication and measurements, is that all specifications were met without a major deviation.

## **Agradecimientos**

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Familia y amigos.

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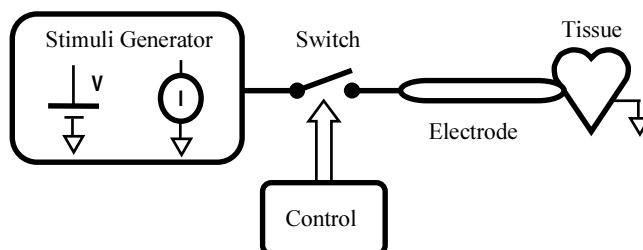
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## 1 Introduction

Most implantable medical devices are electrical stimulation systems, that deliver either current or voltage pulses to the patient according to different requirements. Microelectronics technology steadily contributes to the development of such devices. Stimuli section of the circuit may consist of the basic elements shown in Figure 1.1, a stimuli generator (either a voltage or current source), electrodes connecting the tissue to the device, a switch that toggles the electrical connection of the electrodes and a control block that decides when and for how long a stimulus shall be applied. Stimulation can be either a voltage applied to the tissue from a few hundreds mV to well over 10 V, or a current forced through it ranging from a few tens of  $\mu\text{A}$  to tens of mA. Although at a glance it appears simple, in this work we will focus in a circuit to implement the switch of Figure 1.1. A 0.6 microns high voltage (HV) technology on a p-type SOI wafer with insulator trenches capability was selected (XT06 from XFAB), first to enable stimulation up to 16 Volts, while insulating characteristics allowed the design of a safety compliant circuit in a wide range of connection schemes. Different medium and high voltage, fully isolated transistors can be fabricated with maximum ratings between 8V and up to 60V  $V_{\text{DS}}$ . Because of trench isolation, floating diodes can also be fabricated.



**Figure 1.1. Typical stimuli section of an implantable medical device.**

## 1.1 Background, motivation and goals.

The microelectronics research group (from now on  $\mu$ DIE – <http://die.ucu.edu.uy/microdie>) at the Electrical Engineering Department Universidad Católica del Uruguay (UCU) is dedicated to the research and development of application specific integrated circuits (ASICs), with emphasis on analog and mixed mode "full custom" design in CMOS technology. Low voltage and micropower applications for implantable medical devices are a main research area. In recent years the  $\mu$ DIE has designed and fabricated six ASICs, containing different research & development circuits aimed to be part of implantable medical devices. The circuits were fabricated in 0.35 $\mu$ m, 0.35 $\mu$ m-HV, 0.6 $\mu$ m-HV and 1.5 $\mu$ m CMOS technologies and include ultra low-noise amplifiers [13],  $G_m$ -C filters [14], DC-DC converters [15] and several test structures for transistor modeling.

This work is part of a first cooperation project with Centro de Construcción de Cardioestimuladores del Uruguay (CCC) [12], with the objective to receive some feedback from the medical device industry and to focus the research activities at  $\mu$ DIE towards the needs of real novel implantable electronics under development. CCC helped with the specifications for the circuit and provided us helpful suggestion during the design process.

Another main objective of this work was to gain expertise on HV technology. Our research group currently has a strong interest in HV due to its relevance for implantable electronics, but also because HV will be probably required in the development of ASICs to incorporate microelectronics technology in several cases studied for the national industry (most cases are front-ends involving relatively large voltages). This work allowed the fabrication of the first research ASIC on HV technology at  $\mu$ DIE and because of the challenging design, it required the use of the full features available in HV. At present, two more circuits are being fabricated in HV (XT06, XC06) [3].

This thesis work included the design and test measurements of integrated circuits designed at Departamento de Ingeniería Eléctrica (DIE). The CAD tool employed was Mentor Graphics using a University license through the Mentor-HEP program [16]. Laboratory measurements required only standard instruments like precision multimeters, oscilloscope, voltage sources and function generator.

Although this work prime objective is research, it allowed a rich exchange of ideas with the industry. It is our hope that the designed circuits and the acquired knowledge, may contribute to the development of valuable and innovative products in the near future.

## 1.2 Microelectronics and medical implants

An electronic medical implant is defined as any type of medical device that incorporates electronic components and is used inside the body to achieve a physiological response. The first microelectronic medical implant was a heart pacemaker, which became a common device in the 1970s [17]. But many other implants are now in use, like hearing aids [18], neurostimulators [19], or implantable drug infusion pumps [20], among others. In recent years the use of implantable medical devices has increased and it is expected to continue rising [1]. Not only there has been an increase in the use of existing medical devices, but also new devices, like vision enhancers, are expected to be developed in a nearby future.

Medical devices used for treatment of different diseases have widely different requirements and specifications, nonetheless there are several characteristics shared by most of them.

1. Low power consumption: Changing or charging batteries can be inconvenient, difficult, costly and even risky for the patient; all implantable medical devices need to consume as little energy as possible [21].
2. High reliability: A failure of an implantable medical device can result on inconvenience, pain, damage or even death for the patient. Also maintenance is costly and risky [2].
3. Low voltage signals. Most of the natural signals inside a human body, as well as the output of the transducers, are in the  $\mu\text{V}$  or  $\text{mV}$  range which requires special care in sensing and amplifying [22][23].
4. Low frequencies: The natural frequency span of biological signals vary from a fraction of a hertz to several kilohertz.
5. Small Size: Implantable devices need to be as small as possible, so as to be less invasive to the human body [24]. This does not always means that silicon area should be as small as possible, because increasing silicon area to minimize external components can reduce overall size.
6. High voltage and/or current stimuli.

To fulfill the above needs, microelectronics becomes an essential tool for the development of implantable medical devices. This work deals with a generic circuit for electrical stimuli control, taking into account the above mentioned characteristics.

### *1.2.1 Safety requirements of implantable medical devices*

To guarantee safety requirements of implantable medical devices, is one of the most important issues on the design of an ASIC to ensure no harm is done to the patient. The two principal aspects to take into account are:

- **Reliability:** reliability stands for the probability of a failure to occur. Medical reliability means the frequency (probability) of a failure should be as low as possible. Thus several design practices will be adopted to enhance the reliability of the circuit.
- **Safety:** But even after ASIC test, it is not possible to guarantee that no failure will occur. A safe circuit means that the device does not cause harm to the patient, in case of a single circuit element failure (for example a punctured gate, a short circuit transistor).

The fail safe device does not exist, but if the probability of a single failure is low (high reliability) and considering failures as statistical independent events, the probability of two simultaneous failures can be considered virtually impossible [2][28][29]. Thus, the regular practice for implantable medical devices designers is to ensure that if a single failure occurs in the circuit, it does not cause harm to the patient. The kinds of potentially hazardous effects in an electronic device in direct contact with the human body, may vary with the application. For example in a pacemaker a failure must not result in an artificial pace rate above 200ppm. But for any circuit delivering stimuli like the one in this work, it is mandatory at least to comply with the following rule: any single failure (may be a punctured gate in a MOS transistor, Drain to Source short, etc.) must not cause a significant (for example larger than few  $\mu\text{A}$ ) DC current flow to the tissue. A DC current for example to the heart muscle may produce defibrillation, but any tissue constitution is damaged due to electrochemical phenomena in the case of DC current flow [28][29]. So DC current must be guaranteed to be virtually zero in the case of single failure, for any electrode driver, or electrode sensing circuit (either connected to nerves, muscles, etc.). While the regular practice is to include capacitors in series with the stimulating or sensing electrodes [25][26], in this project a capacitor in series cannot be assumed. Thus a more complex safety mechanism shall be implemented.

### 1.3 Design specifications, circuit PINs

The designed switches must comply with requirements of a wide spectrum of possible applications, in fact it was projected as a general purpose switch for prototypes and low volume series of novel implantable medical devices for several therapies. The designed switches include large MOS transistors to control the current flow and a complex circuitry to drive the transistors' gates.

An application example is shown in Figure 1.2, where the switch controls a voltage pulse to the load  $R_{Meas}$ . The following PINs are necessary:

- CTRL: (Digital Input) Opens and closes the switch. This pin is normally connected to a microcontroller that controls the switch.
- GND: Switch ground.
- $V_{CC}$ : Power supply, for digital and low voltage circuitry.
- $C_{ap}$ :  $C_1$  connection. This capacitor is part of an embedded charge pump that generates, if necessary, either a  $2V_{CC}$  voltage, or a negative voltage  $V_{SS} = (-V_{CC})$  to drive the main transistors gates to achieve the necessary  $5\Omega$  in the full range of stimuli voltages.
- $2V_{CC}/V_{SS}$ :  $2V_{CC}/V_{SS}$  Charge pump generated voltage.
- $V_{IN}$ : Switch input.
- $V_{OUT}$ : Switch output to tissue.
- $V_{High}$ : Reference voltage, it is normally connected to  $V_{IN}$ . It is a reference voltage for a protection circuit in switches B,C, to be discussed in chapter 3.

Note 1: if the charge pump operation is not necessary, Cap pin is not connected and  $2V_{CC}/V_{SS}$  shall be connected to  $V_{CC}/GND$ .

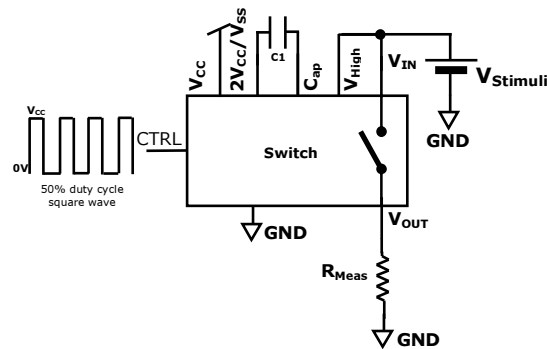
Note 2:  $V_{IN}$   $V_{OUT}$  can be exchanged

The switches shall verify the following specifications:

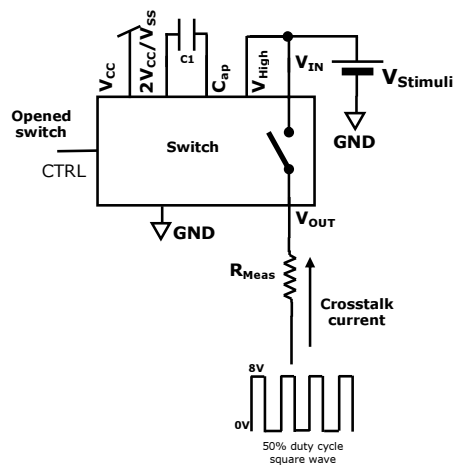
1. On resistance below  $5\Omega$ .
2. Power supply  $V_{CC}$  from 2V to 5V.
3. Negligible static power consumption (few tens nA maximum).
4. Negligible leakage currents (below 20 nA at any pin).
5. On/Off time below  $1\mu s$ .
6. Support voltage stimuli from 100mV to 16V.
7. Support current stimuli from  $10\mu A$  to 30mA.
8. Symmetrical, that is the  $V_{IN} - V_{OUT}$  pins can be exchanged in Figure 1.2 or any other connection scheme and the switch must operate with no further changes or significant performance degradation. To put it simple, the switch must block or allow current flow, in both directions.
9. Safety, the failure of a single circuit element (for example a punctured MOS gate) must not cause a DC current flow through to

the electrode larger than a few micro-amps, otherwise it may be a risk for the patient.

10. Crosstalk shall be the minimum possible: Crosstalk phenomenon is explained in Figure 1.3. In the case of a voltage pulse in the output, ideally no current peaks flow through the switch when opened. Although it is not possible to develop a crosstalk-free device because of the parasitic capacitance in the output node, the effect shall be minimized.
11. Charge injection to the load when the switch is turned on or off, shall be the minimum possible.
12. Electro static discharge (ESD) protection shall be included on every circuit pin.



**Figure 1.2 Voltage stimuli configuration. CTRL signal is provided by a microcontroller, high voltage stimuli are delivered to the tissue ( $R_{Meas}$ ).**



**Figure 1.3 Crosstalk phenomena: tissue voltage can abruptly change due to a stimulus through a different electrode, causing a parasitic current into the switch.**



## **1.4 Conclusions and Contents**

The design of ASICs, for implantable medical devices has both academic and industrial interest. However there is very little published work about the design of circuits to control voltage or current stimuli. This work deals with the design of integrated switches for electrical stimuli delivery to biological tissue, that must comply with a broad span of possible uses in implantable devices, combined with strict safety rules, ESD protection, low crosstalk, low charge injection and negligible leakages, among others, resulting in challenging specifications. A HV-CMOS over SOI wafer was chosen for the application (XT06 from XFAB).

Three different circuits will be developed for the task, named Switch A, Switch B and Switch C. Switch A is a large composite CMOS transmission gate to control stimuli and its driving circuitry. Switches B and C, are very similar, include a dual PMOS large composite transistor and its driving circuitry (there is only a slight difference in the driver circuit between Switches B and C.).

In the following chapter, the selected HV CMOS technology is presented as well as the design of the main transistors (the transmission gate of Switch A and the PMOS of Switches B and C). In chapter 3 the driving circuits and the complete design of the switches are presented, including simulations of the driving circuits. In chapter 4 measurement results are shown. In chapter 5 a comparison between the proposed circuits result is shown, as well as overall conclusions and future work. Mainly because of ESD performance, Switches B or C seems to be the first option for a real device. ESD considerations are presented in Annex A.

## 2 HV CMOS technology and the main MOS transistors

In this chapter the main HV technology characteristics are described, focusing on the employed MOS transistors. The designed switches are composite ones, composed of very large (very wide) transistors that let the current flow or not and a driving circuitry that controls the gate of these so called main transistors. At the end of the chapter the main transistors are designed while the driving circuitry and whole switch operation is described in the next chapter.

### 2.1 Introduction

In spite of the existence of several techniques for the use of standard CMOS technology with relatively high voltages [10][11], high voltage technology (HV) is preferred by medical equipment manufacturers because they strictly follow the integrated circuit (IC) manufacturer rules. Introducing new process layers, a HV CMOS technology allows the fabrication of devices that can support elevated voltages [5]. In this work the selected process is XT06, from Xfab [3], a 0.6 microns HV-MOS on SOI waffer. Regular 5V core CMOS can also be fabricated, as well as double poly capacitors and high-resistivity poly resistors in the target process. For example, in Figure 2.1 a HV NMOS transistor (named nhv) vertical cut is shown. Nhv has the usual structure of a HV transistor, incorporating a thick gate oxide that enables up to 18V  $V_{GS}$ ,  $V_{GB}$  and the drain diffusion is growth into a N-Well to complete a diffused Drain to support elevated  $V_{DS}$  voltages. To help the interpretation of the circuits in this work (different kind of HV, LV, transistors are used) the symbols used for each transistor are shown in Figure 2.2. HV transistors are not symmetrical, the drain which is designed to withstand the highest voltage, is marked with a double line.

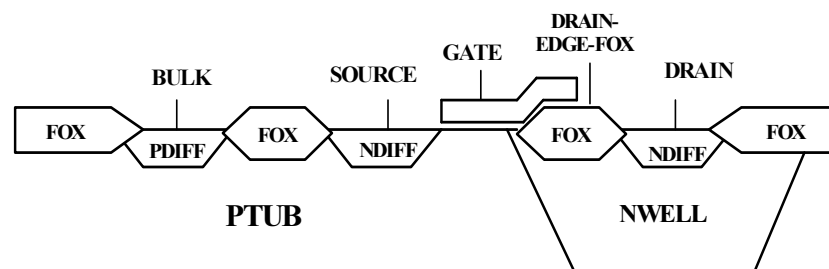
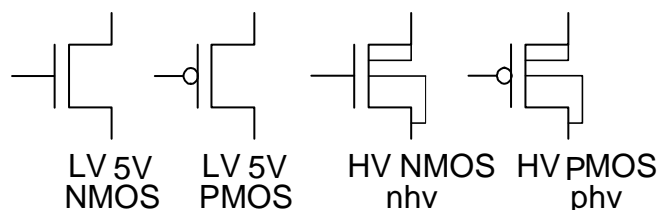


Figure 2.1 Vertical cut view of a typical HV NMOS (nhv)



**Figure 2.2 Symbols for the different kinds of transistors used in the circuits: LV NMOS and PMOS and HV NMOS (nhv) and PMOS (phv). LV transistors use thin oxide and withstand up to 5V  $V_{GS}$ . HV ones use a thick oxide to withstand up to 18V  $V_{GS}$  and up to 60V  $V_{DS}$  because of their diffused Drain.**

## 2.2 XT06

XT06 technology from XFAB [3] was selected for the ASIC, because apart of being HV, its unique isolation capability allowed the widest range of possible connection configurations without the risk of latchup, or safety problems.

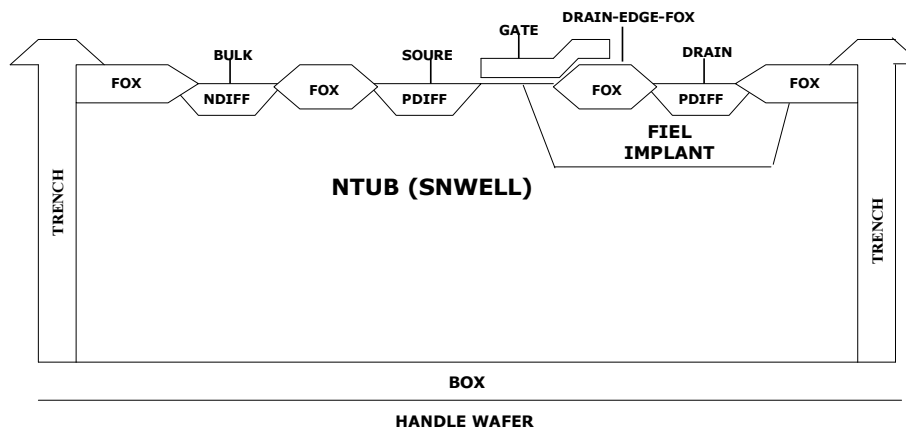
The XT06 Series complements X-FAB's 0.6 $\mu$ m Modular Mixed Signal Technology. XT06 uses dielectric isolation on SOI wafers, which allows unrestricted 40 V high and low side operation of all devices. The process offers reduced parasitics which results in smaller crosstalk, reduced noise and better EMI characteristics. XT06 thus allows innovative circuit design with reduced circuit complexity. CMOS as well as bipolar transistors are available with breakdown voltages of up to 110 V. The 5V CMOS core is compatible in design rules and transistor performance with simpler, similar 0.6  $\mu$ m CMOS processes (for example XC06 technology in standard waffer). For analog applications, several capacitor and resistor devices can be realized using the double poly architecture [4]. Also isolating trenches allows the use of forward diodes. In Table 2.1 a summary of available devices in XT06 is shown.

**Table 2.1 XT06 devices and characteristics.**

| MOS TRANSISTORS       | $V_T$ (V)               | $I_{DS}@V_{GS}$ ( $\mu$ A/ $\mu$ m)  | $BV_{DSS}$ (V) | Max $V_{DS}$ (V) |
|-----------------------|-------------------------|--------------------------------------|----------------|------------------|
| NMOS 5V               | 0.87                    | 470@5                                | 31             | 5.5              |
| PMOS 5V               | 0.9                     | 230@5                                | 12             | 5.5              |
| NMOS with ESD implant | 0.9                     | 520@5                                | 12             | 5.5              |
| NMOS HV               | 0.82                    | 220@12                               | 60             | 30               |
| PMOS HV               | 0.75                    | 190@12                               | 70             | 40               |
| RESISTORS             | RS ( $\Omega/\square$ ) | Max $V_{CE}$ (V)                     |                |                  |
| Low TC poly0          | 580                     | 60                                   |                |                  |
| High resistive poly0  | 3500                    | 60                                   |                |                  |
| FORWARD DIODES        | $V_f$ (V)               | Max $I_f$ (mA/ $\mu$ m)              | Max $V_r$ (V)  |                  |
| Rectifier diode       | 0.82                    | 0.25                                 | 10             |                  |
| Rectifier HV diode    | 0.83                    | 0.25                                 | 50             |                  |
| CAPACITORS            | BV (V)                  | Area Cap (fF/ $\mu$ m <sup>2</sup> ) | Max $V_{CC}$   |                  |
| poly0/pol1 cap        | 30                      | 1.87                                 | 8              |                  |
| linear poly0/pol1 cap | 20                      | 1.02                                 | 8              |                  |

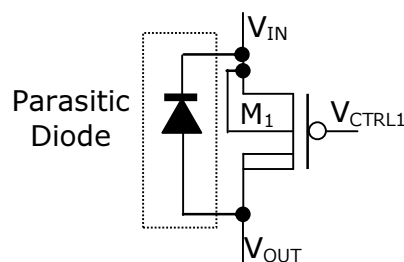
### 2.2.1 PMOS High Voltage transistor (phv) and Switches B, C.

PHV transistor in XT06 will be used as the main pass transistor in switches B and C (also in parallel with nhv in Switch A), to allow the passage or not of the stimuli. In Figure 2.3 a vertical cut of a phv transistor is shown.

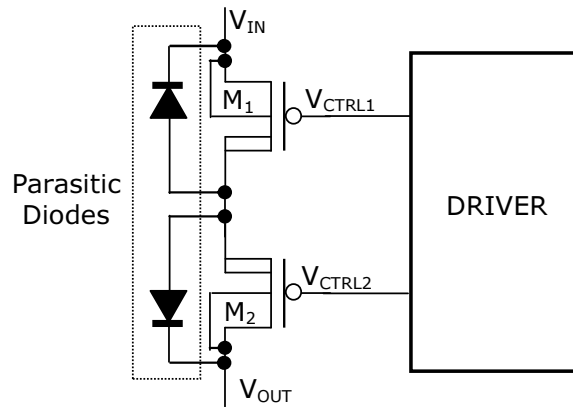


**Figure 2.3 PHV transistor vertical cut.**

In Figure 2.4 phv transistor with its associated parasitic diode is shown, the switch is opened (preventing current flow) when  $V_{CTRL1}$  is connected to  $V_{IN}$ , but if  $V_{OUT}$  is larger than  $V_{IN}$ , conduction of the stimuli will take place through the parasitic diode. It is important to mention that in the Switches to be presented, because there is no absolute maximum voltage in the circuit, but also because of the required symmetry, Source and Bulk nodes will be always tied. To comply with the symmetry specification, two phv transistors in series (shown in Figure 2.5) are used as the main composite transistor for switches B and C. The driver circuit connects  $V_{CTRL1}$  to  $V_{IN}$  and  $V_{CTRL2}$  to  $V_{OUT}$ , to open the switch. Because this PMOS switch shall control pulses down to 100mV, to close the switch both gates are connected to a negative voltage  $V_{SS}$ .  $V_{SS}$  will be also generated in switches B and C, with the aid of an external capacitor (section 3.1.3) in a charge pump configuration. If for a given application, no extremely low stimuli voltages are required, then the charge pump operation can be avoided connecting the gates to GND to close the switch.

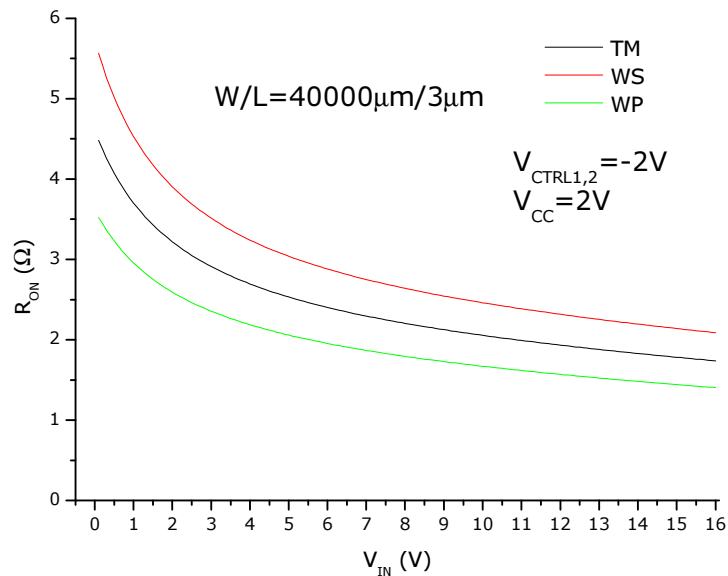


**Figure 2.4 PHV transistor switch.**



**Figure 2.5 Switches type B and C connection scheme. Two phv transistors are connected in series to control the current flow.**

In Figure 2.6 the simulated on resistance ( $R_{ON}$ ) of the switch (Figure 2.5) is shown, for the three transistor models (corners) available from the manufacturer, typical (TM), worst slow (WS - maximum threshold voltage  $V_T$ ) and worst power (WP - minimum threshold voltage  $V_T$ ). A  $W/L = 40000\mu\text{m}/3\mu\text{m}$  was selected; the length is the minimum possible for phv's, the width was selected to comply with  $5\Omega$  resistance (Typical transistor,  $V_{CC} = 2V$ ).



**Figure 2.6 Dual phv switch (switches B and C) on resistance  $R_{ON}$ , TM black, WS red and WP green.**

### 2.2.2 NMOS High Voltage transistor (nhv)

NHV transistor will be the main transistor (in parallel with phv) for the Switch A. In Figure 2.7 a vertical cut of a nhv transistor is shown.

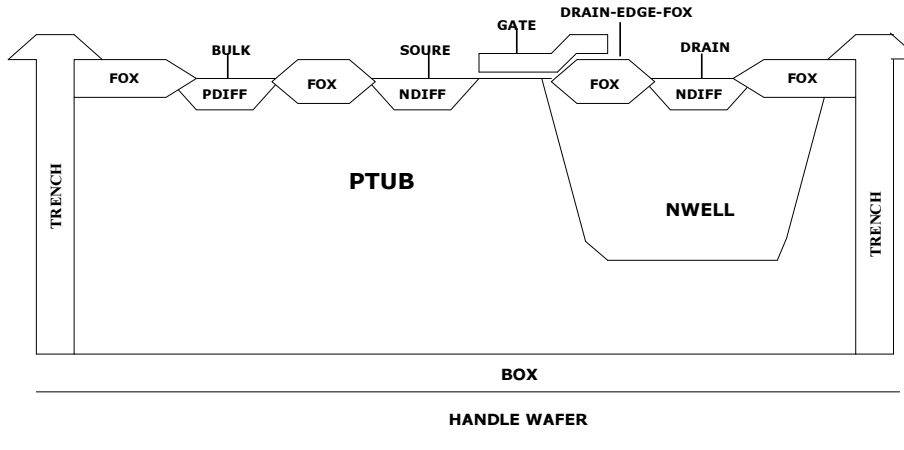


Figure 2.7 NHV transistor vertical cut.

In Figure 2.8 nhv transistor with its parasitic diode is shown, the switch is opened (preventing current flow) when  $V_{CTRL}$  is set to 0V. By making a similar analysis as in 2.2.1, two nhv transistors in series are used (shown in Figure 2.9).

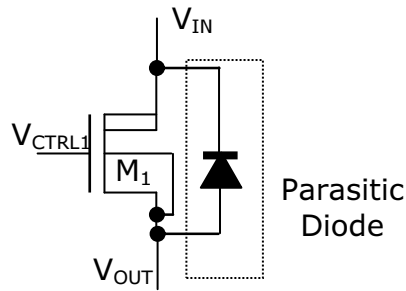
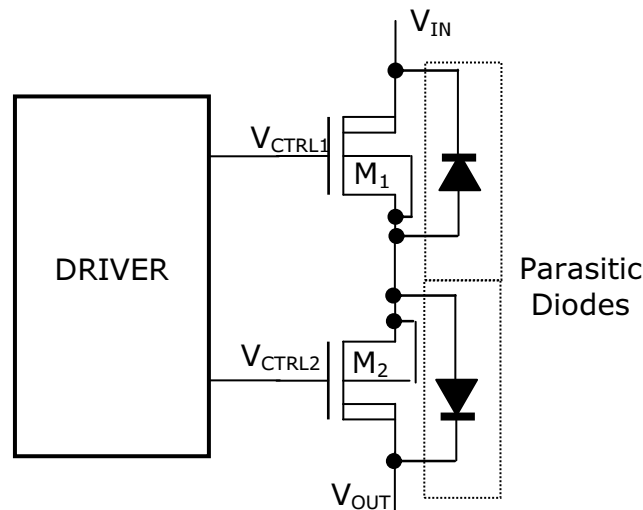
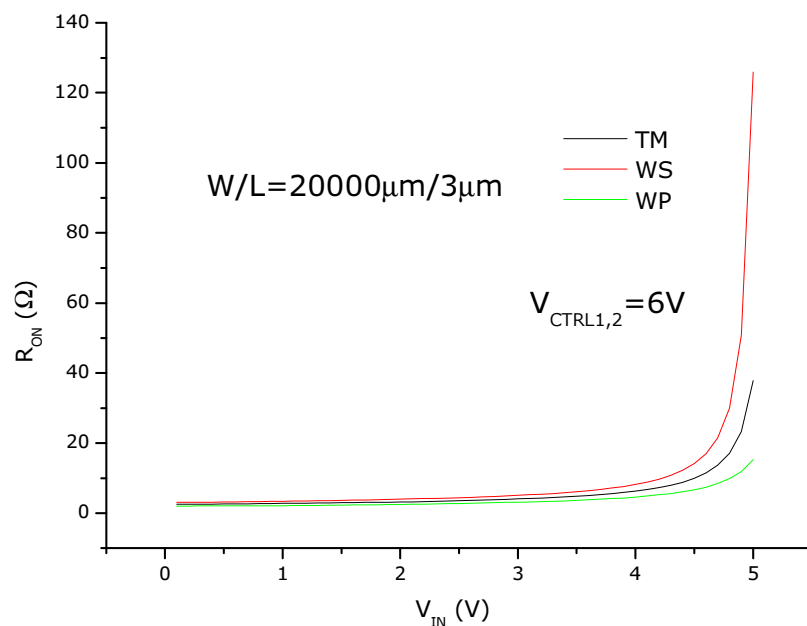


Figure 2.8 NHV transistor switch.



**Figure 2.9 Two nvh transistors in series switch.**

In Figure 2.10 the simulated on resistance ( $R_{ON}$ ) of the switch (Figure 2.9) is shown, simulations for the three models, typical (TM), worst slow (WS) and worst power (WP).

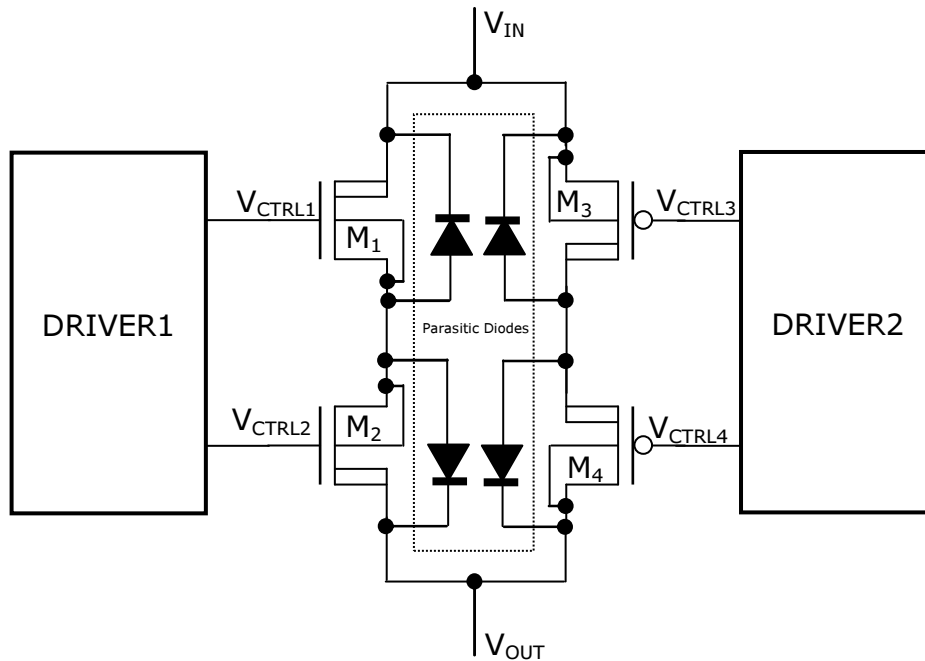


**Figure 2.10 Switch  $R_{ON}$ , TM black, WS red and WP green.**

### 2.2.3 High Voltage Transmission gate (TG) for switch A.

By combining the main switches shown in Figure 2.5 and Figure 2.9 a high voltage transmission gate switch is obtained as shown in Figure 2.11. The driver circuit connects  $V_{CTRL1}$  to 0V,  $V_{CTRL2}$  to 0V,  $V_{CTRL3}$  to  $V_{IN}$  and  $V_{CTRL4}$  to

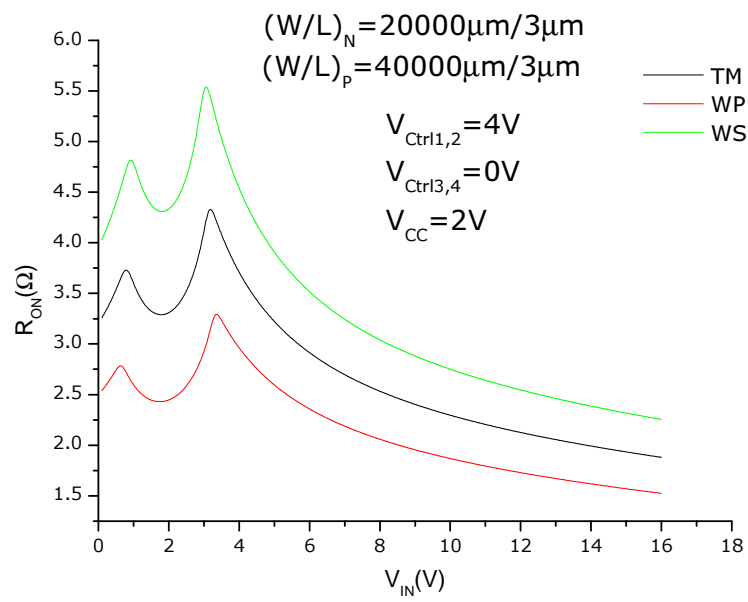
$V_{OUT}$ , to open the switch. Because this switch shall control pulses down to 100mV, to close the switch  $V_{CTRL1,2}$  gates are connected to  $2V_{CC}$  voltage (two times power supply voltage) while  $V_{CTRL3,4}$  are connected to 0V.  $2V_{CC}$  will be also generated in switch A, with the aid of an external capacitor (section 3.1.2) in a charge pump configuration. In comparison to the circuit in Fig.2.5, apart from the lower total resistance particularly for the lower stimuli voltages, the main advantage of the HV TG configuration, is that it avoids the use of a negative voltage for switching. A negative voltage even in the case of a isolated technology may, present some difficulties for the designer.



**Figure 2.11 High voltage transmission gate of Switch A.**

In Figure 2.12 the simulated on resistance ( $R_{ON}$ ) of the switch (Figure 2.11) is shown, all simulations were done for three models, typical (TM), worst slow (WS) and worst power (WP).





**Figure 2.12 High voltage transmission gate of Switch A total on-resistance  $R_{\text{ON}}$ , TM black, WS red and WP green.**

## 2.3 Main switch dimension

Transistor sizing was calculated to comply with the  $5\Omega$  switch resistance specified in section 1.3 (with only small deviation in the case of WS transistors, which was considered acceptable for the sake of a moderate silicon area). The total resistance of PMOS main MOSFETs of Switch B and Switch C, are shown in Figure 2.6, while Figure 2.12 shows the equivalent resistance of Switch A's TG. The selected main transistor's dimensions are:

- For PMOS  $40000\mu\text{m}/3\mu\text{m}$
- For NMOS  $20000\mu\text{m}/3\mu\text{m}$  (Only Switch A)

It should be pointed out that the approximated resistance of the metal wires user for routing was calculated. The amount of contacts and metal wires width, were determined to achieve an approximated  $1\Omega$  total connection resistance in the stimulus path that shall be added to MOSFETs  $R_{\text{ON}}$ . Total maximum resistance was still considered acceptable for the application. The detailed metal wire plus contacts resistance calculation is omitted for the sake of simplicity.

## 3 Driver circuitry & complete switch design

### 3.1 Basic building blocks

In this section the basic blocks that compose the designed switches (drivers) are presented.

#### 3.1.1 Level-shifters

A level-shifter (LS) adapts logical signals (0 to  $V_{CC}$ ) to another level that could be higher or lower than  $V_{CC}$  or in our case even negative voltage values. For the design of the switches drivers, different types of level-shifters were used.

##### 3.1.1.1 NMOS level-shifter

In Figure 3.1 a basic level shifter (from now it will be denoted as NMOS\_LS) is shown, it is a classical circuit to translate a low voltage (LV) digital signal 0- $V_{CC}$ , into a high voltage (HV) one, 0- $2V_{CC}$  in this case [5][27][30]. The circuit is named NMOS\_LS because it will drive the gate of the main NMOS in the TG of Figure 2.11. The "In" signal controls the output "Out", the NMOS\_LS has two states:

- State "1": When the "In" signal is  $V_{CC}$  the  $M_1, M_5$  and  $M_6$  transistors are turned on and the output "Out" goes to  $2V_{CC}$  voltage which will be generated by a two times voltage multiplier (section 3.1.2).
- State "0": When the "In" signal is 0V, the transistors  $M_2, M_3$  and  $M_4$  are switched on and the output "Out" goes to 0V.

It should be pointed that the circuit in Figure 3.1 has no static power consumption.



### 3.1.1.2 $2V_{CC}$ level-shifter

The  $2V_{CC}$  level-shifter (named  $2V_{CC\_LS}$ ) is a small variation of the  $NMOS\_LS$  with only a slight transistor size change.  $2V_{CC\_LS}$  will be used in the charge pump of section 3.1.2.

Whilst  $2V_{CC\_LS}$  is nearly equal to the one in Figure 3.1, in this work we opted to provide different names to different circuit blocks, even with only a small change in circuit topology or layout. Also the original circuit block names set given at the very first design stages was preserved in this document, although it may look a bit cumbersome for who is not familiar with the circuits.

**Table 3.2  $2V_{CC}$  level-shifter transistors dimensions.**

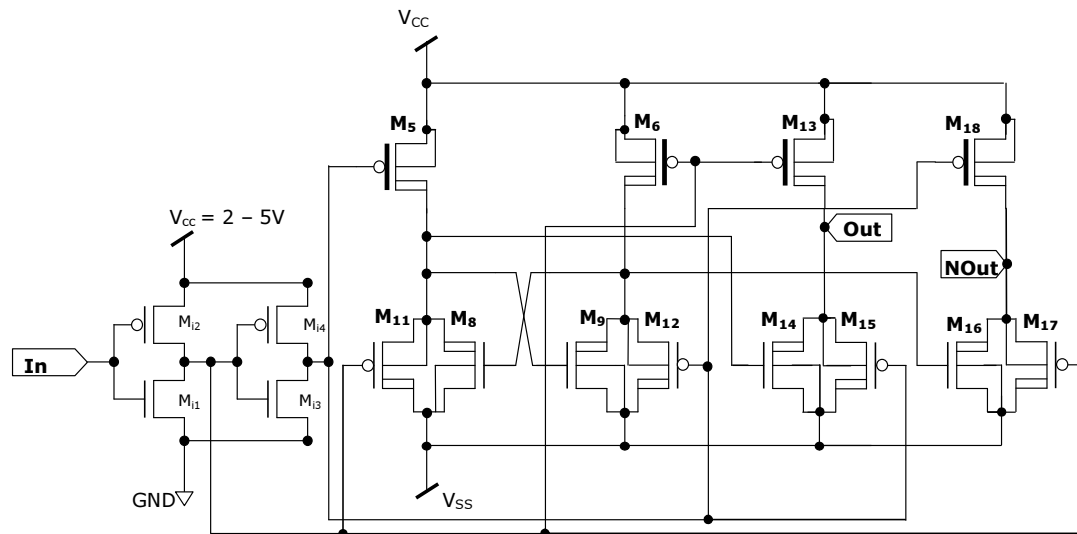
| Transistors | W/L ( $\mu\text{m}/\mu\text{m}$ ) |
|-------------|-----------------------------------|
| $M_{1,4}$   | 100/3                             |
| $M_{1,2}$   | 60/3                              |
| $M_{3,6}$   | 100/3                             |
| $M_{4,5}$   | 10/3                              |

### 3.1.1.3 Negative level-shifter

In Figure 3.2 the negative level-shifter ( $NEG\_LS$ ) is shown. This LS translates a logical '0' from 0V at the input, to a negative voltage  $V_{SS}$  at the output. The logical '1' is equal to  $V_{CC}$  at both LV and HV side. The  $NEG\_LS$  has two inverted outputs in the HV, the circuit operation can be described in two states:

- State "1": When the "In" signal is  $V_{CC}$  the transistors,  $M_6, M_8, M_{11}, M_{13}, M_{16}$  and  $M_{17}$  are closed and transistors,  $M_5, M_9, M_{12}, M_{14}, M_{15}$  and  $M_{18}$  are open, making the output "Out" to go to  $V_{CC}$  and "NOut" go to  $V_{SS}$ , generated by the  $V_{SS}$  generator (section 3.1.3).
- State "0": When the "In" signal is 0V the transistors,  $M_6, M_8, M_{11}, M_{13}, M_{16}$  and  $M_{17}$  are opened and transistors,  $M_5, M_9, M_{12}, M_{14}, M_{15}$  and  $M_{18}$  are closed, making the output "Out" to go to  $V_{SS}$  and "NOut" to  $V_{CC}$ .

Note transistor pairs NMOS-PMOS in parallel were connected to  $V_{SS}$ , to ensure a stable  $NEG\_LS$  operation in the full range of  $V_{CC}$  and  $V_{SS}$ .



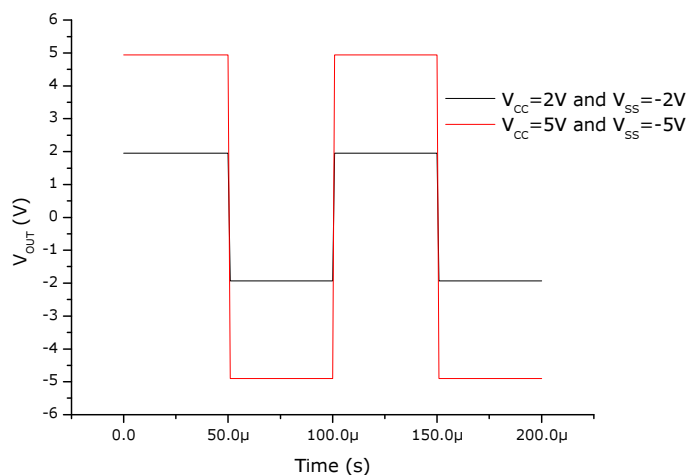
**Figure 3.2 Negative level-shifter.**

In Table 3.3 a summary of transistors dimensions is presented.

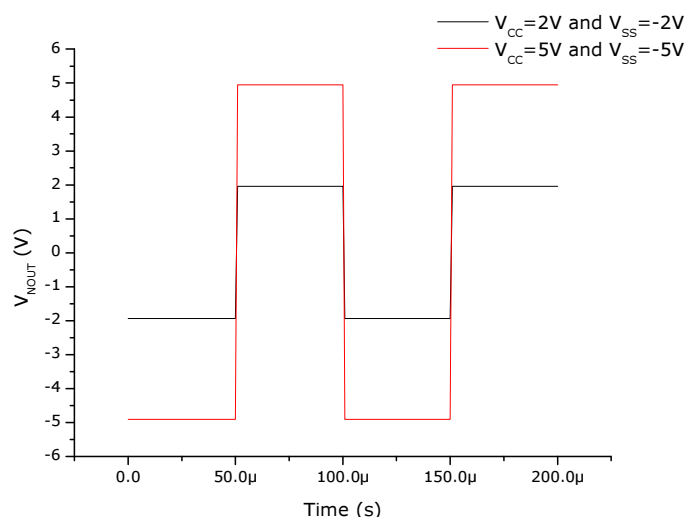
**Table 3.3 Negative level-shifter transistors dimensions.**

| Transistors           | W/L ( $\mu\text{m}/\mu\text{m}$ ) |
|-----------------------|-----------------------------------|
| $M_{1,1-4}$           | 20/3                              |
| $M_{5,6,13,14,15,16}$ | 60/3                              |
| $M_{8,9,11,12}$       | 10/3                              |

In Figure 3.3 and Figure 3.4 the NEG\_LS simulated outputs "Out" and "NOut" are shown, for a 10KHz square wave input. This and most simulations in the document were performed for the three models: TM, WS and WP, but only TM is shown for the sake of simplicity, but also because no significant difference was observed.



**Figure 3.3 Negative level shifter non inverted output (Out) transient simulation for  $V_{CC}$  2V, 5V and  $V_{SS}$  -2V, -5V.**



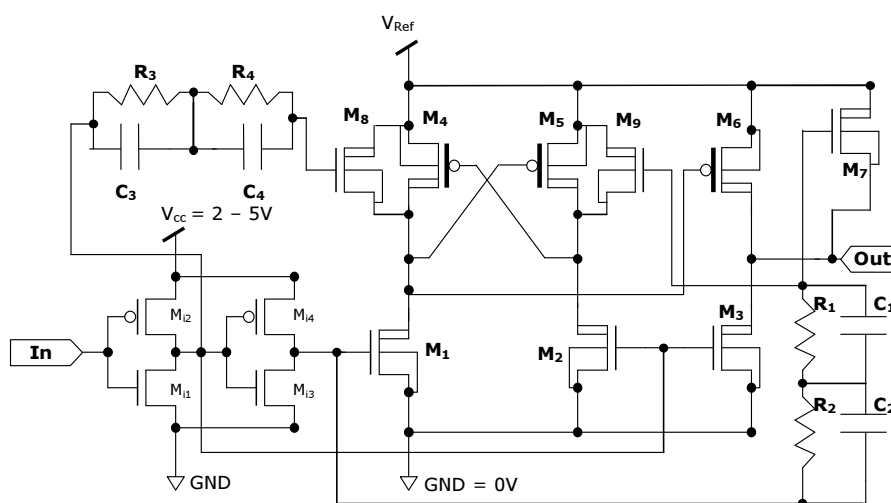
**Figure 3.4 Negative level shifter inverted output (NOut) transient simulation, for  $V_{CC}$  2V, 5V and  $V_{SS}$  -2V, -5V.**

### 3.1.1.4 SAFEPMOS1 level-shifter

In Figure 3.5 a PMOS level-shifter (named SAFEPMOS1\_LS) is shown, to translate a digital input signal 'In'  $0-V_{CC}$ , into a HV digital output signal  $0-V_{Ref}$ , with a distinctive full range for  $V_{Ref}$  from 0 to 16V. The SAFEPMOS1\_LS is a variation of the NMOS\_LS, but the output signal "Out" is connected to  $V_{Ref}$  through a transmission gate (TG)  $M_6$  and  $M_7$ . Also transistors  $M_4$ ,  $M_5$ , in Figure 3.1, are now substituted by a TG. The transmission gate is necessary because  $V_{Ref}$  can be very small (100mV) and  $M_6$  will not work properly; for small  $V_{Ref}$ 's current conduction will take place through  $M_7$ . Transistors  $M_8$  and  $M_9$ , added for the same reason,

guarantee the stability of the level shifter at low  $V_{Ref}$  values. Because  $V_{Ref}$  voltage may be connected directly to the electrodes in tissue contact (see Section 3.2) and since the gates of transistors  $M_7$ ,  $M_8$  and  $M_9$  go to  $V_{CC}$  when there is no stimulation, if there is a failure in the gate oxide of one of these transistors, a direct path from  $V_{CC}$  to tissue may be created. To prevent this direct path, the gates are commanded through a RC circuit, where  $R$  has an impedance larger than  $1M\Omega$ , to limit the current flow into tissue under a single element failure condition. The LS\_P has two states:

- State "1" or " $V_{Ref}$ ": When the "In" signal is  $V_{CC}$  the the output "Out" goes to  $V_{Ref}$ .
- State "0": When the "In" signal is  $0V$ , the output "Out" goes to  $0V$ .



**Figure 3.5 SAFEMOS1 level-shifter.**

Transistor sizes were chosen ensure a full charge (from 100m to 16V) or discharge (from 16V to 100mV) of the output in less than 500ns with a load of 0.36nF corresponding to the approximated capacitive gate load of the large  $40000\mu\text{m}/3\mu\text{m}$  phv transistor.

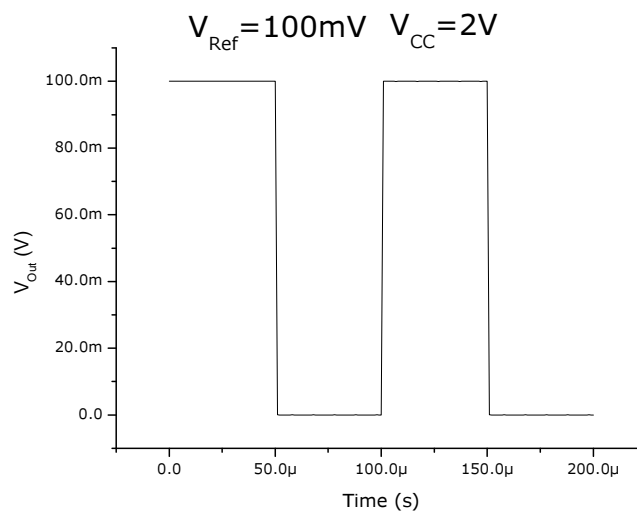
In Table 3.4 a summary of transistors sizes is presented.

**Table 3.4 SAFEMOS1 level-shifter transistors dimensions and R, C, values.**

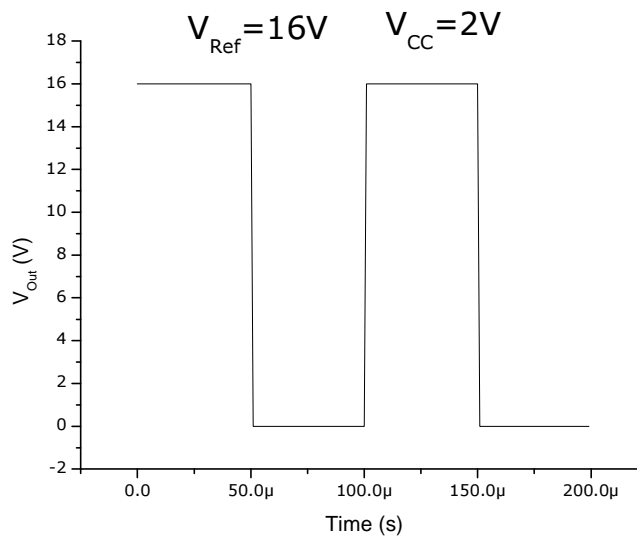
| Transistors            | W/L ( $\mu\text{m}/\mu\text{m}$ ) |
|------------------------|-----------------------------------|
| $M_{11-4}$             | 20/3                              |
| $M_{1,2}$              | 60/3                              |
| $M_{3,6,7}$            | 400/3                             |
| $M_{4,5,8,9}$          | 10/3                              |
| Component              | Value                             |
| $C_{1,2}$ (cpoly-poly) | 20pF                              |
| $C_{3,4}$ (cpoly-poly) | 5 <sup>o</sup> pF                 |
| $R_{1,2,3,4}$ (rpolyh) | 500k $\Omega$                     |

The SAFEMOS1\_LS simulated output "Out" is shown for a 10KHz square wave input and  $V_{CC} = 2V$ .





**Figure 3.6 SAFEPMOS1\_LS simulated output "Out" with  $V_{Ref}$  100mV and  $V_{CC}$  2V.**



**Figure 3.7 SAFEPMOS1\_LS simulated output "Out" with  $V_{Ref}$  16V and  $V_{CC}$  2V.**

### 3.1.1.5 SAFEMOS2 level-shifter

In Figure 3.8 the SAFEMOS2 level-shifter (SAFEMOS2\_LS) is shown. This circuit connects its output, "GATE", with the input, " $V_{IN}$ ", when the "CTRL" signal is 0V. If CTRL is  $V_{CC}$ , "GATE" is left in third state. " $\Phi_{2N}$ " is generated by the NEG\_LS (section 3.1.1.3) used as an inverter. The SAFEMOS2\_LS circuit is very similar to the SAFEMOS1\_LS, but with a few differences:

- All transistors connected to  $V_{IN}$  ( $M_{4x}$ ,  $M_{5x}$ ,  $M_{6,7}$ ) are implemented with two transistors connected in series but flipped (Source connected to Source). This configuration with two diodes connected in opposite, prevents current circulation even in the case of negative voltage peaks in  $V_{IN}$  (remember  $V_{IN}$  is connected to tissue and its voltage may vary because of different kinds of coupling).
- The only connection to the output GATE is  $V_{IN}$  through  $M_{6,7}$ , which is controlled by CTRL, allowing to leave GATE in high impedance (third state) when CTRL is  $V_{CC}$ .
- As  $V_{IN}$  can vary from 16V to 100mV,  $M_{4x}$ ,  $M_{5x}$ ,  $M_{6,7}$  are connected as a transmission gate, ensuring operation in all the possible ranges.
- As  $M_4$ ,  $M_5$  and  $M_7$  gates are connected to  $V_{CC}$  when no stimulus is present, for safety reason this could be a problem, as if any of this transistors oxide is punctured (single failure), there will be a direct current path into the tissue. The connection of this gates through an RC circuit, limit this current to acceptable levels (two capacitors are used to withstand the HV after a failure).

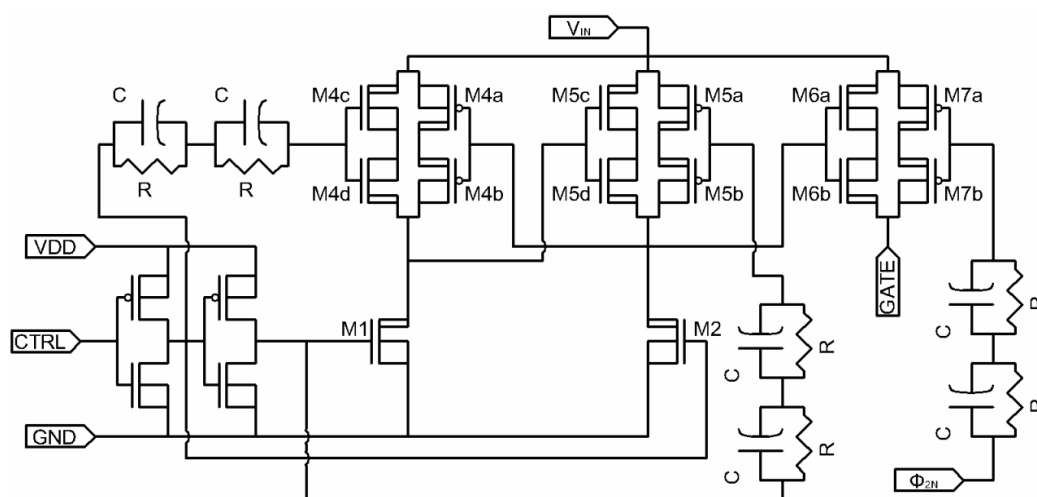


Figure 3.8 SAFEMOS2 level-shifter.

In Table 3.5 a summary of transistors sizes is presented.

**Table 3.5 SAFEPMOS2 level-shifter transistors dimensions.**

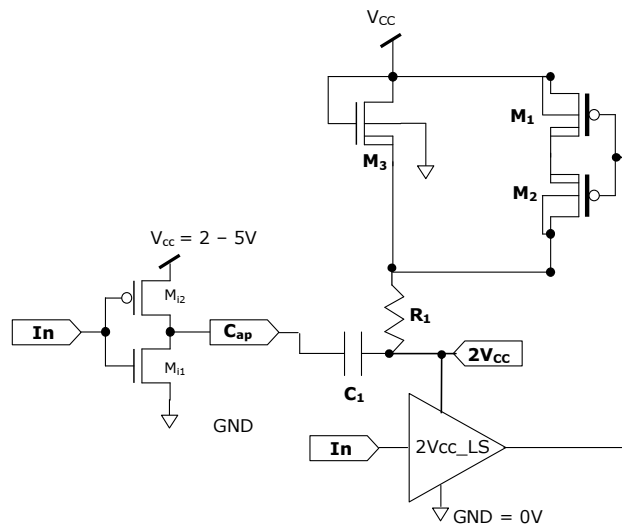
| <b>Transistors</b> | <b>W/L (<math>\mu\text{m}/\mu\text{m}</math>)</b> |
|--------------------|---|
| $M_{i1-4}$         | 100/3   |
| $M_{1,2}$          | 60/3  |
| $M_{6,7}$          | 400/3   |
| $M_{4i,5i}$        | 10/3  |
| <b>Component</b>   | <b>Value</b>                                      |
| C (cpoly-poly)     | 5pF   |
| R (rpolyh)         | 650k $\Omega$                                     |

### 3.1.2 $2V_{CC}$ generator.

The main NMOS transistors in Figure 2.11 require a voltage two times  $V_{CC}$ . This voltage is generated on-chip, momentarily during a stimulus, by the  $2V_{CC}$  generator shown in Figure 3.9. An external pumping capacitor is necessary, the  $2V_{CC}$  generator has two states:

- State "1": When the "In" signal is  $V_{CC}$ , the capacitor  $C_1$  is charged to  $V_{CC}$  through  $M_1$  and  $M_2$ . The  $M_3$  transistor is in diode configuration, it is used to start-up the circuit.
- $2V_{CC}$  state: When the "In" signal is 0V the output " $C_{ap}$ " of the inverter goes to  $V_{CC}$ . As the capacitor already charged and cannot discharge because the  $2V_{CC\_LS}$  cuts off the transistors  $M_1$  and  $M_2$  the output " $2V_{CC}$ " goes to  $2xV_{CC}$  volts.

Note:  $C_1$  is an external capacitor and its value can vary from tens nF to few  $\mu\text{F}$ , depending on admissible leakages, capacitor footprint size, type, or stimuli duration.



**Figure 3.9 2V<sub>CC</sub> generator, C<sub>1</sub> external.**

In Table 3.6 a summary of transistors sizes and components values is presented.

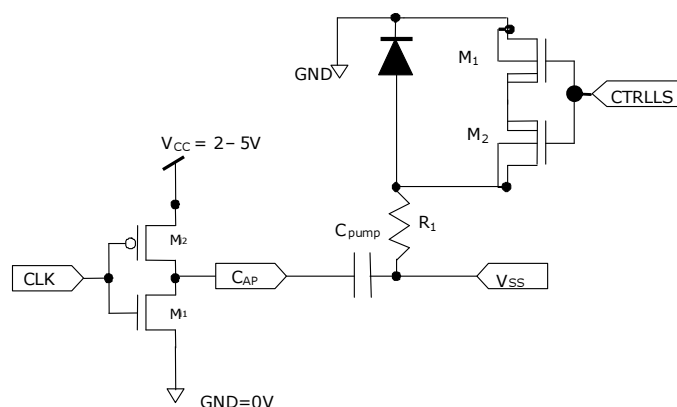
**Table 3.6 2V<sub>CC</sub> generator transistors dimensions and components values.**

| Transistors               | W/L (μm/ μm)  |
|---------------------------|---------------|
| M <sub>1i1-2</sub>        | 200/3         |
| M <sub>1,2</sub>          | 60/3          |
| M <sub>3</sub>            | 10/3          |
| Component                 | Value         |
| C <sub>1</sub> (external) | 1μF (typical) |
| R <sub>1</sub> (rpolyh)   | 100Ω          |

### 3.1.3 V<sub>SS</sub> generator

The main PMOS transistors of Switches B, C in section 2.2.1, require a negative voltage (V<sub>SS</sub>) (see also NEG\_LS and the NegD of section 3.1.4). This voltage is generated on-chip by the V<sub>SS</sub> generator shown in Figure 3.10. As the V<sub>SS</sub> is only needed when stimulating, it is only generated when "CTRL" goes to V<sub>CC</sub>. The generated voltage is V<sub>SS</sub> = -V<sub>CC</sub>, using an external pump capacitor C<sub>pump</sub>. "CTRLLS" is generated by a NEG\_LS block using the inverted output. The V<sub>SS</sub> generator has two states:

- State "0": When "CLK" is 0V the node C<sub>AP</sub> is connected to V<sub>CC</sub> through M<sub>1i2</sub> and the node V<sub>SS</sub> is connected to GND through M<sub>1</sub> and M<sub>2</sub>. This effectively charges the external capacitor C<sub>pump</sub> to V<sub>CC</sub>. The diode is used in the start-up of the circuit.
- -V<sub>CC</sub> state: When "CLK" is V<sub>CC</sub> the node CAP is connected to GND but the capacitor cannot discharge, so the node V<sub>SS</sub> acquires a negative voltage of -V<sub>CC</sub>.



**Figure 3.10 V<sub>SS</sub> generator.**

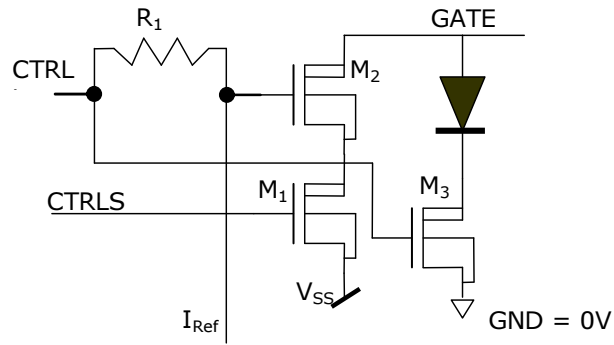
In Table 3.7 a summary of transistors sizes and components value is presented.

**Table 3.7 V<sub>SS</sub> generator transistors dimensions and components values.**

| <b>Transistors</b>        | <b>W/L (μm/ μm)</b> |
|---------------------------|---------------------|
| M <sub>i1-2</sub>         | 200/3               |
| M <sub>1,2</sub>          | 60/3                |
| <b>Component</b>          | <b>Value</b>        |
| C <sub>1</sub> (external) | 1μF (typical)       |
| R <sub>1</sub> (rpolyh)   | 100Ω                |

### 3.1.4 Negative driver.

In Figure 3.11 the Negative driver (NegD) is shown. The NegD will be used in Switch B and Switch C, to connect the gate of the main PMOS (the output "GATE" of Figure 3.11) to V<sub>SS</sub>, but depending on the control loop current I<sub>Ref</sub>, of section 3.1.5. When the "CTRL" signal is '1' (V<sub>CC</sub>) GATE node goes to V<sub>SS</sub> if I<sub>ref</sub> = 0. If the "CTRL" signal is a 0V, the "GATE" is left in third state. "CTRLS" is generated by a NEG\_LS (section 3.1.1.3) and is in phase with "CTRL". When I<sub>Ref</sub> ≈ 0 and "CTRL" is V<sub>CC</sub>, the transistor M<sub>2</sub> is closed and "GATE" is connected to V<sub>SS</sub> through M<sub>1</sub> and M<sub>2</sub>, but if I<sub>Ref</sub> is large enough, M<sub>2</sub> will be open and "GATE" will be connected to GND through M<sub>3</sub> (and the diode in series). The diode also ensures that when I<sub>Ref</sub> ≈ 0 no conduction between "GATE" and GND occurs. To summarize, NegD connects "GATE" to a low voltage when CTRL is V<sub>CC</sub> and leaves it in third state otherwise. The low voltage is either V<sub>SS</sub> if I<sub>Ref</sub> ≈ 0 or GND.



**Figure 3.11 Negative driver.**

In Table 3.8 a summary of transistors size and components value is presented.

**Table 3.8 Negative driver transistors dimensions and component values.**

| <b>Transistors</b> | <b>W/L (<math>\mu\text{m}/\mu\text{m}</math>)</b> |
|--------------------|---|
| $M_{1,2,3}$        | 600/3   |
| <b>Component</b>   | <b>Value</b>                                      |
| $R_1$ (rpolym)     | 683k $\Omega$                                     |

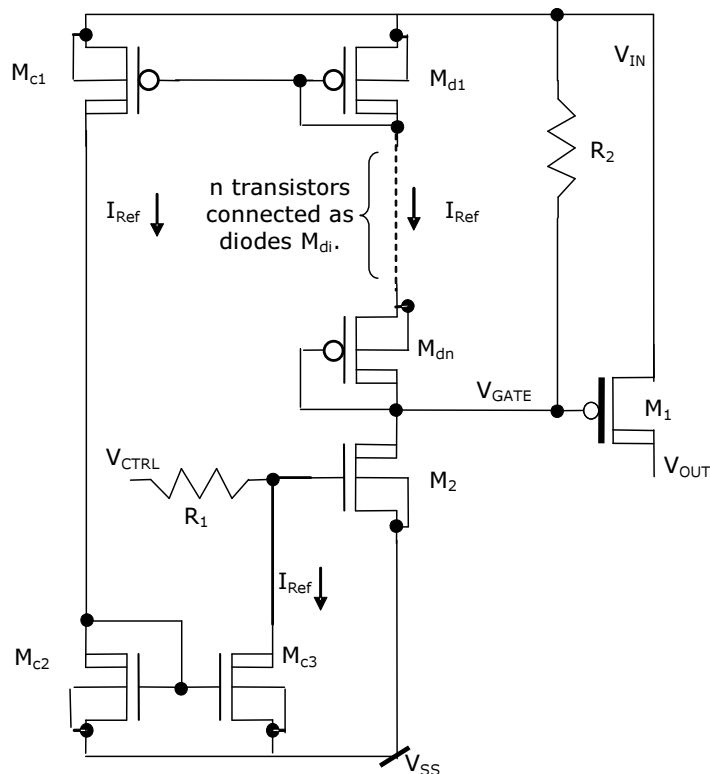
### 3.1.5 A novel over voltage $V_{GS}$ protection circuit

The circuit in Figure 3.12 shows a PMOS switch  $M_1$ , which may be a large output driver transistor that may connect the voltage  $V_{IN}$  to  $V_{OUT}$ . While  $V_{DS1}$  ( $V_{IN}-V_{OUT}$ ) may be large for example up to 50V in a HV technology,  $V_{GS1}$  is limited to a much lower value, 5V in standard CMOS and upto 12-18V in a HV technology, because of the gate oxide strength. To turn on  $M_1$ , a driver may connect its gate to  $V_{SS}$  (the most negative voltage in the circuit) but there is a risk of gate puncturing if  $V_{GS1}$  exceeds maximum rating. To overcome this problem a voltage control loop is proposed.

$V_{CTRL}$  is a low voltage logic signal varying between a low voltage  $V_{CC}$  (i.e. 3 V) and  $V_{SS}$ ; when  $V_{CTRL}$  is  $V_{CC}$   $M_2$  is turned on if  $I_{Ref} = 0$  thus pushing  $V_{G1}$  to  $V_{SS}$  and turning on  $M_1$ . But as  $I_{Ref}$  increases, the voltage drop through  $R_1$  increases as well and  $M_2$  resistance dramatically increases (up to cutoff) and  $V_{G1}$  may reach an equilibrium voltage well above  $V_{SS}$ .  $I_{Ref}$  is a function of  $V_{GS1}$  voltage because of the  $n$  stacked diode-connected  $M_{di}$  transistors, which copy their current to the  $V_{G2}$  node through  $M_{ci}$  transistors. As  $V_{GS1}$  increases,  $I_{Ref}$  increases in a strongly-non linear way and an equilibrium  $V_{GS1}$  voltage close to the voltage drop of the stacked  $M_{di}$  diodes is achieved.  $V_{GS1}$  voltage during  $M_1$  conduction is a function of  $n$ , the number of stacked  $M_{di}$  transistors, their threshold voltage and  $M_2$ ,  $R_1$  characteristics. These circuit elements should be designed according to rated  $V_{GS}$  voltage for the technology and corner cases.

When  $V_{CTRL}$  is  $V_{SS}$ ,  $M_2$  transistor is opened and  $R_2$  pushes  $V_{G1}$  to  $V_{IN}$  thus  $M_1$  is opened.  $R_2$  has been placed to illustrate circuit operation but may be substituted by a more complex circuit to avoid static current consumption when  $M_1$  is turned on, or to increase speed. Note that this control loop also draws some current when  $M_1$  is on (that can be minimum with a careful design), but may operate regardless of the  $V_{IN}$  value ranging to an arbitrarily large value. A modified version of the circuit will be employed, to implement Switch B, Switch C circuits, using the driver in the previous section.

Finally it should be pointed that in regular switching applications  $M_1$  size is very large thus validating the use of the extra circuit elements count. In these work a large  $M_1$  ( $W/L = 40000\mu\text{m}/3\mu\text{m}$ ) dual transistor is employed and the control loop resulted much smaller.



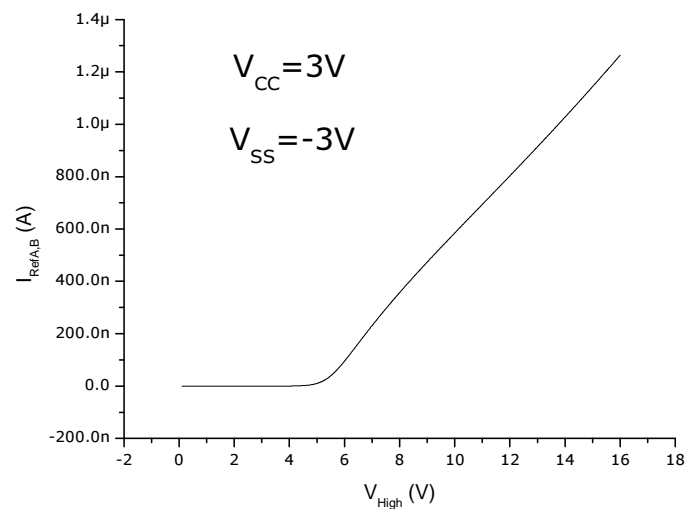
**Figure 3.12 Over voltage  $V_{GS}$  protection circuit scheme.**

In Figure 3.13 the actual employed circuit that generates the current  $I_{Ref}$  for the NegD (section 3.1.4) is shown. The circuit copies the current through the  $M_0$  branch to the output transistors  $M_2$  and  $M_3$ . If there is no stimulation, CTRL is 0V,  $M_0$  is opened so  $I_{Ref} = 0$ . When CTRL is  $V_{CC}$ ,  $M_0$  is closed, but only if  $V_{HIGH}$  is high enough to overcome the  $V_{GS}$  of the 6 transistors ( $M_{di}$ ) connected as diodes, does current actually flow through  $M_0$ . Therefore the  $I_{Ref}$  current is only generated if CTRL is  $V_{CC}$  and  $V_{High}$  is high enough. Note that this is a variation of the control loop previously proposed (see Figure 3.12), where the reference voltage is measured to fixed ground instead of  $V_{GATE}$ , the actual protection circuit is the combination of the circuit in Figure 3.13 and the negative driver form section 3.1.4.





In Figure 3.14 the simulated current reference of the over voltage  $V_{GS}$  protection circuit is shown, for  $V_{SS}$  -3V and  $V_{CC}$  3V sweeping  $V_{High}$  from 100mV to 16V.



**Figure 3.14 Simulated current reference of the over voltage  $V_{GS}$  protection circuit for  $V_{SS}$  -3V and  $V_{CC}$  3V**

## 3.2 Switch A

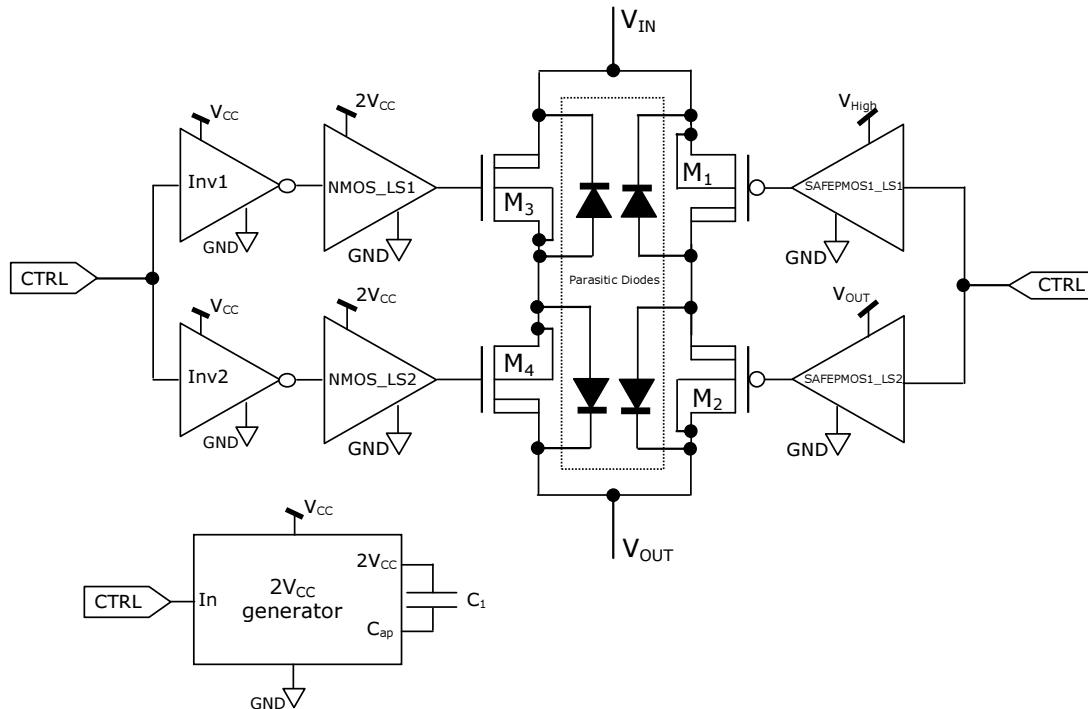
In Figure 3.15 the switch A is shown, it is implemented with the following basic building blocks from section 3.1:

- Two SAFEPMOS1 level-shifters (SAFEPMOS1\_LS1(2)) (section 3.1.1.4).
- Two NMOS level-shifters (NMOS\_LS1(2)) (section 3.1.1.1).
- One high voltage transmission gate (section 2.2.3).
- Two standard inverters (Inv1(2)).
- $2V_{CC}$  generator (section 3.1.2).

Stimuli conduction is done through the high voltage transmission gate ( $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$ ). To turn the switch off (no stimuli conduction)  $M_1$  and  $M_2$  gates are connected to  $V_{IN}$  and  $V_{OUT}$  respectively and  $M_3$  and  $M_4$  to ground. To turn on the switch (stimuli conduction)  $M_1$  and  $M_2$  gates are connected to ground and  $M_3$  and  $M_4$  gates to  $2V_{CC}$ . The  $2V_{CC}$  voltage is generated during stimulation only. To sum up the complete switch has two states:

- Closed state: When the signal "CTRL" is 0V the outputs of SAFEPMOS1\_LS1(2) and NMOS\_LS1(2) are 0V and  $2V_{CC}$  respectively, making conduction possible through the high voltage transmission gate ( $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$ ). If the voltages  $V_{IN}$ ,  $V_{OUT}$  are high, the  $M_1$ ,  $M_2$  branch will conduct most of the current, if not, the  $M_3$ ,  $M_4$  branch will transport most of the current.

- Open State: When the signal "CTRL" is  $V_{CC}$  the outputs of SAFEPMOS1\_LS1(2) and NMOS\_LS1(2) are  $V_{High}(V_{OUT})$  and  $0V$  respectively, cutting off conduction through high voltage transmission gate ( $M_1, M_2, M_3$  and  $M_4$ ) if  $V_{High} \geq V_{IN}$ .



**Figure 3.15 Switch A schematic,  $M_{1,2W/L}=40000\mu\text{m}/3\mu\text{m}$  and  $M_{3,4W/L}=20000\mu\text{m}/3\mu\text{m}$  .**

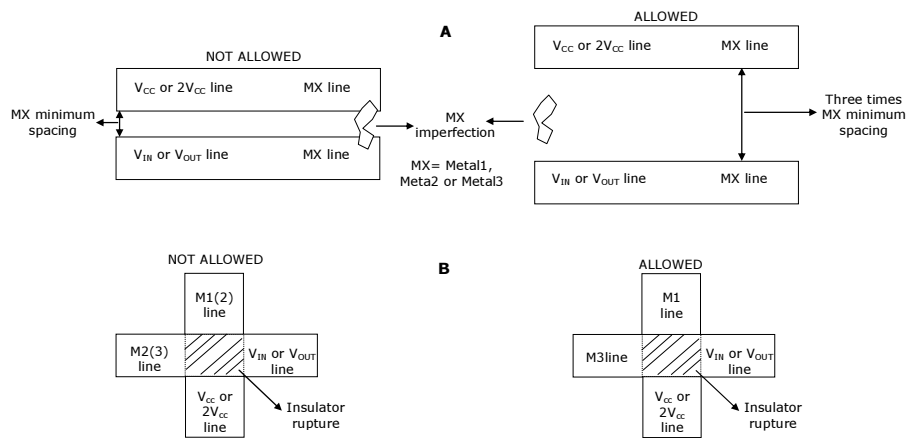
The switch A has 8 PADs:

- CTRL: Opens ( $V_{CC}$ ) and closes ( $0V$ ) the switch.
- GND: Switch ground.
- $V_{CC}$ : Power supply.
- $C_{ap}$ :  $C_1$  external capacitor connection for the charge pump.
- $2V_{CC}$ :  $2V_{CC}$  generated voltage.
- $V_{IN}$ : Switch input.
- $V_{OUT}$ : Switch output.
- $V_{High}$ : Reference voltage for closing the switch, normally is just connected to  $V_{IN}$ .

In Figure 3.17 the complete layout of the switch A is shown. The total occupied area is  $3.8\text{mm}^2$  (PADs included). Special care was taken in to account when making the layout, to prevent DC current to go through the electrode in case of a single failure. The following precautions were taken:

- Wires conducting  $V_{CC}$  or  $2V_{CC}$  shall not be closer than three times the minimum metal spacing to  $V_{IN}$  or  $V_{OUT}$ .
- Lines conduction  $V_{CC}$  or  $2V_{CC}$  shall cross over  $V_{IN}$  or  $V_{OUT}$  lines only if they have two or more metal layer level of difference (see Figure 3.16 B).

- The total resistance of the line going from  $V_{IN}$  to the high voltage transmission gate (TG) and from the TG to  $V_{OUT}$  shall be smaller than  $1\Omega$



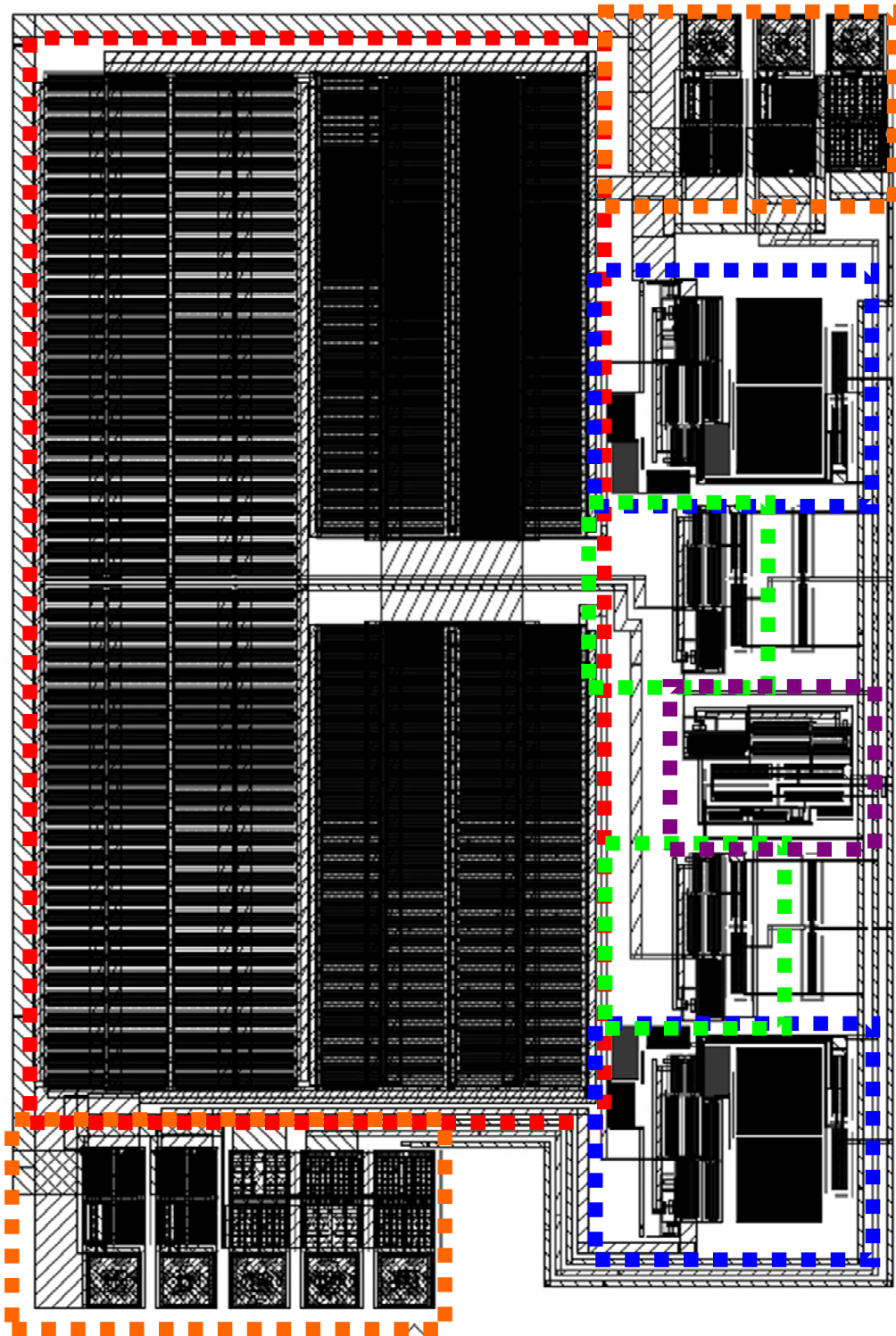
**Figure 3.16** Layout taken cautions.

### Safety Analysis:

In the circuit in Figure 3.15,  $M_2$ ,  $M_4$  and SAFEPMOS1\_LS1(2) are in direct contact to the electrode to tissue. Thus the safety analysis shall consider any possible failure on these circuit devices when not stimulating. If  $M_2$ 's gate is punctured there is no problem. If  $M_4$ 's gate is punctured, the tissue is connected to GND through an unpredictable resistance. In an implantable device, there is no problem to connect the tissue to a given voltage; the problem is to allow a DC current through it. **Thus the medical device manufacturer, that employs the Switch A, shall guarantee that when not stimulating all the electrodes are either in high impedance, or connected to GND. GND shall be the common mode voltage for biological tissue.** Now the safety condition can be better described in the following manner: a single failure of a circuit device shall not connect the electrode to a potential different than GND, or the current shall be limited to a few  $\mu A$ . SAFEPMOS1\_LS fulfils this requirement as discussed in the corresponding section. Finally, a Drain to Source short circuit in  $M_4$ ,  $M_2$  may connect  $V_{IN}$  to  $V_{OUT}$  through  $M_3$ 's,  $M_1$ 's associated diodes, thus depending on the medical device electrode's distribution, the manufacturer shall turn off the stimuli voltage generator  $V_{IN}$  when not stimulating.

An overall conclusion is that the proposed Switch cannot guarantee by itself the safety of the device being implemented. In fact, at least  $V_{IN}$  to  $V_{OUT}$  connection in the case of failure cannot be avoided. From the implantable medical device perspective, the proposed switch provides a tool to design a safe device because any single failure may provoke only leakages to GND (or to  $V_{IN}$ ). According to our knowledge, this is the

regular situation in the design of implantable devices. Note for example if any single failure may provoke leakages either to GND or  $V_{DD}$  (or any other fixed potential) the design of a safe device becomes virtually impossible because at least a common mode voltage is fixed to tissue.



**Figure 3.17** Switch A layout, High voltage transmission gate (Red), LS\_P (Blue), LS\_N (Green),  $2V_{CC}$  generator (Violet) and PADS (Orange).

### 3.3 Switches B and C

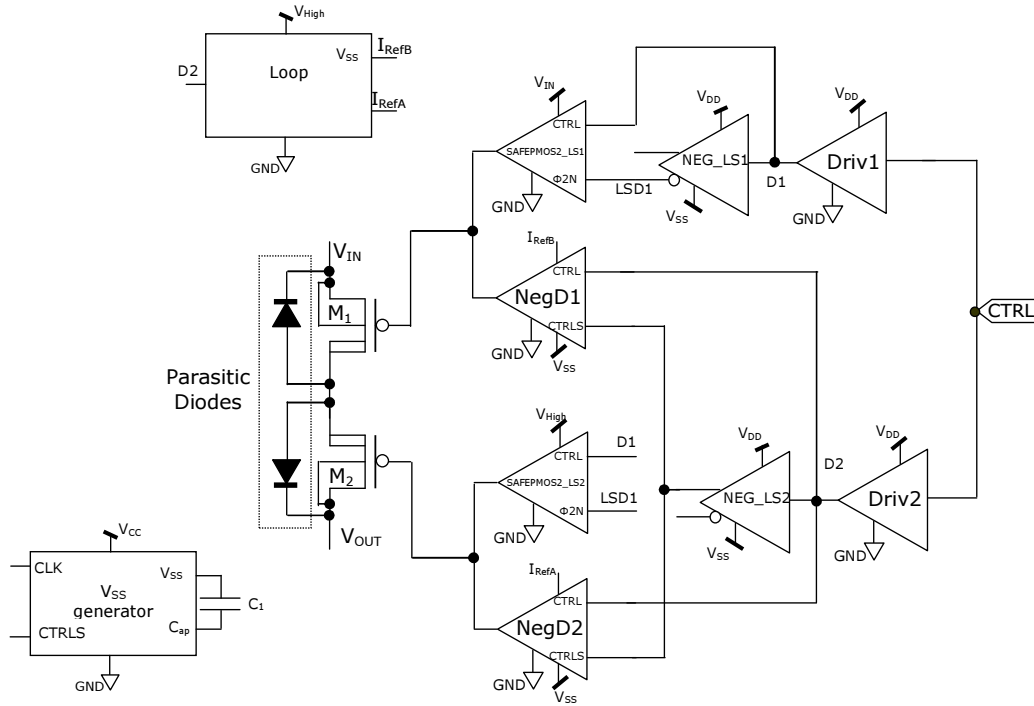
#### 3.3.1 Switch B design

In Figure 3.18 the switch B is shown, it is implemented with the following basic building blocks from section 3.1:

- Two Negative level-shifters (NEG\_LS1(2)) (section 1.3).
- Two SAFEPMOS2 level-shifters (SAFEPMOS2\_LS1(2)) (section 3.1.1.5).
- Two pvh transistors in series array (see section 2.2.1).
- Two standard drivers (Driv1(2)).
- Two negative drivers (NegD1(2)) (section 3.1.4).
- $V_{SS}$  generator (section 3.1.3).
- Over voltage  $V_{GS}$  protection circuit (Loop) (section 3.1.5)

Stimuli conduction takes place through transistors  $M_1$ ,  $M_2$ . CTRL is 0V when the switch is open (no stimulus), SAFEPMOS2\_LS1 connects  $M_1$ 's gate to  $V_{IN}$  and SAFEPMOS2\_LS2 connects  $M_2$ 's gate to  $V_{OUT}$ . Since  $V_{IN}$  and  $V_{OUT}$  may vary, only in this way it is guaranteed that  $V_{GS} = 0V$  to effectively open the pvh's thus the switch. In this case  $V_{SS} = GND$  and no static current is consumed. To closed (stimulus), CTRL is set to  $V_{CC}$ , the SAFEPMOS2\_LS1(2) goes to high impedance and both NegD connect the gates to either GND or  $V_{SS}$  to ensure  $M_1$ ,  $M_2$ , conduction. The negative voltage  $V_{SS}$  is necessary as the stimulus voltage can be very small (100mV), the  $V_{SS}$  charge pump provides the momentary negative voltage. On the other hand, when the stimulus voltage is very high (16V) and for example  $V_{SS} = -4V$  the  $V_{GS} \sim 20V$  may damage the gate oxide of  $M_1$ ,  $M_2$ . To overcome this problem, the subcircuit Loop was designed to generate a high enough current ( $I_{Ref}$ ) to close the path to  $V_{SS}$  in NegD when  $V_{High} > 12V$ . On this scheme  $V_{High}$  shall be connected to the highest of  $V_{IN}$  or  $V_{OUT}$ . In this way the circuit is protected in extreme voltages while ensuring low impedance when the stimulus voltage is very low. To sum up the complete switch has two states:

- Open state: When CTRL is 0V, SAFEPMOS2\_LS1 open  $M_1$  and SAFEPMOS2\_LS2 open  $M_2$ .  $V_{SS} = GND$  and no static current is consumed.
- Closed State: When CTRL is  $V_{CC}$ ,  $V_{SS}$  generator generates  $V_{SS} = -V_{CC}$ , NegD1 closes  $M_1$  and NegD2 closes  $M_2$ . If  $V_{High} > 12V$ ,  $I_{Ref}$  closes the path to  $V_{SS}$  and  $M_1$  and  $M_2$  gates are connected to GND, otherwise they are connected to  $V_{SS}$ .



**Figure 3.18 Switch B schematic,  $M_{1,2w/L}=40000\mu\text{m}/3\mu\text{m}$  .**

The switches B and have 8 PADS:

- CTRL: Opens (0) and closes ( $V_{CC}$ ) the switch.
- GND: Switch ground.
- $V_{CC}$ : Power supply.
- $C_{ap}$ :  $C_1$  external capacitor connection, for the  $V_{SS}$  generator.
- $V_{SS}$ :  $V_{SS}$  negative generated voltage.
- $V_{IN}$ : Switch input.
- $V_{OUT}$ : Switch output.
- $V_{High}$ : Reference voltage for the protection circuitry. Shall be connected to the largest voltage when stimulating.

In Figure 3.19 the complete layout of the switch B is shown. The same precautions as switch A were taken. The total occupied area is 2mm<sup>2</sup> (PADs included).

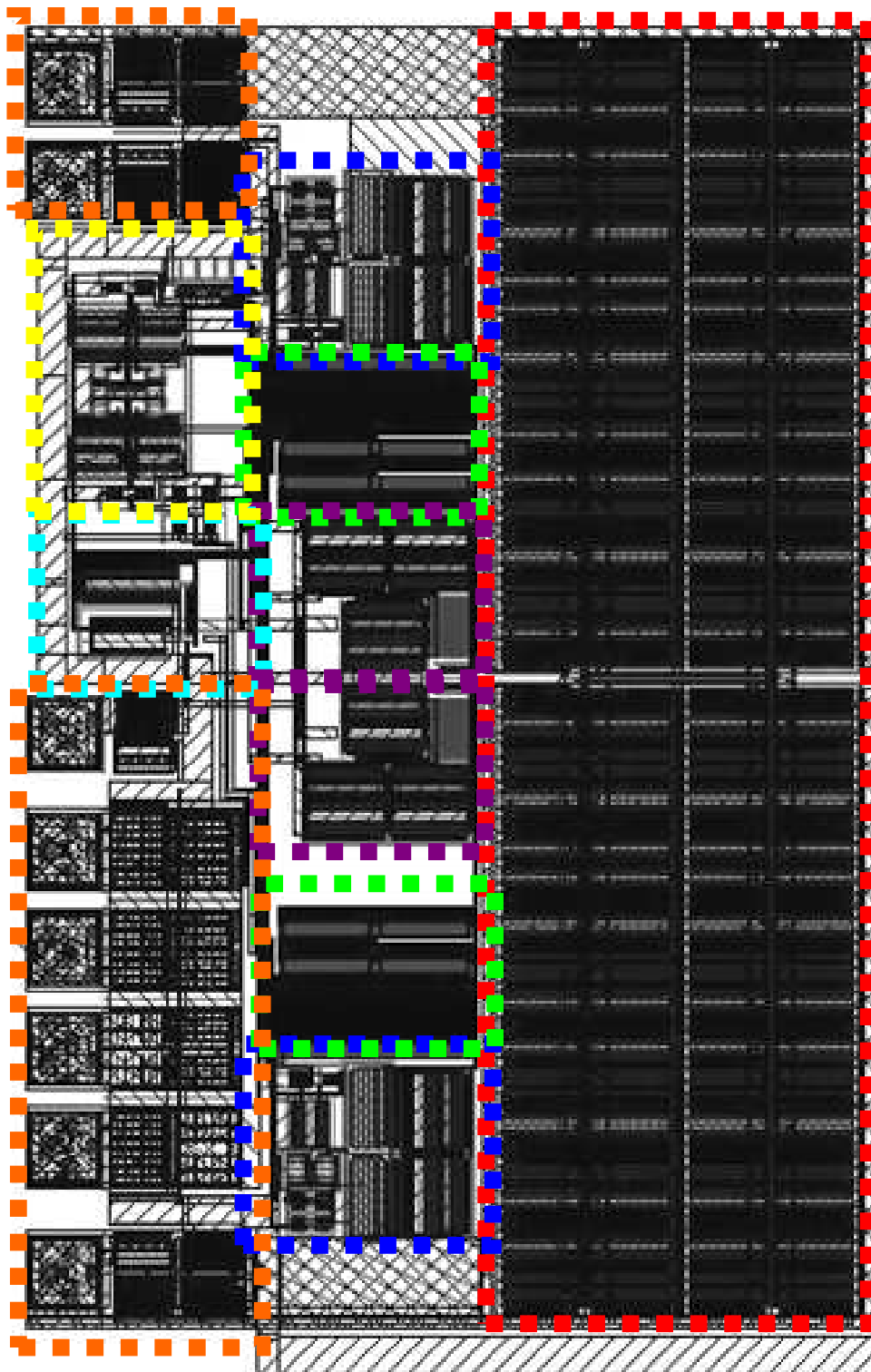
Safety Analysis:

In the circuit in Figure 3.18,  $M_1$ ,  $M_2$  and SAFEPMOS2\_LS1(2) are in direct contact to the electrode to tissue. Thus the safety analysis shall consider any possible failure on these circuit nodes when not stimulating. If  $M_2$ 's gate is punctured there is no problem. If a Drain to Source short circuit in  $M_1$ ,  $M_2$  may connect  $V_{IN}$  to  $V_{OUT}$  through  $M_1$ 's,  $M_2$ 's associated diodes.

**Thus the medical device manufacturer, that employs the Switches B, C shall guarantee that when not stimulating all the electrodes are either in high impedance, or connected to GND. GND shall be the common mode voltage for biological tissue.**

An overall conclusion is that the proposed Switch cannot guarantee by itself the safety of the device being implemented. In fact, at least  $V_{IN}$  to  $V_{OUT}$  connection in the case of failure cannot be avoided. From the implantable medical device perspective, the proposed switch provides a tool to design a safe device because any single failure may provoke only leakages to GND (or to  $V_{IN}$ ).

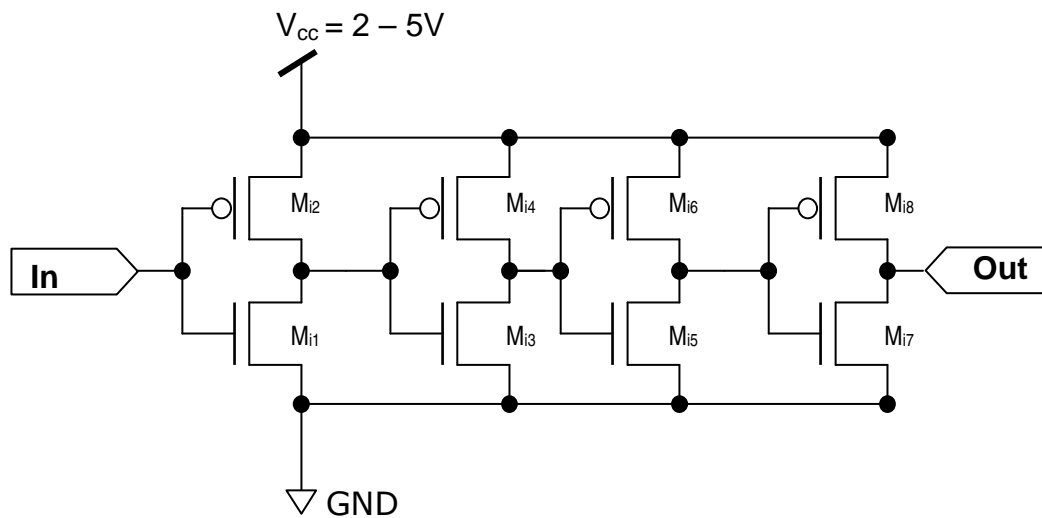




**Figure 3.19** Switch B layout, PHV opposing diodes array (Red), SLS (Blue), NegD (Green), LSN(Violet),  $V_{ss}$  generator (sky blue), loop (yellow) and PADS (Orange).

### 3.3.2 Switch C

Switch C is a very small variation of switch B, the difference is that DRV2 (see Figure 3.18) is changed by a chain of asymmetrical inverters [6][7], shown in Figure 3.20. This chain generates a significant delay only in the low to high transition (see Figure 3.21) making the NegD2 turning on slower and turning off faster. The delay was introduced to reduce the short-circuit current generated when the SAFEPMOS2\_LS is not yet off and the NegD2 is on. The short-circuit current is small but the proposed modification makes it even smaller.



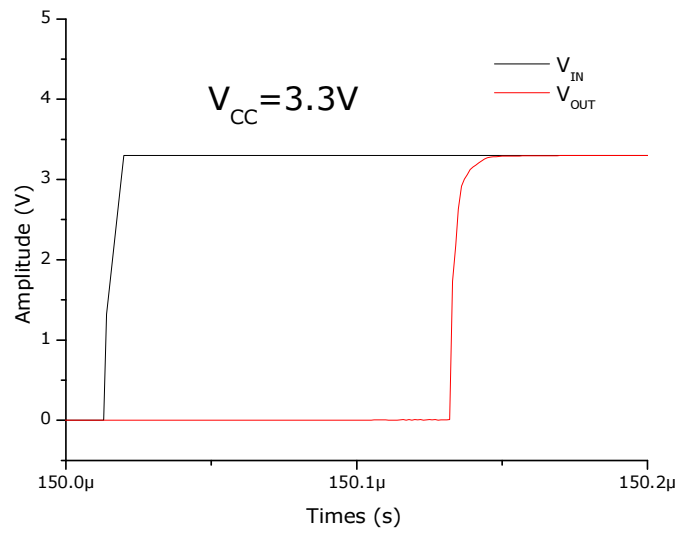
**Figure 3.20 Implemented asymmetrical inverter chain.**

In Table 3.10 a summary of transistor sizes are presented.

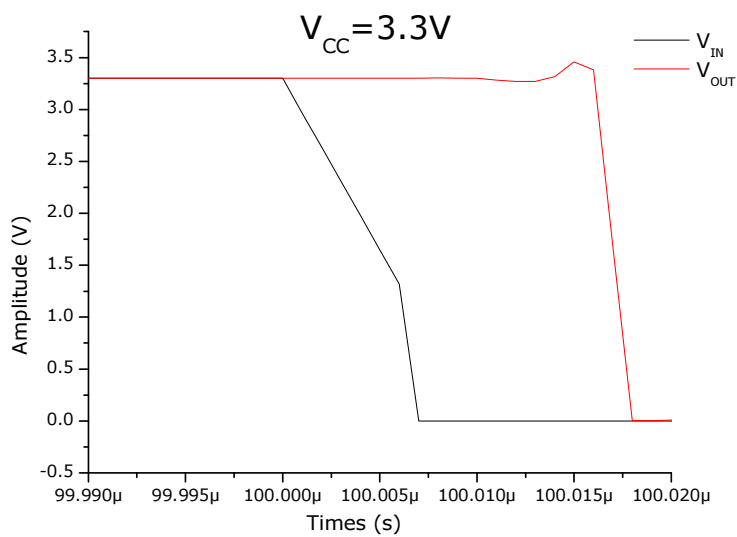
**Table 3.10 Asymmetrical inverter chain transistors dimensions.**

| Transistors   | W/L ( $\mu\text{m}/\mu\text{m}$ ) |
|---------------|-----------------------------------|
| $M_{1,2,3,6}$ | 10/3                              |
| $M_{4,5}$     | 4/30                              |
| $M_{7,8}$     | 20/3                              |

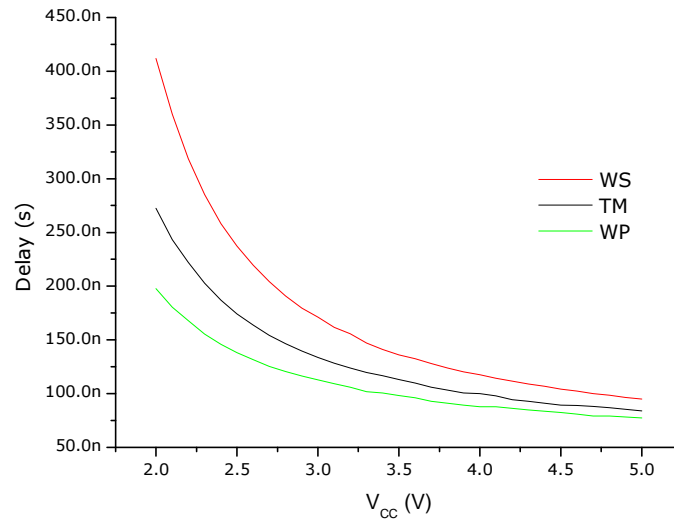
From Figure 3.21 to Figure 3.23 some simulation results of the asymmetrical inverter chain can be shown. Note delay is only generated in the low to high transition.



**Figure 3.21 Simulated asymmetrical inverters chain rising edge.**



**Figure 3.22 Simulated asymmetrical inverters chain falling edge.**



**Figure 3.23 Simulated delay vs V<sub>cc</sub>.**

It should be pointed that, from simulations and measurements, no significant difference was observed between both circuits (Switch B and C). However both were included in the available 10mm<sup>2</sup> and in the following chapter, both were measured like different circuits.

## 4 Measurements

The circuits were fabricated and measured, to compare their performance and select the best option for a future project. A first conclusion is that the three circuits worked properly, switching the load as expected. In this chapter, the full measurement result of switches A, B and C, are presented. Switch on resistance, transient response, power consumption, leakages, crosstalk, charge injection and ESD robustness, measured characteristics will be shown in this order.

### 4.1 Switch impedance (RON)

#### 4.1.1 $R_{ON}$ with $2V_{CC}$ (switch A) and $V_{SS}$ (switch B, C)

In Figure 4.1 the setup used to measure  $R_{ON}$  is shown ( $2V_{CC}$  and  $V_{SS}$  were generated with the aid of an external supply).  $R_{ON}$  measurements were obtained by sweeping  $V_{Stimuli}$  from 100mV to 16V for  $V_{CC} = 2, 2.4, 3.3, 4$  and 5V, the measured values are shown from Figure 4.2 to Figure 4.9.

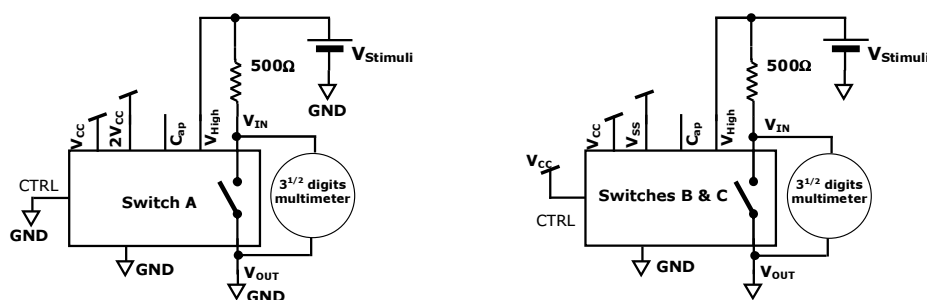
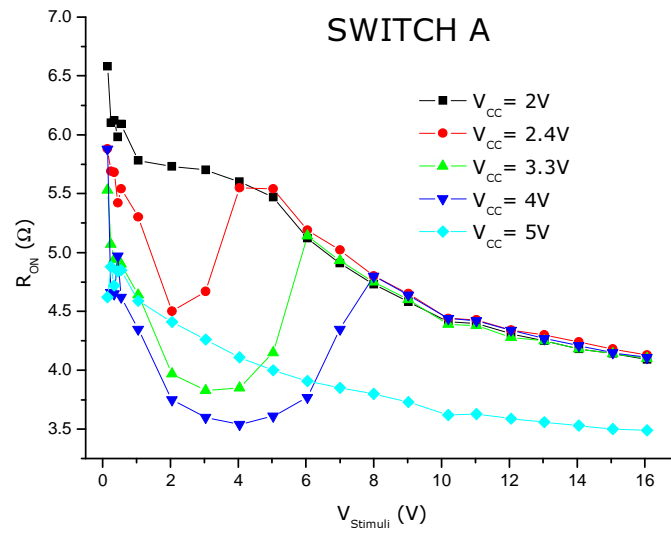
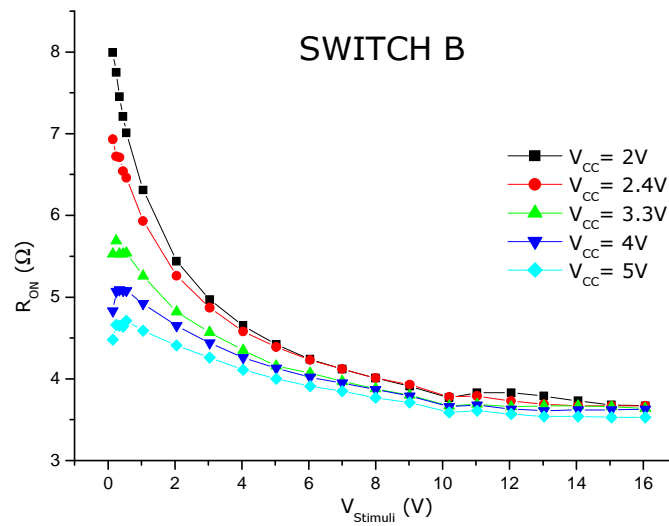


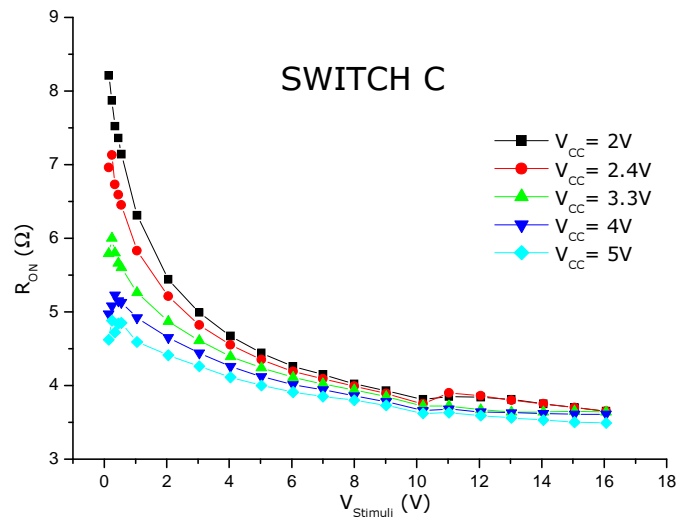
Figure 4.1  $R_{ON}$  measurement circuit configuration.



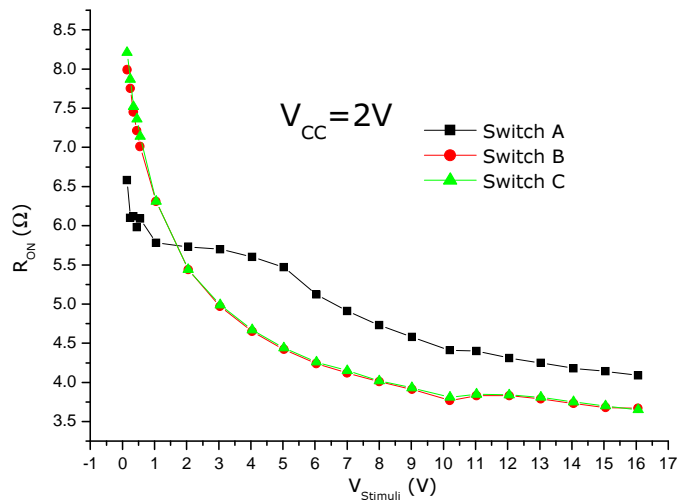
**Figure 4.2 Switch A  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ . The voltage doubler is supposed to generate  $2V_{CC}$  voltage.**



**Figure 4.3 Switch B  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ . The negative voltage generator is supposed to provide  $V_{SS} = (-V_{CC})$  voltage.**



**Figure 4.4 Switch C  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ . The negative voltage generator is supposed to provide  $V_{SS} = (-V_{CC})$  voltage.**



**Figure 4.5 Switch A, B and C  $R_{ON}$  comparison, for  $V_{CC} = 2V$ .**

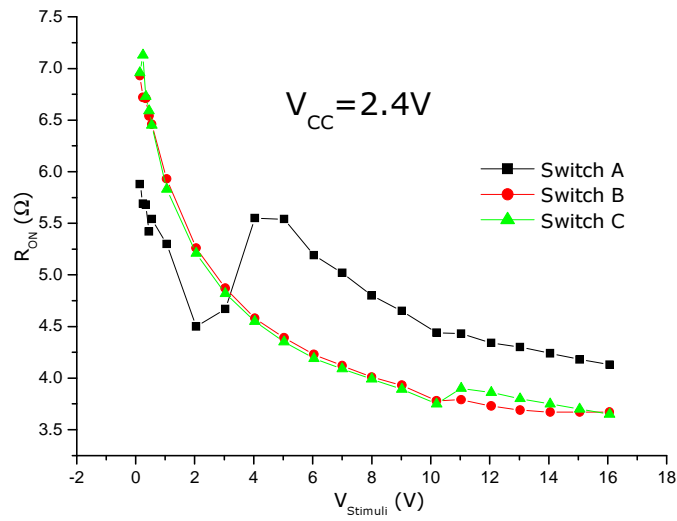


Figure 4.6 Switch A, B and C  $R_{ON}$  comparison, for  $V_{CC} = 2.4V$ .

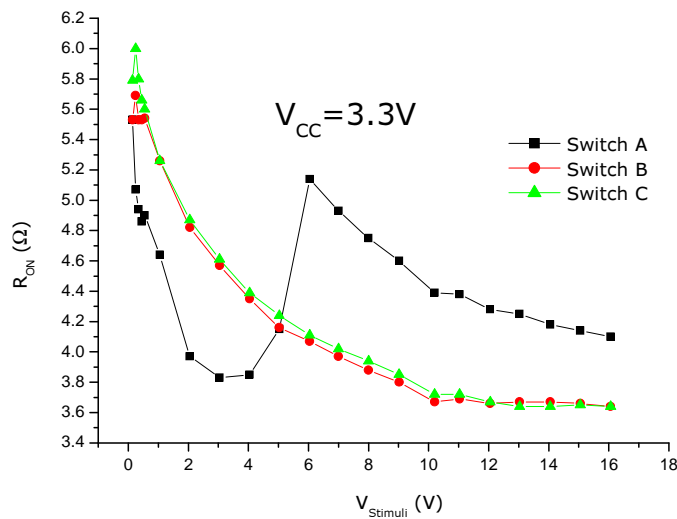
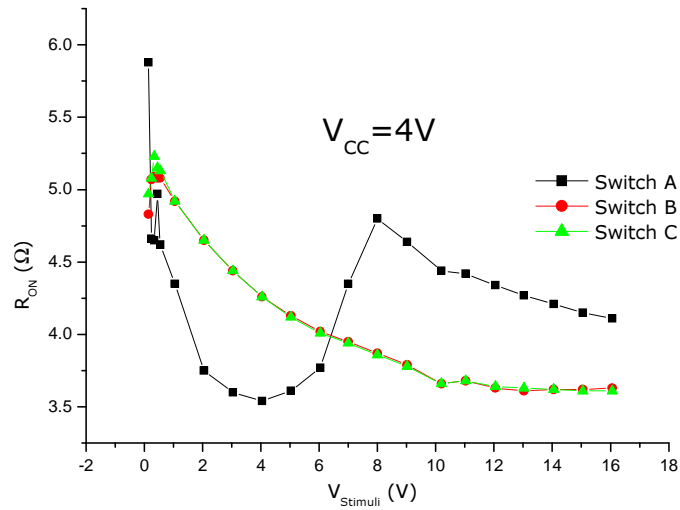
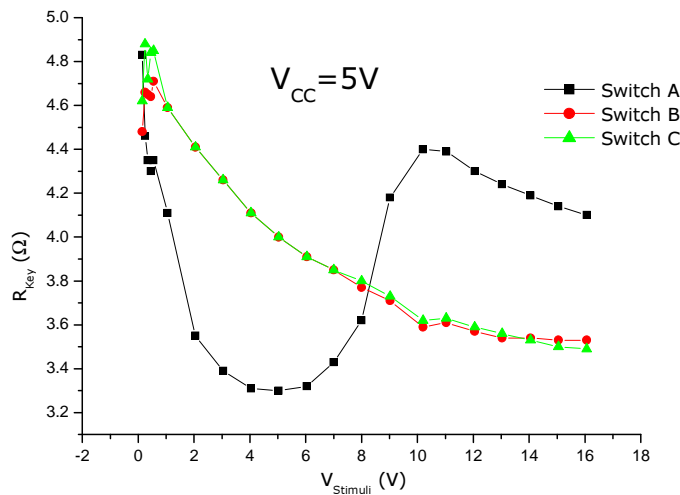


Figure 4.7 Switch A, B and C  $R_{ON}$  comparison, for  $V_{CC} = 3.3V$ .





**Figure 4.8 Switch A, B and C  $R_{ON}$  comparison, for  $V_{CC} = 4V$ .**



**Figure 4.9 Switch A, B and C  $R_{ON}$  comparison, for  $V_{CC} = 5V$ .**

The measured  $R_{ON}$  of switches A, B and C are within expected values, considering both MOSFET and wires resistance, for all  $V_{Stimuli}$  and  $V_{CC}$  ranges. The result tough exceeds a bit the target  $5\Omega$  value for the lower  $V_{Stimuli}$ , it is assumed to comply with specifications in section 1.3.

### 4.1.2 $R_{ON}$ without charge pump: without $2V_{CC}$ (Switch A) or $V_{SS}$ (Switch B, C).

In some cases, the user may suppress the external capacitor (thus the charge pump) for the sake of a simpler circuit, if no low stimulus voltages will be required. In Figure 4.10 the setup used to measure  $R_{ON}$  is shown ( $2V_{CC}$  connected to  $V_{CC}$  and  $V_{SS}$  connected to ground).  $R_{ON}$  measurement was obtained sweeping  $V_{Stimuli}$  from 100mV to 16V, for  $V_{CC}$  2, 2.4, 3.3, 4 and 5V, the measured result are shown from Figure 4.11 to Figure 4.13.

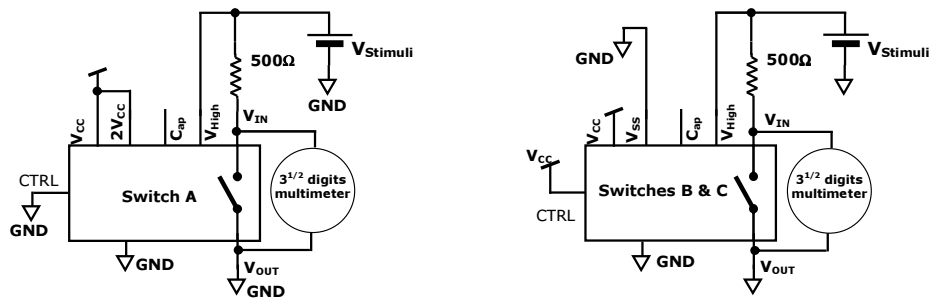


Figure 4.10  $R_{ON}$  measurement circuit configuration.

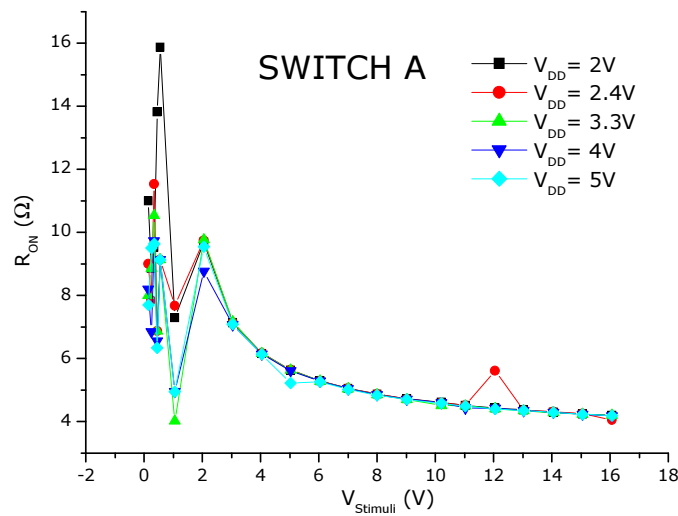
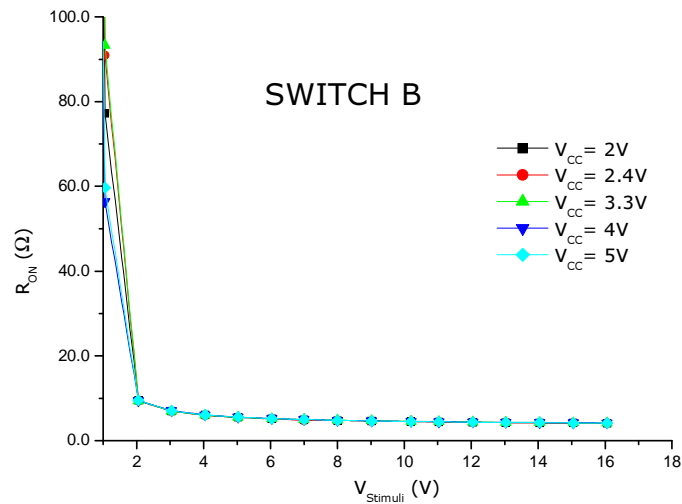
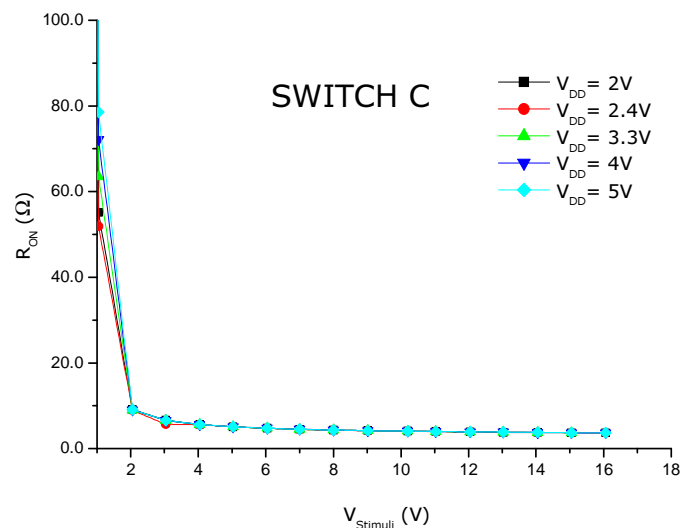


Figure 4.11 Switch A  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ .  $2V_{CC}$  connected to  $V_{CC}$



**Figure 4.12 Switch B  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ .  $V_{SS}$  connected to ground**



**Figure 4.13 Switch C  $R_{ON}$  for different stimuli voltage  $V_{stimuli}$  and supply voltage  $V_{CC}$ .  $V_{SS}$  connected to ground**

As expected the  $R_{ON}$  impedances of switches B and C get larger when  $V_{Stimuli}$  is low (see Figure 4.12 and Figure 4.13) without the  $V_{SS}$  generator, because the gates of the main PMOS are put to 0V to close the switches, making  $V_{GS}$  very small though making the transistor impedance large. For switch A the  $R_{ON}$  impedance is quite low in all  $V_{Stimuli}$  regions because of the high voltage transmission gate configuration (see Figure 3.15), but not as low as specified in section 1.3  $V_{Stimuli}$  for certain values.

## 4.2 Voltage stimuli with $2V_{CC}$ (switch A) and $V_{SS}$ (switches B, C)

In Figure 4.14 the setup used for the measurement of voltage stimuli response of the three switches is shown. The measurement was done with  $V_{Stimuli}$  100mV, 5V and 16V and  $V_{CC}$  2V, 2.8V and 5V, turning on and off the switches with a 10kHz, 50% duty cycle, square wave.

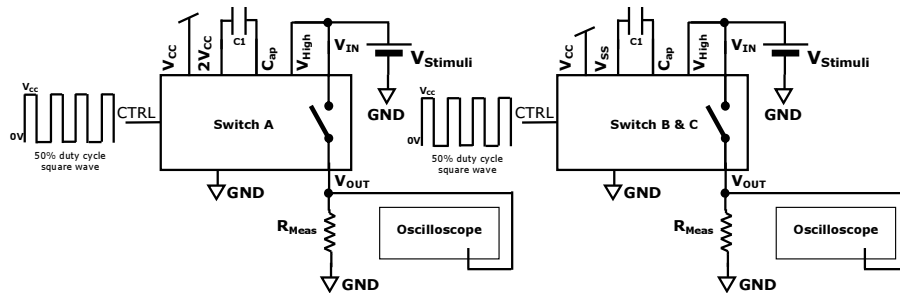


Figure 4.14 Voltage stimuli measurement setup,  $R_{Meas}=500\Omega$ .

From Figure 4.15 to Figure 4.23 the measurement results of voltage stimuli are shown.

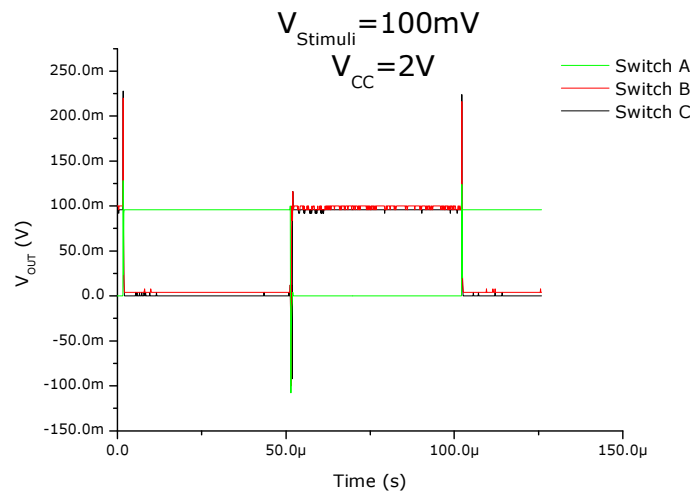
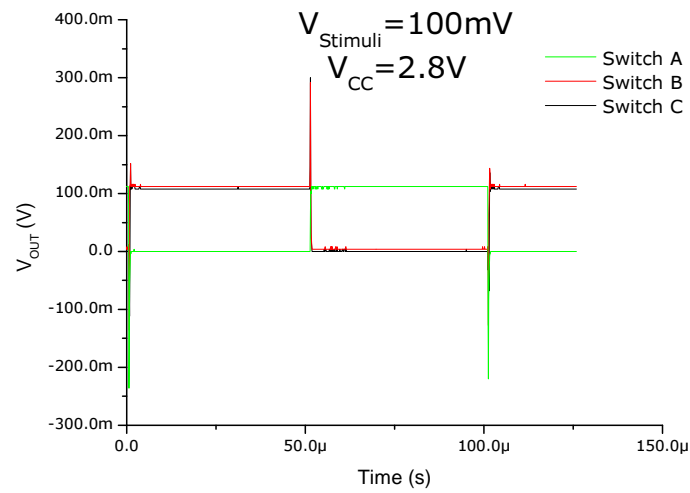
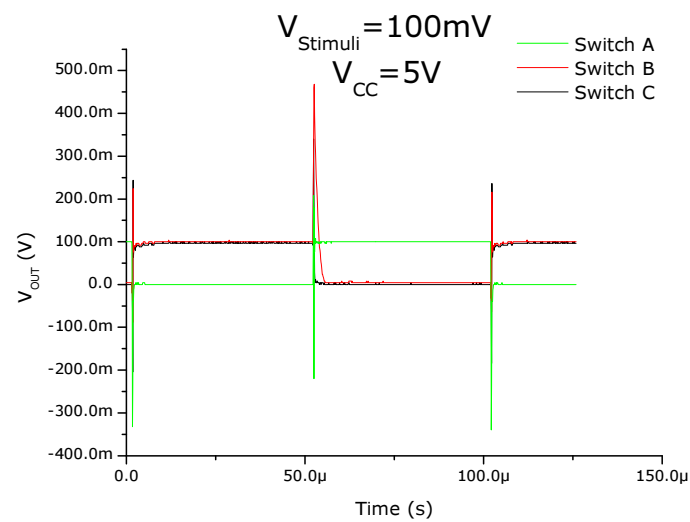


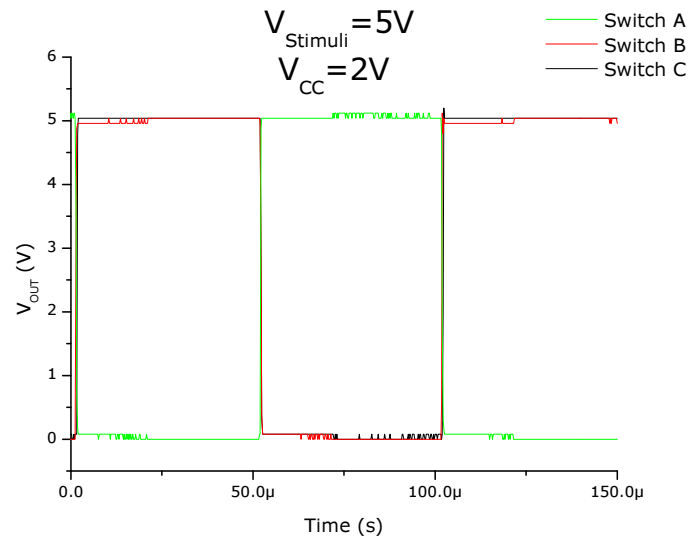
Figure 4.15 Switches A,B and C voltage stimuli response for  $V_{Stimuli}=100mV$  and  $V_{CC}=2V$ .



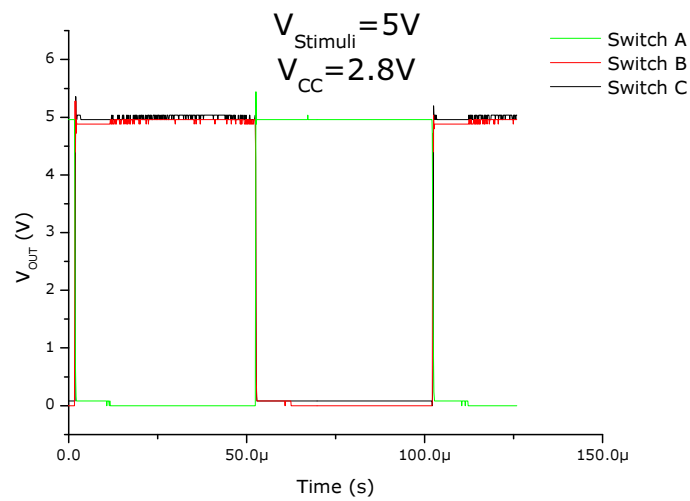
**Figure 4.16** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 100mV$  and  $V_{CC} = 2.8V$ .



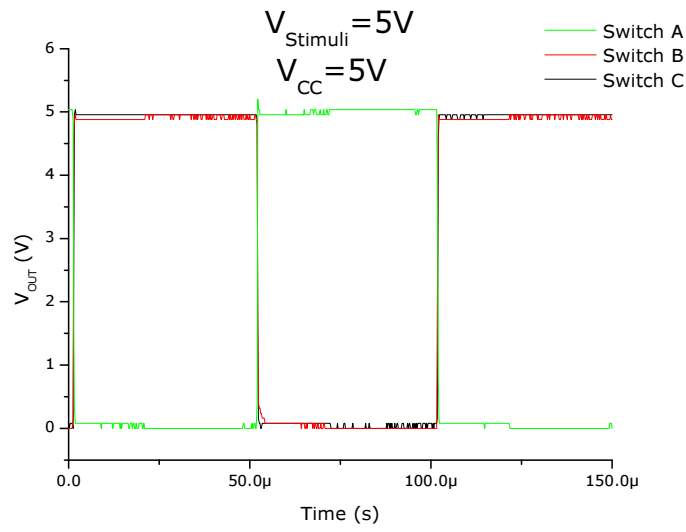
**Figure 4.17** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 100mV$  and  $V_{CC} = 5V$ .



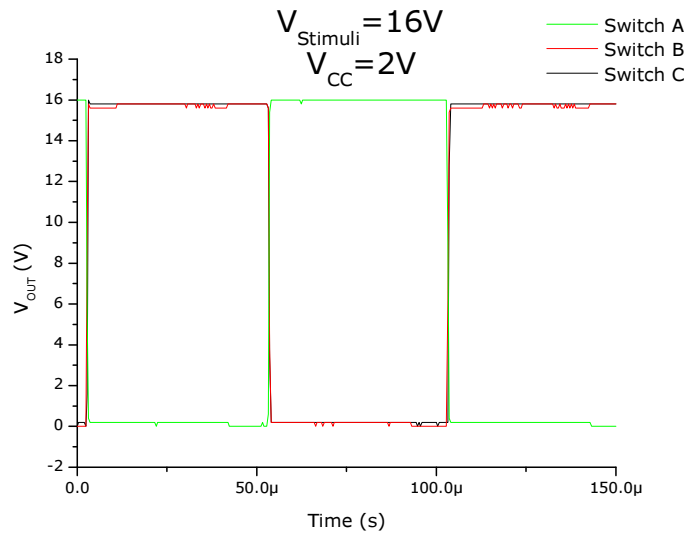
**Figure 4.18** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 5V$  and  $V_{CC} = 2V$ .



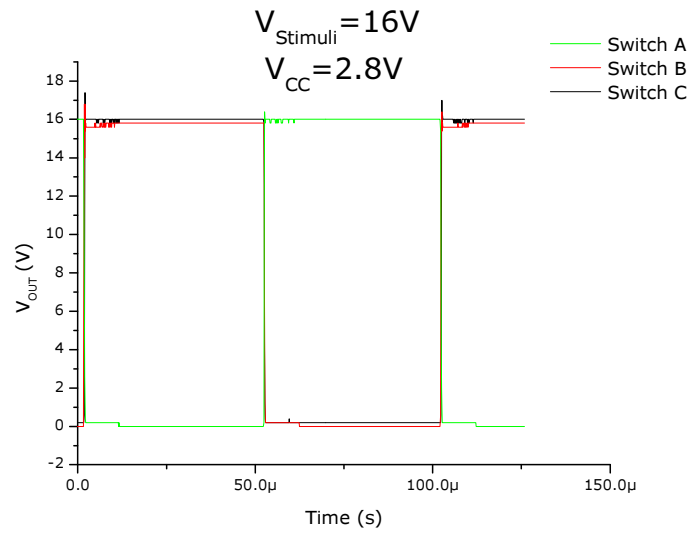
**Figure 4.19** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 5V$  and  $V_{CC} = 2.8V$ .



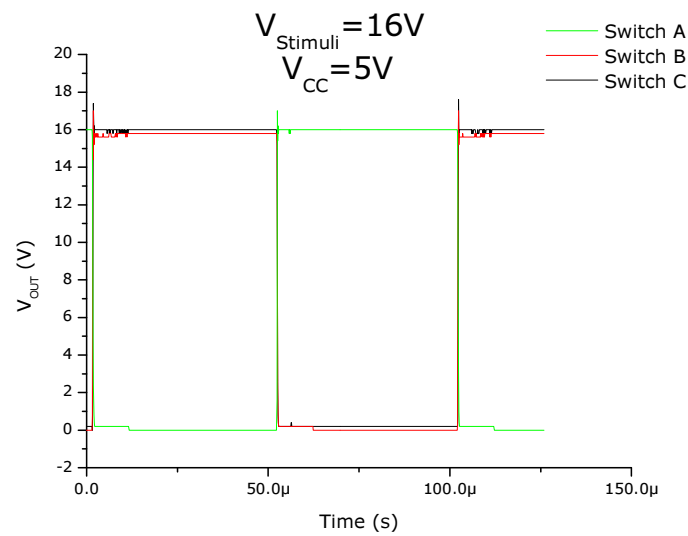
**Figure 4.20** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 5V$  and  $V_{CC} = 5V$ .



**Figure 4.21** Switches A,B and C voltage stimuli response for  $V_{Stimuli} = 16V$  and  $V_{CC} = 2V$ .



**Figure 4.22 Switches A,B and C voltage stimuli response for  $V_{stimuli} = 16V$  and  $V_{CC} = 2.8V$ .**



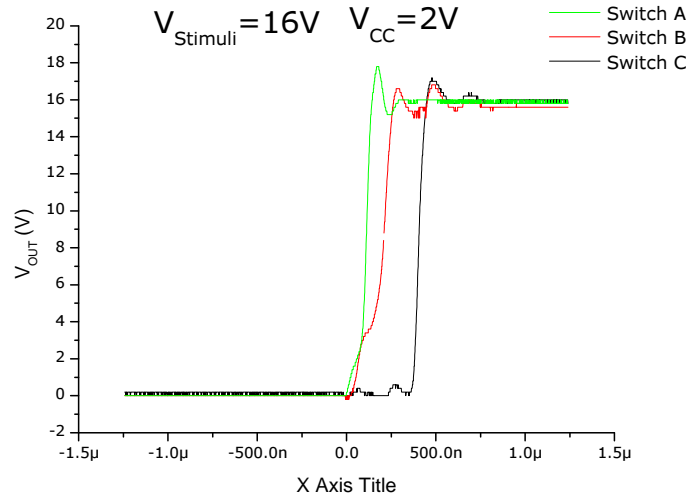
**Figure 4.23 Switches A,B and C voltage stimuli response for  $V_{stimuli} = 16V$  and  $V_{CC} = 5V$ .**

As specified in section 1.3, the three designed switches are capable of delivering stimuli pulses from 100mV to 16V, for  $V_{CC}$  ranging from 2V to 5V.

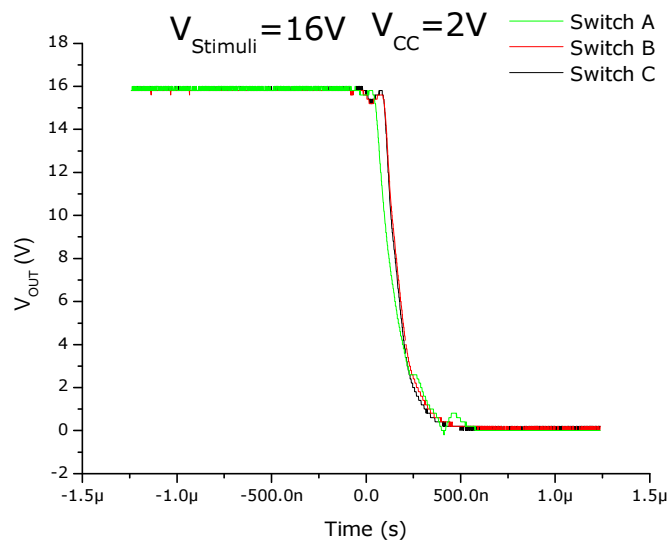


### 4.3 ON/OFF time

ON/OFF time was measured for voltage stimuli application, using the setup of Figure 4.14, for the three switches. In Figure 4.24 and Figure 4.25 a rising and falling edge of the three switches is shown, all the measured delays were below 500ns complying with specified in section 1.3.



**Figure 4.24 Measured rising edge transient response, for  $V_{CC}$  2V and  $V_{Stimuli}$  16V.**



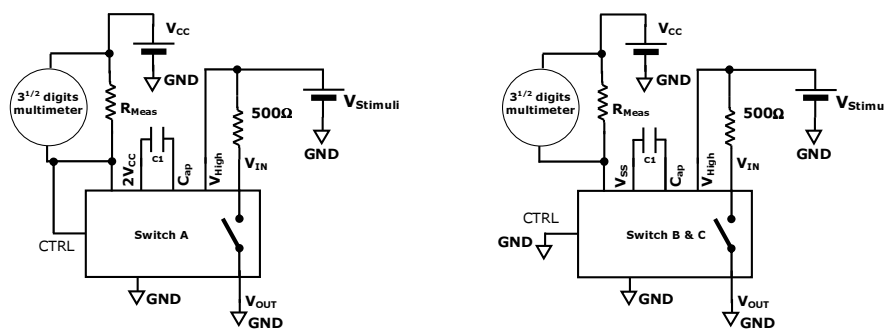
**Figure 4.25 Measured falling edge transient response, for  $V_{CC}$  2V and  $V_{Stimuli}$  16V.**

As expected the rising edge of the switch C is slower than Switch B due to the adding off asymmetrical inverters that affect only one edge. The 200n delay is within the expected values as shown in Figure 3.23.

## 4.4 Power consumption

### 4.4.1 Static power consumption

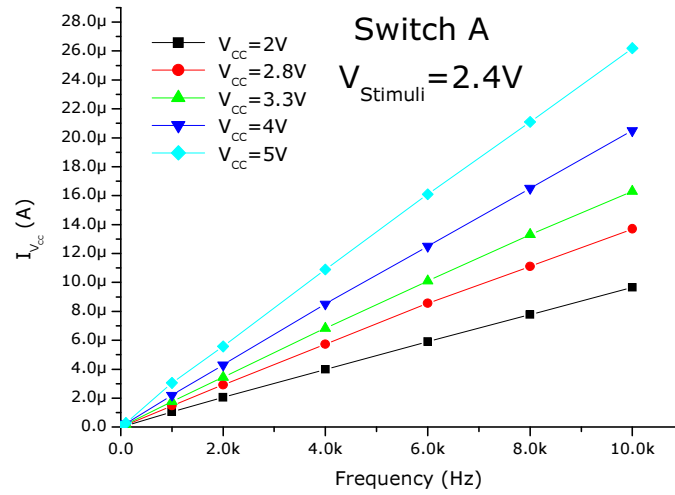
$V_{CC}$  current was measured for the switches opened for  $V_{CC}$ , 2, 2.8, 3.3, 4 and 5V and  $V_{Stimuli}$  2.4V and 16V. The experimental setup for this measure is shown in Figure 4.26.



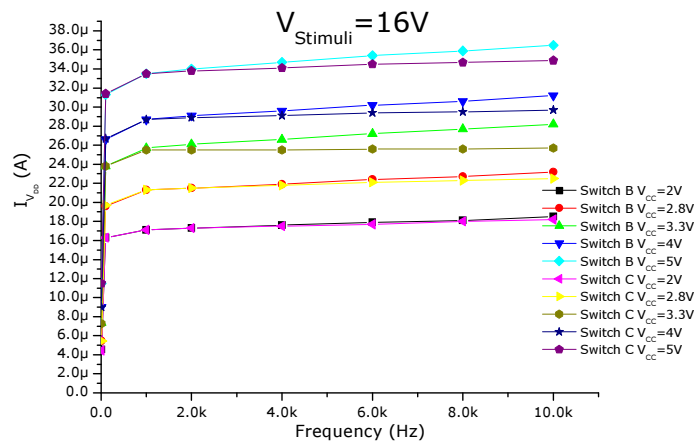
**Figure 4.26 Static power consumption measurement setup,  $R_{Meas}=1M\Omega$ .**

In all cases for the three switches (A, B and C), static consumption was below 5nA, complying with specifications in section 1.3.

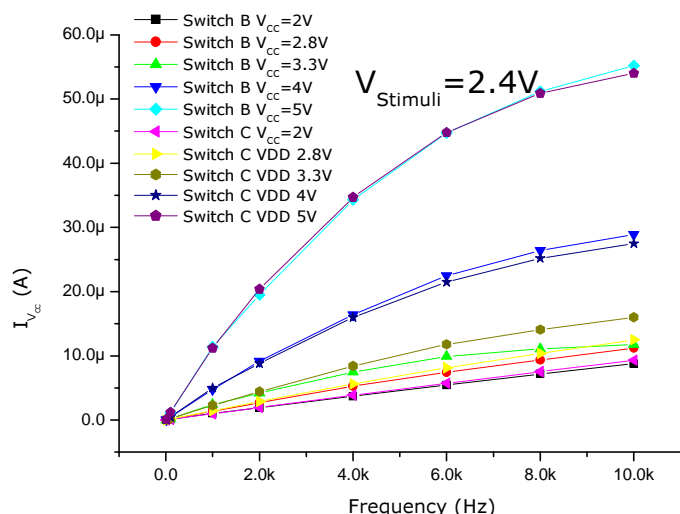




**Figure 4.29 Switch A dynamic power consumption measurement for  $V_{Stimuli} = 2.4V$ .**



**Figure 4.30 Switches B and C dynamic power consumption measurement for  $V_{Stimuli} = 16V$ .**

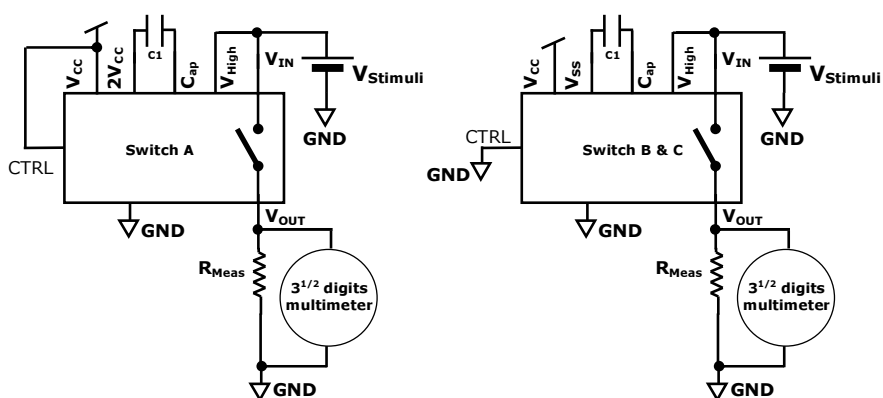


**Figure 4.31 Switches B and C dynamic power consumption measurement for  $V_{Stimuli} = 2.4V$ .**

Note that the dynamic power consumption of Switch A is approximately proportional to frequency, indicating that power consumption is due to the repetitive charge-discharge of gate and parasitic capacitors. In the case of switches B and C, power consumption has a fixed floor for large  $V_{Stimuli}$  values corresponding to the current through the protective loop of section 3.1.5.

## 4.5 Leakage currents

Leakage currents were measured for the switches opened,  $V_{Stimuli}$  16V and  $V_{CC}$  2, 2.8, 3.3, 4 and 5V, the measurement setup is shown in Figure 4.32.



**Figure 4.32 Leakage current measurement setup,  $R_{Meas} = 1M\Omega$ .**

The measured leakage current for all cases was below 1nA (in the precision boundaries of the setup of Fig.4.20).

## 4.6 Crosstalk

An implantable medical device generally has more than one stimulus channels and when one channel switch closes (stimuli pass) the others channel switches opens. Because of the conductive tissue, an electric pulse in an electrode causes also a voltage pulse in the other ones connected near the former. If the switches that block current flow from/to electrodes were ideal, no current should exist trough them when open. But real switches allow some current to pass, this phenomenon is called crosstalk. In Figure 4.33 the setup used to measure crosstalk is shown, with  $V_{Stimuli}$  0 and 16V for  $V_{CC}$  2.8V. The measurement results are shown from Figure 4.34 to Figure 4.37.

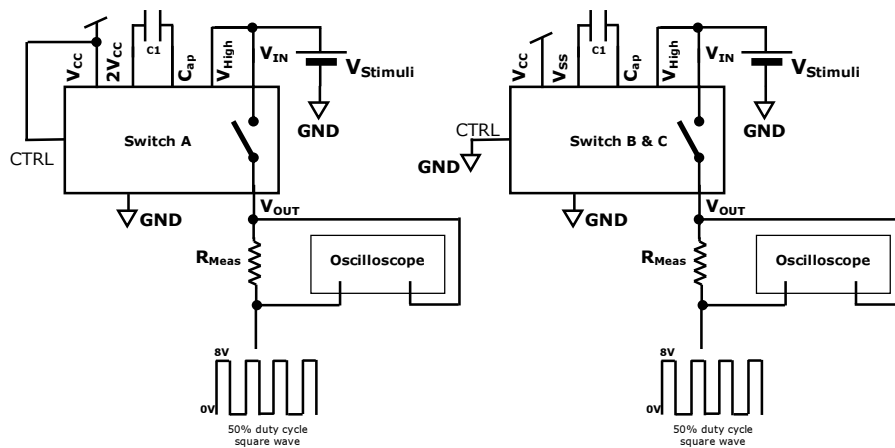
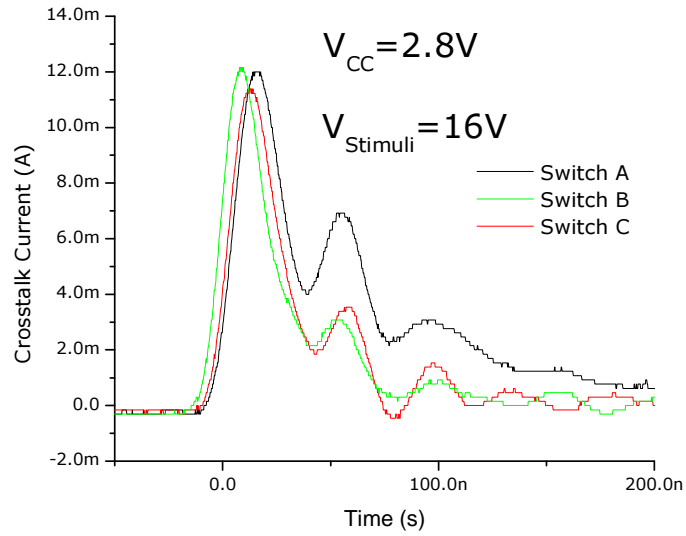
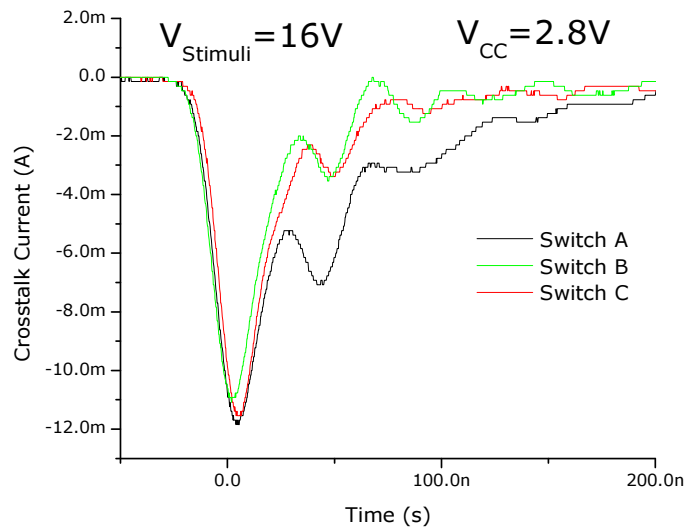


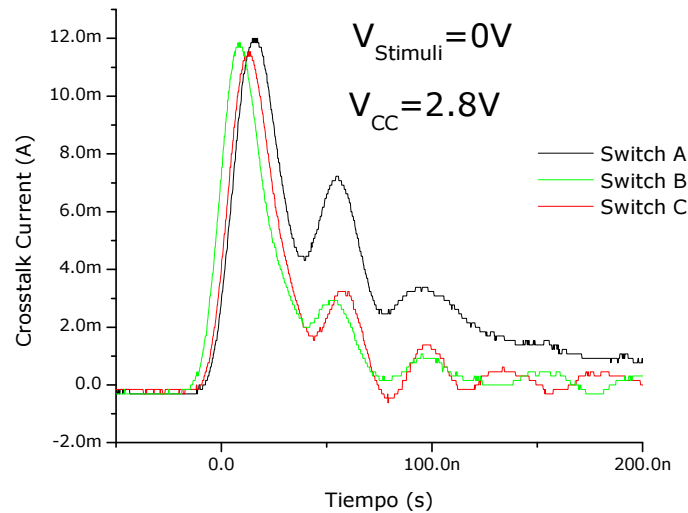
Figure 4.33 Crosstalk measurement setup.



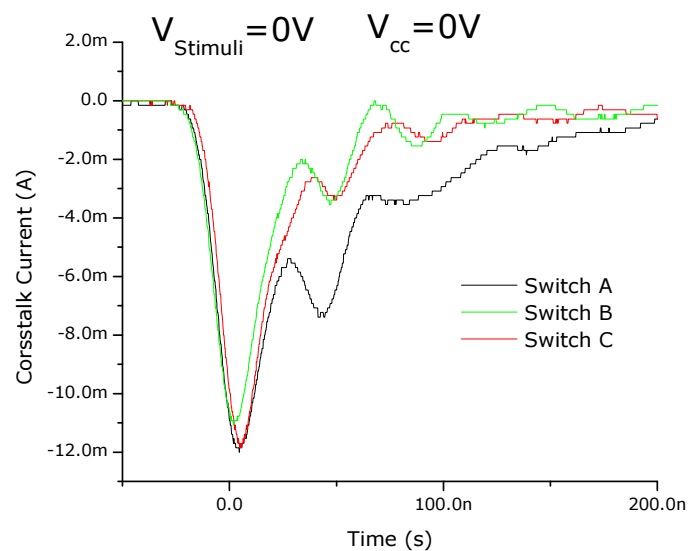
**Figure 4.34** Rising edge crosstalk current, for  $V_{Stimuli} = 16V$  and  $V_{CC} = 2.8V$ .



**Figure 4.35** Falling edge crosstalk current, for  $V_{Stimuli} = 16V$  and  $V_{CC} = 2.8V$ .



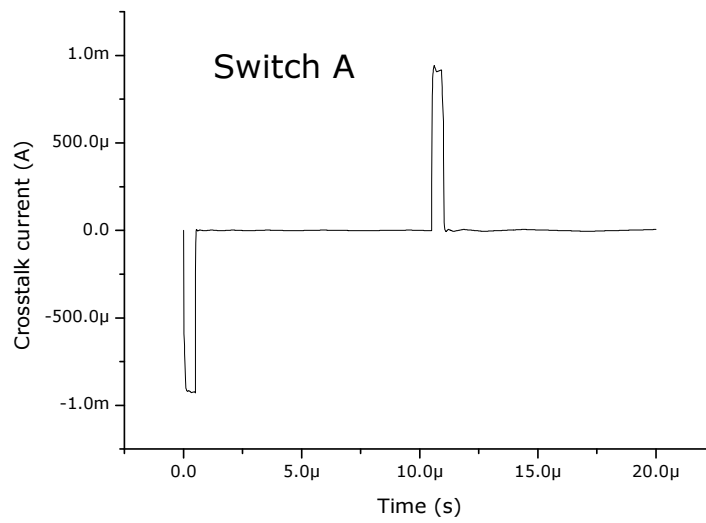
**Figure 4.36 Rising edge crosstalk current, for  $V_{Stimuli}=0V$  and  $V_{CC}=2.8V$**



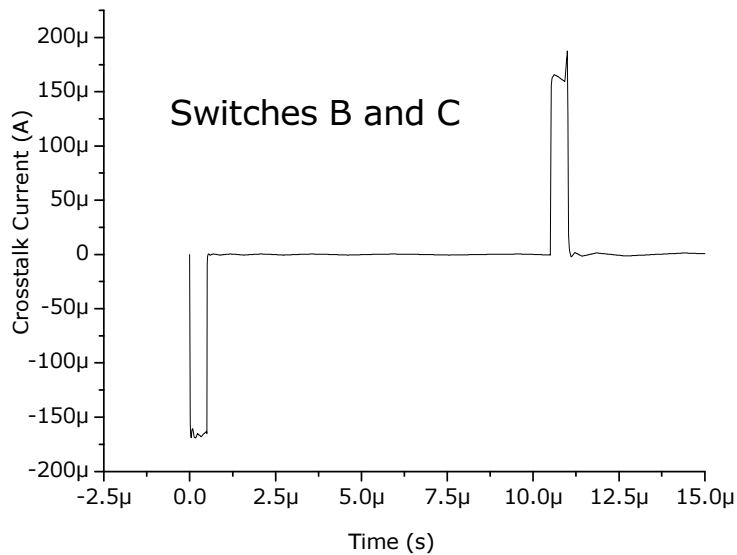
**Figure 4.37 Falling edge crosstalk current, for  $V_{Stimuli}=0V$  and  $V_{CC}=2.8V$**

In all cases, the integrated charge going into the switches is approximately 0.6nC for the switch A and 0.3nC for switches B and C, this charges includes the charge introduced by the oscilloscope probes. The oscilloscopes charge was measured in 0.2nC, so the actual charge going into the switches is 0.4nC for switch A and 0.1nC for switches B and C. To compare, in Figure 4.38 and Figure 4.39 the simulated crosstalk current is shown, the charge going into the switches is 0.5nC for switch A and 0.075nC for switches B and C. It should be highlighted the accuracy of the simulations when compared to measured results, as well as the fact that crosstalk resulted 4 times less in the case of switches B and C.





**Figure 4.38 Switch A simulated crosstalk current.**



**Figure 4.39 Switches B and C simulated crosstalk current.**

Switches B and C present a much smaller crosstalk, because the switches are close by connecting  $V_{OUT}$  with the gate of transistor  $M_2$  (see Figure 3.18), instead of switch A that connects  $M_2$  gate to 0V (see Figure 3.15).

## 4.7 Current stimuli (charge injection)

In Figure 4.40 the setup used for measuring current stimuli response of the three switches is shown. The idea is to use the designed switches to connect/disconnect a current source to tissue instead of a voltage, which is a usual configuration in medical devices. The current source was implemented with an opamp and a NPN bipolar transistor and switches were turned on and off with and 10kHz 50% duty cycle square wave.

In Fig.4.28  $R_{Meas}$  emulates the tissue load. In the case of an ideal current source, the current through the load shall be an ideal square current pulse. But because of charge injection at the switch turn on/off, a undesired current peak can be observed.

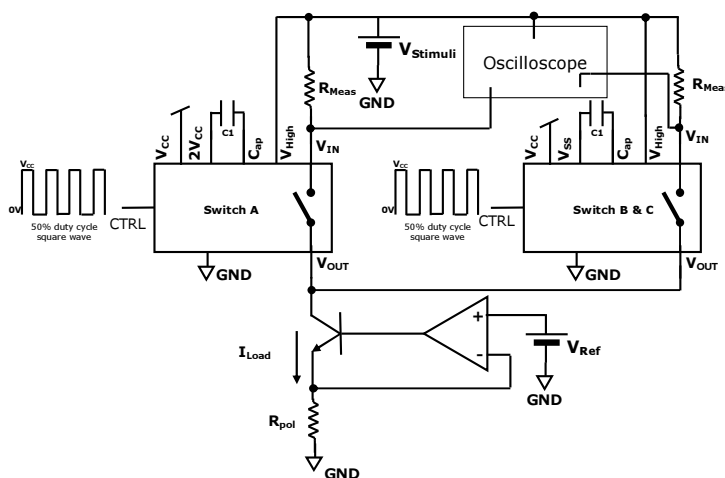
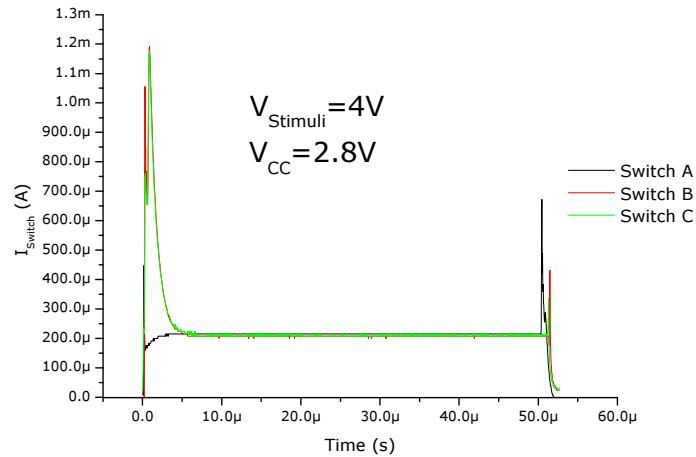


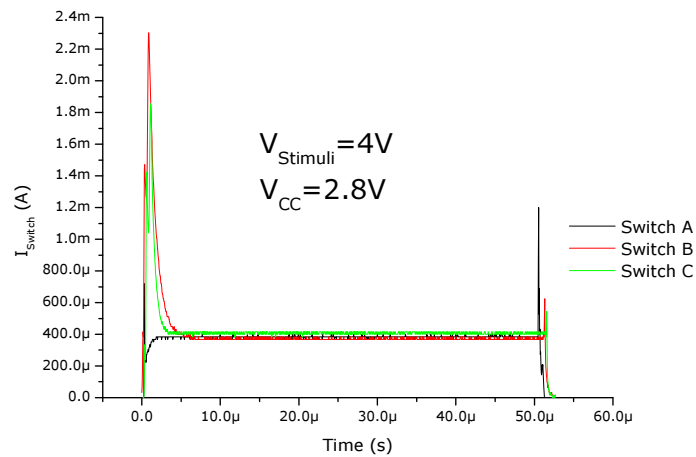
Figure 4.40 Current stimuli measurement setup.

### 4.7.1 Current stimuli sweep with $2V_{CC}$ (switch A) and $V_{SS}$ (switches B, C)

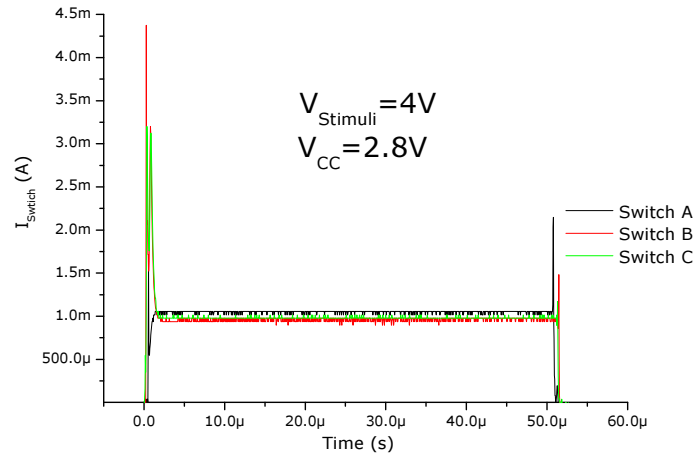
From Figure 4.41 to Figure 4.45 the measured transient current pulses when sweeping the stimuli current (see Figure 4.40) from  $200\mu\text{A}$  to  $10\text{mA}$ , for  $V_{\text{Stimuli}} = 4\text{V}$  and  $V_{CC} = 2.8\text{V}$  are shown.



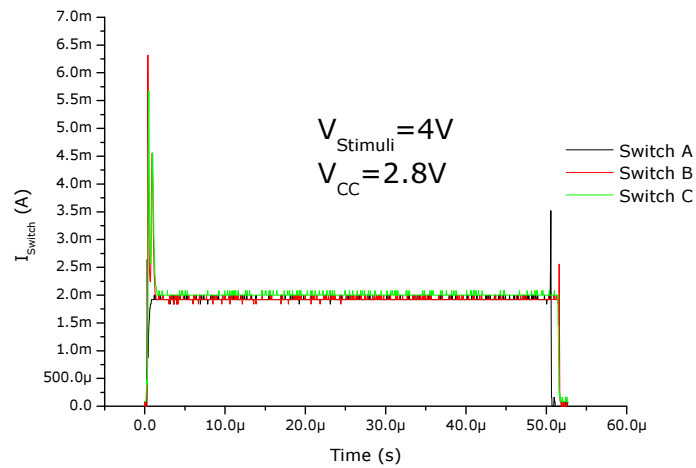
**Figure 4.41 Measured  $200\mu\text{A}$  current stimulus pulse for  $V_{\text{Stimuli}} = 4\text{V}$  and  $V_{CC} = 2.8\text{V}$ .**



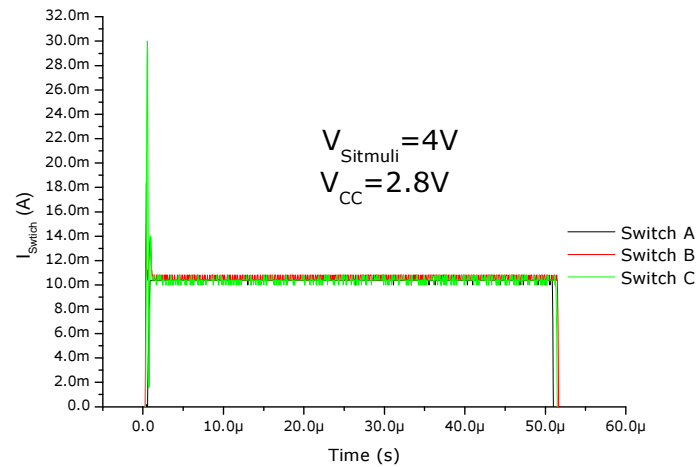
**Figure 4.42 Measured  $400\mu\text{A}$  current stimulus pulse for  $V_{\text{Stimuli}} = 4\text{V}$  and  $V_{CC} = 2.8\text{V}$ .**



**Figure 4.43 Measured 1mA current stimulus pulse for  $V_{\text{Stimuli}}=4\text{V}$  and  $V_{\text{CC}}=2.8\text{V}$ .**



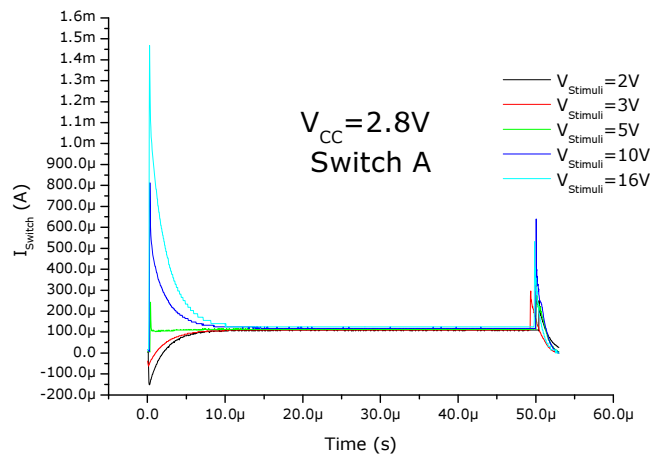
**Figure 4.44 Measured 2mA current stimulus pulse for  $V_{\text{Stimuli}}=4\text{V}$  and  $V_{\text{CC}}=2.8\text{V}$ .**



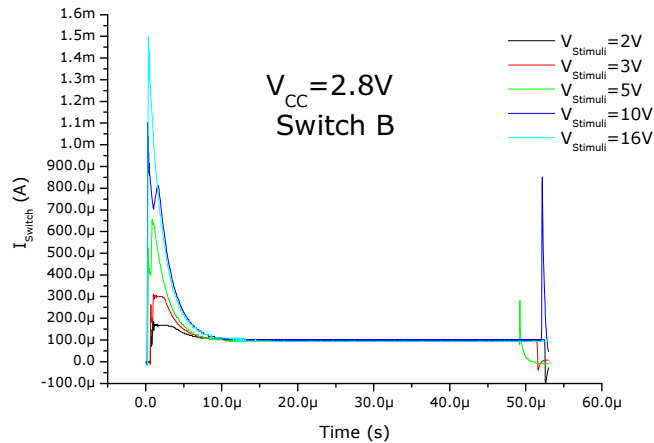
**Figure 4.45 Measured 10mA current stimulus pulse for  $V_{stimuli}=4V$  and  $V_{CC}=2.8V$ .**

#### 4.7.2 $V_{stimuli}$ sweep with $2V_{CC}$ (switch A) and $V_{SS}$ (switches B, C)

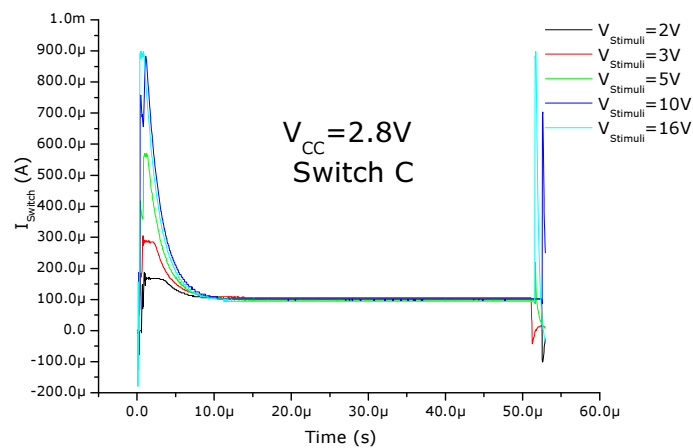
From Figure 4.46 to Figure 4.48 the measured transient current pulses when sweeping  $V_{stimuli}$  (see Figure 4.40) from 2V to 16V, for a load current of  $100\mu A$  and  $V_{CC} 2.8V$ , are shown.



**Figure 4.46 Switch A measured  $100\mu A$  current stimulus pulse for  $V_{stimuli}$  from 2V to 16V and  $V_{CC}=2.8V$ .**

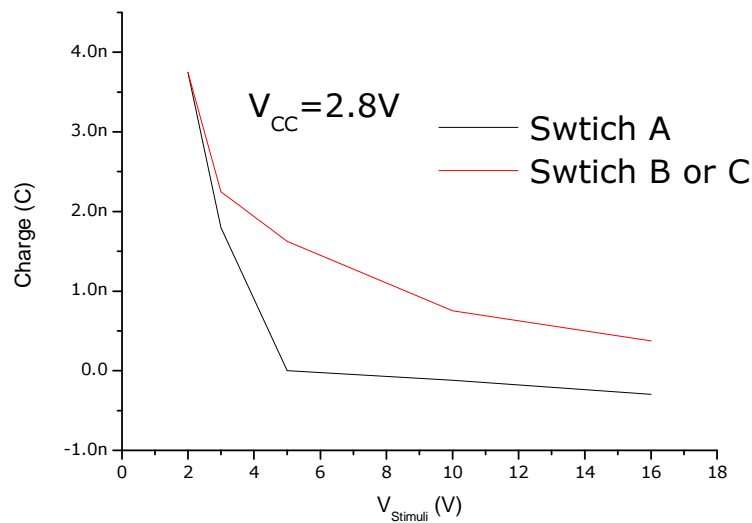


**Figure 4.47 Switch B measured 100 $\mu$ A current stimulus pulse for  $V_{\text{Stimuli}}$  from 2V to 16V and  $V_{CC} = 2.8V$ .**



**Figure 4.48 Switch C measured 100 $\mu$ A current stimulus pulse for  $V_{\text{Stimuli}}$  from 2V to 16V and  $V_{CC} = 2.8V$ .**

As specified in section 1.3, the three designed switches are capable of delivering stimuli pulses from 10 $\mu$ A to 30mA, for  $V_{CC}$  ranging from 2V to 5V. Significant current spikes and current diminishments were detected when opening or closing the switches, due to the charge injected (NHV transistors) or taken (PHV transistors) by the main transistors switches (Figure 3.15 and Figure 3.18). In Figure 4.49 the measured injected charge for 100 $\mu$ A stimulus current is shown.



**Figure 4.49 Measured injected charge, 100 $\mu$ A current stimulus pulse for V<sub>Stimuli</sub> from 2V to 16V and V<sub>CC</sub>=2.8V.**

## 4.8 ESD testing

ESD testing was performed using an ESD gun “ESD Simulator NSG435” from Schaffner Instruments, that deliver ESD test pulses complying with the HBM (ESD Human Body Model) described in section 7.1. The test was carried by delivering a positive and negative ESD pulse to each pad of the three switches, with different amplitude values, with and without power supply connected. In Table 4.1 a summary of the test to be performed is presented.

**Table 4.1 Normalized ESD conditions to be tested.**

| Level                         | 0    | 1    | 2   | 3   |
|-------------------------------|------|------|-----|-----|
| No power supply<br>HV pads    | 500V | 1kV  | 2kV | 6kV |
| No power supply<br>Other pads | 250V | 500V | 1kV | 2kV |
| Power supply<br>HV pads       | 500V | 1kV  | 2kV | 6kV |
| Power supply<br>Other pads    | 250V | 500V | 1kV | 2kV |

The pass/fail criterion to determine the test success after ESD pulse injection includes: the switches must work properly (OPEN and CLOSE) and static power consumption must be normal (below 20nA) , after the induced ESD event.

In Table 4.2 the summary of the test result is shown.

**Table 4.2 ESD test results.**

| Level             | Switch A          | Switch B | Switch C |
|-------------------|-------------------|----------|----------|
| 0 No power supply | PASS              | PASS     | PASS     |
| 0 Power supply    | PASS              | PASS     | PASS     |
| 1 No power supply | FAIL <sup>1</sup> | PASS     | PASS     |
| 1 Power supply    | PASS              | PASS     | PASS     |
| 2 No power supply | FAIL <sup>1</sup> | PASS     | PASS     |
| 2 Power supply    | FAIL <sup>1</sup> | PASS     | PASS     |
| 3 No power supply | FAIL <sup>1</sup> | PASS     | PASS     |
| 3 Power supply    | FAIL <sup>1</sup> | PASS     | PASS     |

Note 1: Failed to open properly.

A very important conclusion is that the ESD strength of Switches B and C, is much higher than in the case of Switch A. The reason is that for the target process and in general, large NMOS like the ones in the TG of Figure 2.11, are much sensitive to ESD (a brief explanation is detailed in Annex A)



## 5 Conclusions

Throughout this thesis work, a study of HV-CMOS technology applied to implantable medical devices was conducted. A general purpose switch for electrical stimuli control in widely different situations was designed, fabricated in XT06 HVCMOS technology and measured. Three different versions of the circuit were compared (two of them very similar). The designed switches presented low impedance (around  $5\Omega$ ), high voltage capability (up to 16V), high current (up to 30mA) capability, with almost no static power consumption and leakage current below 1nA on each pin. The switches performance was almost the same for power supply ranging from 2V to 5V. For the three switches the measured characteristics comply with minor deviations, the initial specifications presented in section 1.3.

First a study of basic HV-CMOS devices and composite current control transistors, were presented (section 2). Then the complete switches design, including composite pass transistors and driving circuitry was presented in Section 3. Some novel HV circuit blocks were developed, like full range Level Shifters and a self-protected gate driver for PMOS transistors. In Section 4, an extensive set of measurements is presented, allowing comparing the performance of the three circuits.

Switches comparison:

Regarding the on-Resistance, all the switches show a good measured performance. Although the measured value exceeds the target  $5\Omega$  on certain circumstances, the result is considered to be acceptable. High current conduction capability is limited by the heat dissipation in the ASIC. It should be pointed out that during testing, a switch was damaged due to a short circuit. In a real medical device, the switches shall be protected against an accidental short circuit between electrodes.

Regarding voltage stimuli, the three designed switches are capable of delivering stimuli pulses from 100mV to 16V, for  $V_{CC}$  ranging from 2V to 5V. No significant differences were detected between the switches.

Regarding response time, all the switches show a good measured on/off time below 500ns.

Regarding the power consumption, all the switches show negligible static consumption (Below 5nA). Dynamic power consumption of Switch A is approximately proportional to frequency, indicating power consumption is due to the repetitive charge-discharge of gate and parasitic capacitors. In the case of switches B and C, power consumption has a fixed floor for large  $V_{Stimuli}$  values corresponding to the current through the protective loop of section 3.1.5.

In all three switches negligible leakage currents were measured.

Regarding crosstalk, Switches B and C present a much smaller crosstalk, because the switches are close by connecting  $V_{OUT}$  with the gate of transistor  $M_2$  (see Figure 3.18), instead of switch A that connects  $M_2$  gate to 0V (see Figure 3.15).

Regarding current stimuli and charge injection, the three designed switches are capable of delivering stimuli pulses from  $10\mu A$  to  $30mA$ , for  $V_{CC}$  ranging from 2V to 5V. Significant current spikes and current diminishment were detected when opening or closing the switches, due to the charge injected (NHV transistors) or taken (PHV transistors) by the main transistors switches, the injected charge is dependent of the stimuli voltage. In some cases switch A is able to diminish the effect of charge injection due to the high voltage transmission gate used as main switch.

Regarding area, switch A ( $3.8mm^2$ ) is almost two times larger than switches B,C ( $2mm^2$ ), because of the use of the HV transmission gate instead of two in series PHV transistors.

Regarding ESD, Switch B,C proved to be much more robust than Switch A. The problem with switch A is the large nhv NMOS transistors in the transmission gate configuration. As pointed in the manufacturer's ESD design guidelines, HV-PMOS are much more robust than HV-NMOS. In effect, phv turn-on characteristic in the case of an ESD event, is like in Figure 7.2 on the left, while for nhvs is like in Figure 7.2 on the right. For a large phv, turn on characteristic is homogeneous in the  $40000\mu m/3\mu m$  very wide transistor, thus ESD discharge can take place through the whole transistor (becomes what is known as a self-protected device). But the nhv deep snapback characteristic may cause a single transistor finger to trigger before the rest of the wide nhv, thus all the ESD current goes through a single finger (or transistor zone) causing a local transistor damage.

Due to ESD weakness, Switch A is, in principle, discarded and Switches B,C, are proposed as the better option. Switch A failed when performing ESD tests of section 4.8. Of course a better ESD protection mechanism can be designed with the cumulated ESD experience of the last designs in XT06 of our group, but in any case phv are inherently more robust. Also Switch A showed a much larger crosstalk effect than switches B, C (section 4.6) and a larger circuit area. On the other hand only a smaller charge injection can be observed in switch A under certain circumstances (because nhv, phv charge injection effect can be compensated in the TG). No significant differences were found between switches B and C.

The proposed switch:

Thus an overall conclusion is that Switch B, C can be either selected for the task. Switch A is momentarily put aside mainly because of ESD strength.

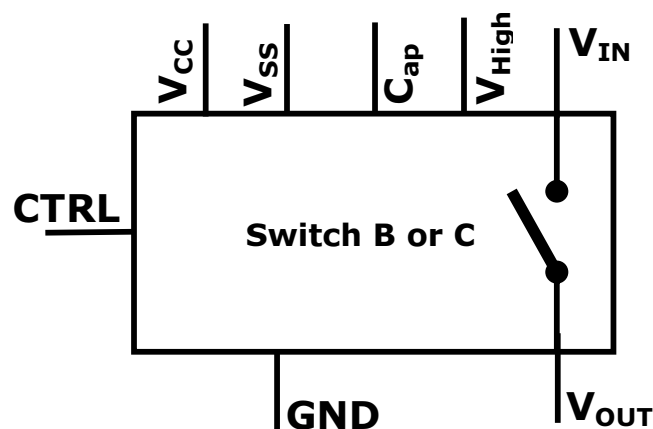
The proposed switches fulfill with minor deviations, the specifications in section 1.3.

In Table 5.1 the measured characteristics of the switches B (C) are presented,

**Table 5.1 Switches B and C measured characteristics.**

| <b>Characteristic</b>             | <b>Min</b> | <b>Typ</b>       | <b>Max</b>  |
|-----------------------------------|------------|------------------|-------------|
| <b>Impedance</b>                  | 3.5Ω       | --               | 8Ω          |
| <b>Power supply</b>               | 2V         | --               | 5V          |
| <b>Static current consumption</b> | --         | --               | Below 5nA   |
| <b>Leakage currents</b>           | --         | --               | Below 1nA   |
| <b>Voltage stimuli</b>            | 100mV      | --               | 16V         |
| <b>Current stimuli</b>            | 100μA      | --               | 30mA        |
| <b>Crosstalk</b>                  | --         | 0.1nC            | --          |
| <b>ON/OFF time</b>                | --         | --               | Below 500nS |
| <b>Symmetrical</b>                | --         | YES              | --          |
| <b>ESD protected</b>              | --         | --               | 6k          |
| <b>Area</b>                       |            | 2mm <sup>2</sup> |             |

The selected switches have 8 pins as shown in Figure 5.1, in pins names, function and type (see ANNEX A) is presented.



**Figure 5.1 Switch B and C block.**

**Table 5.2 Switch B or C pins.**

| <b>Name</b> | <b>Function</b>                       | <b>Type</b> |
|-------------|---------------------------------------|-------------|
| CTRL        | Open and closes the switch            | IN          |
| $V_{CC}$    | Power supply                          | $V_{CC}$    |
| GND         | Switch ground                         | GND         |
| CAP         | Pump capacitor                        | OUT         |
| $V_{SS}$    | Negative generated voltage            | $V_{SS}$    |
| $V_{IN}$    | Switch input                          | HV          |
| $V_{OUT}$   | Switch output                         | HV          |
| $V_{High}$  | Voltage reference to close the switch | HV          |

## 5.1 Future work

Some aspects were identified that can be improved in future versions of the switches:

- A compensator to diminish the spikes detected in section 4.7 can be incorporated and integrated into the switches if the necessary circuit area (a large capacitor will be required) can be assigned.
- A current limiting circuit can be introduced to protect the switches in the case of a short circuit between electrodes. Several techniques shall be investigated: current limit will be complex in the full range of operation, power limit via a temperature sensor in the die is easy to implement but may not fully protect the device.

## 5.2 Publications

Three publications are associated to this thesis work:

- 1) A.Arnaud, J.Gak, M.Miguez, "An integrated switch in a HV-SOI wafer technology, with a novel self-protection mechanism." JICS accepted to be published in 2010.

2) A.Arnaud, J.Gak, M.Miguez , "A self-protected integrated switch in a HV technology", Proc. 22th Symposium on Integrated Circuits and Systems Design - SBCCI 09 - Natal, Brazil - Sep.2009.

3) A.Arnaud, J.Gak, M.Miguez , "Integrated Switch for Implantable Medical Devices", Proc.XV Workshop of iberchip - Buenos Aires, Argentina - Mar.2009.

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## 7 Annex A: ESD protection design

ESD is a crucial factor for integrated circuits and influences their quality and reliability [8]. Custom PAD libraries including special HV protections, were designed for all the inputs and outputs, of the designed circuits. Custom PADS allowed an efficient die area allocation, as well as to verify safety considerations even at ESD protection circuitry level. In this Annex a brief introduction to ESD protection is presented, as well as the different protection circuits that were included in the ASIC.

### 7.1 Human Body model

Several models are used for ESD events but the most used is the Human Body model (HBM) and the ESD protections in this work were selected according to it. The HBM ESD event describes the discharge procedure of a charged human body directly into a device. The device is directly contacted and the charges are transferred into the device [8], the ESD test model uses the simplified equivalent circuit in Figure 7.1, where the human body is modeled by a 100pF capacitor and 1500 $\Omega$  series resistors.

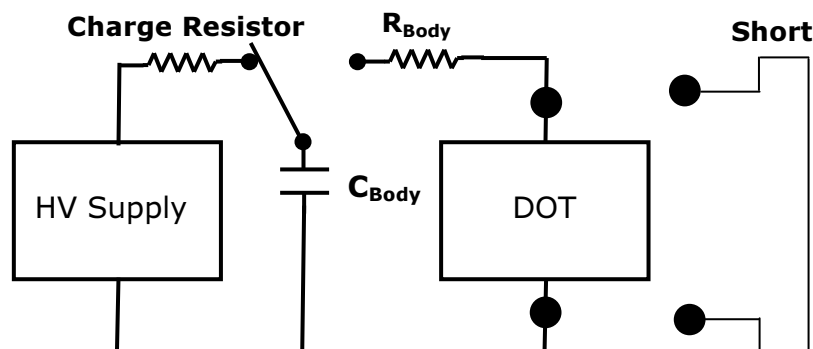


Figure 7.1 MIL-STD HBM circuit.



## 7.2 ESD protection device types

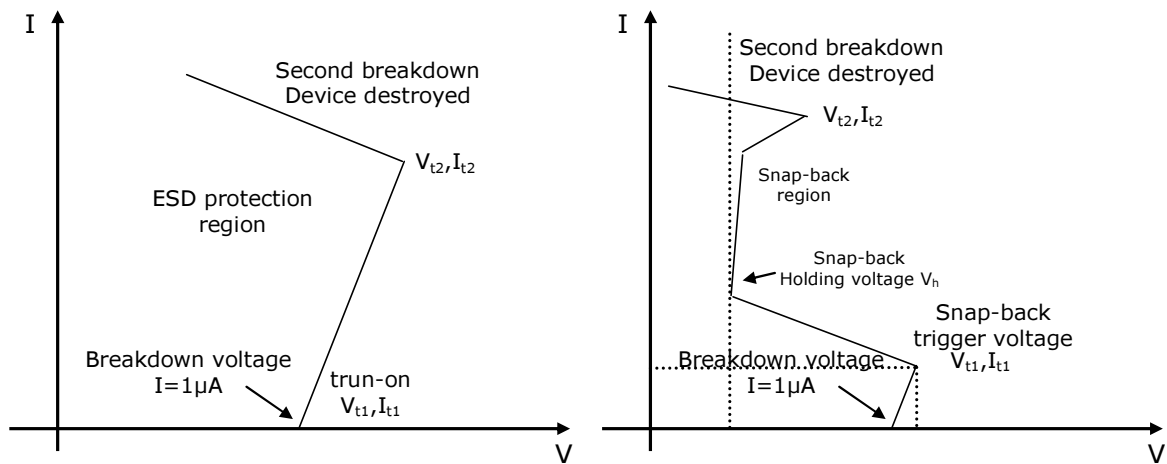
Basically, ESD protection circuitry limits the voltage between internal nodes in the ASIC and provides a discharge path in the HBM model, to avoid large current peaks through devices in the ASIC that are not prepared to do so. The ESD protecting follows some rules [8]:

- Sufficient discharging paths to bypass any ESD stress.
- Certain degree of ESD robustness and protect themselves against ESD damages during an ESD discharge.
- Provide a high ESD protection capability with minimum layout area
- Remain inactive in the normal operating condition of the IC and to pass normal I/O signals.
- Cause acceptable, as small as possible signal delays when added to an I/O structure.

There are basically two kinds of ESD protection devices to realize the ESD protection concept, turn-on characteristic or snap-back characteristic [8].

The turn-on characteristic ESD protection device is turned on at the threshold point  $V_{t1}$ ,  $I_{t1}$  in a certain triggering time and forms a low-impedance discharge path to divert the ESD current, shown in Figure 7.2 left side. The turn-on voltage needs to be sufficiently low for voltage clamping but ought to be greater than the operating voltage to avoid accidental triggering under normal operation.

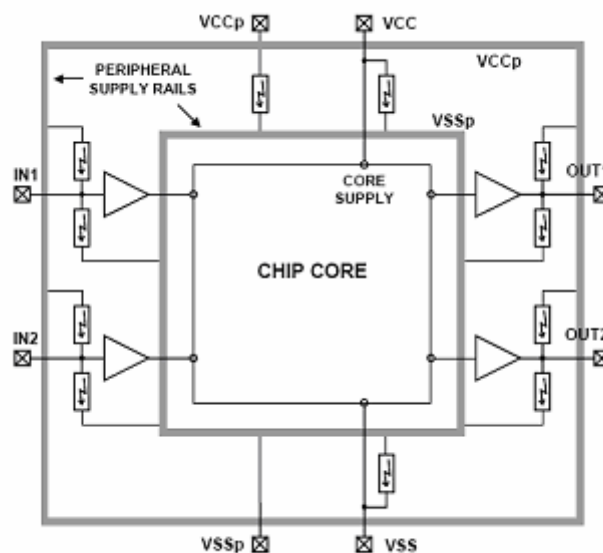
The snap-back characteristic of ESD protection device uses a snap-back I-V characteristic as in Figure 7.2 right side. When the ESD protection device is turned on at the triggering point the device is driven into the snap-back region with a low holding voltage creating a low impedance discharge path. The trigger voltage needs to be high enough above the operating voltage. The low trigger voltage ensures proper voltage clamping. Thus, a deep snap-back I-V curve is preferable for better ESD protection. The trigger current at the trigger voltage has to be selected with latch-up in consideration. The maximum ESD protection level of this device is represented by the second breakdown point,  $V_{T2}$   $I_{t2}$ .



**Figure 7.2** Typical turn-on and snap-back characteristics if ESD protection structure.

### 7.3 ESD protection strategy

ESD protection strategies can be implemented with a pad based protection. Pad based ESD protection shown in Figure 7.3, relies on ESD protection devices between the I/O pad and the ground rail. These devices will be forward biased or break down during ESD stress to divert the discharge current. Devices with snap back characteristic are preferred as breakdown devices. Additional ESD protection devices between the I/O pad and the supply rail are recommended but not required. The supply and ground pads have also to be protected by snap-back devices. A continuous ground rail is preferred [8].



**Figure 7.3** Pad based ESD protection.

## 7.4 Low voltage I/O ESD protected pads

In Figure 7.4 the low voltage I/O ESD protected pad is shown. It consists in a diode configuration PMOS ( $M_{pd1}$ ), diode configuration NESD ( $M_{nd1}$ ) (the NESD transistor is a low voltage NMOS transistor with a special ESD protection implant [9]) and poly resistor ( $R_s$ , not present in output type pads).

If a positive ESD event occurs discharge will be done through  $M_{pd1}$ , if a negative ESD event occurs discharge will be done through  $M_{nd1}$ ,  $R_s$  limits the input current to the integrated circuit.

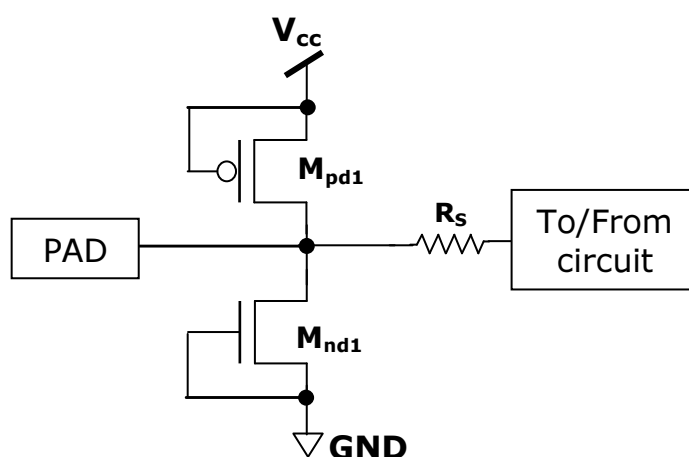


Figure 7.4 Low voltage I/O pad.

Transistors and resistors layout and sizes were determined using [9], in Table 7.1 a summary of transistors and resistors dimensions are shown.

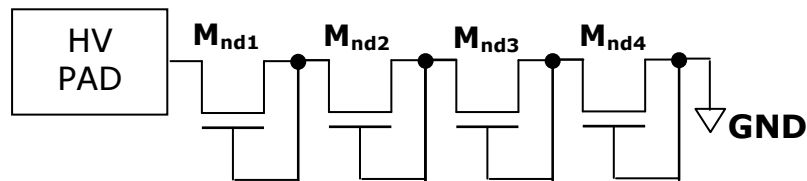
Table 7.1 I/O pad dimensions.

| Transistor | W/L ( $\mu\text{m}/\mu\text{m}$ ) | Number of gates |
|------------|-----------------------------------|-----------------|
| $M_{pd1}$  | 60/0.8                            | 16              |
| $M_{n1}$   | 68/1.1                            | 20              |
| Resistors  | Type                              | Value           |
| $R_s$      | $R_{\text{POLYH}}$                | 1.5K $\Omega$   |

## 7.5 High voltage I/O ESD protected pads

XT06 allows stacking of low voltage ESD protection devices to achieve higher break down voltages to use as a high voltage ESD protection device [9]. In Figure 7.5 the high voltage I/O ESD protected pad is shown consisting off 4 stacked diode configuration NESD ( $M_{nd1-4}$ ).

If a positive ESD event occurs discharge will be done through stacked NESD deep NPN snap-back (the NPN is a parasitic bipolar transistors), if a negative ESD event occurs discharge will be done through stacked diodes configuration NESD.



**Figure 7.5 High voltage I/O pad.**

Transistors layout and sizes were determined using [9], in Table 7.2 a summary of transistors sizes are shown.

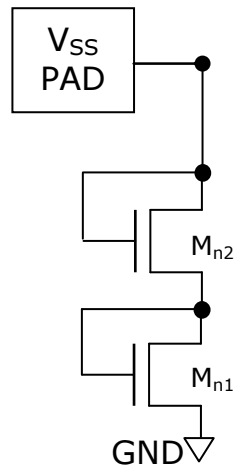
**Table 7.2 HV pad dimensions.**

| Transistor  | W/L ( $\mu\text{m}/\mu\text{m}$ ) | Number of gates |
|-------------|-----------------------------------|-----------------|
| $M_{nd1-4}$ | 68/1.1                            | 6               |

## 7.6 $V_{SS}$ ESD protected pad

In Figure 7.6 the  $V_{SS}$  pad is shown. It consist in a diode configuration, diode 2 stacked diode configuration NESD ( $M_{nd1-2}$ ).

If a negative ESD event occurs discharge will be done through stacked NESD deep NPN snap-back (the NPN is a parasitic bipolar transistors), if a positive ESD event occurs discharge will be done through stacked diodes configuration NESD.



**Figure 7.6  $V_{SS}$  pad.**

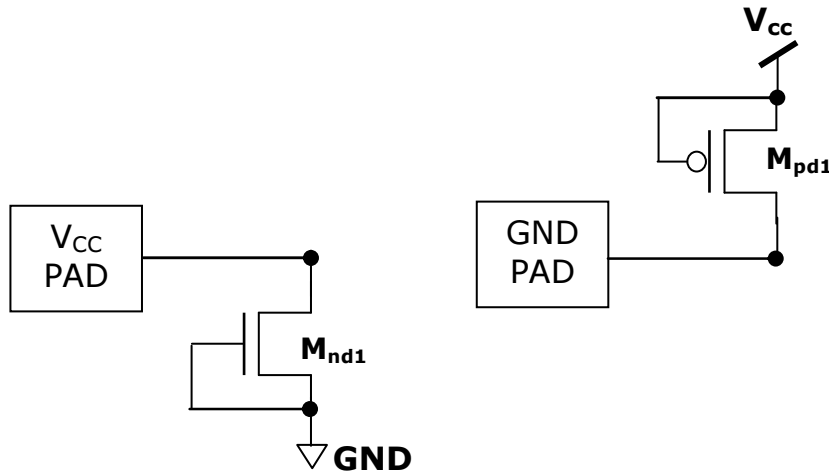
Transistors layout and sizes were determined using [9], in Table 7.3 a summary of transistors sizes are shown.

**Table 7.3  $V_{SS}$  pad dimensions.**

| Transistor | W/L ( $\mu\text{m}/\mu\text{m}$ ) | Number of gates |
|------------|-----------------------------------|-----------------|
| $M_{n1,2}$ | 60/1.1                            | 20              |

## 7.7 $V_{CC}$ and GND ESD protected pads

In Figure 7.7  $V_{CC}$  (left) and GND (right) protected pads are shown. It consist in a diode configuration PMOS ( $M_{pd1}$ ) for  $V_{CC}$  and a diode configuration NESD ( $M_{nd1}$ ) for GND (the NESD transistor is a low voltage NMOS transistor with a special ESD protection implant [9]).



**Figure 7.7  $V_{CC}$  (left) and GND pads (right).**

Transistors layout and dimension were determined using [9], in Table 7.4 a summary of transistors sizes are shown.

**Table 7.4  $V_{CC}$  and GND pad dimensions.**

| Transistor | W/L ( $\mu\text{m}/\mu\text{m}$ ) | Number of gates |
|------------|-----------------------------------|-----------------|
| $M_{pd1}$  | 60/0.8                            | 16              |
| $M_{nd1}$  | 68/1.1                            | 20              |

## 7.8 PAD list

In Table 7.5 the complete list of pad and pad type for each switch is presented.

**Table 7.5 Pads complete list.**

| <b>Name</b> | <b>Switch</b> | <b>Type</b> |
|-------------|---------------|-------------|
| CTRL        | A             | IN          |
| $V_{CC}$    | A             | $V_{CC}$    |
| GND         | A             | GND         |
| CAP         | A             | OUT         |
| $2V_{CC}$   | A             | HV          |
| $V_{IN}$    | A             | HV          |
| $V_{OUT}$   | A             | HV          |
| $V_{High}$  | A             | HV          |
| CTRL        | B or C        | IN          |
| $V_{CC}$    | B or C        | $V_{CC}$    |
| GND         | B or C        | GND         |
| CAP         | B or C        | OUT         |
| $V_{SS}$    | B or C        | $V_{SS}$    |
| $V_{IN}$    | B or C        | HV          |
| $V_{OUT}$   | B or C        | HV          |
| $V_{High}$  | B or C        | HV          |