

A Complete Compact Model for Flicker Noise in MOS Transistors

Alfredo Arnaud

Electrical Engineering Department
 Facultad de Ingeniería y Tecnologías - Universidad Católica del Uruguay
 Av.8 de Octubre 2801 CP.11200 - Montevideo, Uruguay
 e-mail: aarnaud@ucu.edu.uy

Abstract— In this work, a consistent, physics-based, one-equation-all-regions model for flicker noise in MOS transistors that consider both mobility and carrier number fluctuations is presented. The final result resembles the known BSIM flicker noise model but some inconsistencies are avoided because no approximations and interpolation are necessary. Instead, exact noise integration along the channel was possible with the aid of a one-equation-all-regions dc model of the MOS transistor. Finally, a brief discussion is presented about which of the terms of the new model are necessary for the designer, that require accurate but simple equations for the design space exploration.

I. INTRODUCTION

It is quite well accepted that the sources of flicker noise (or 1/f noise) are mainly carrier number and mobility fluctuations, due to random trapping–detrapping of carriers in energy states named ‘traps’ near the surface of the semiconductor. In transistors with very small dimensions the effect of one or a few single traps in the noise power spectral density (PSD) can be observed. In this work the however, the discussion is about noise for long channel, large transistors, with a large number of traps within the oxide (as usual in most analog circuits). But even for this case, a general, consistent, 1/f noise model has not yet been accepted. Flicker noise models are too complex or not general enough for the design space exploration, thus analog designers normally prefer empirical or SPICE models. Due to its simplicity the empirical model (SPICE NLEV=2,3):

$$\frac{S_{I_d}(f)}{I_D^2} = \frac{K_F \cdot g_m^2}{W \cdot L \cdot C_{ox}} \cdot \frac{1}{f^{EF}} \quad (1)$$

is very appropriate for hand calculations, and a good approximation of the physical model in equation (2) [1]. In (1) S_{I_d} is the noise current PSD of a transistor, K_F , EF , are constants to adjust, C_{ox} is the oxide capacitance per unit area, g_m , W , L , are the transistor transconductance, width, and length respectively. On the other hand, the BSIM flicker noise model of the Appendix [2][3] has been widely employed by designers using SPICE simulators, because the foundries normally provide adjusted BSIM parameters. The original noise model in [2] has changed little along time[3], considers

both local carrier number and mobility fluctuations, integrated along the channel using several approximations and interpolation. The model is accurate but has 3 parameters to adjust which seems excessive for a noise model. Other flicker noise models exist. A compact, physics based model was proposed in [4]:

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{ot} \mu}{L^2 n C_{ox}' I_D} \cdot \frac{1}{f^{EF}} \cdot \ln \left[\frac{n C_{ox}' \phi_t - Q_{IS}'}{n C_{ox}' \phi_t - Q_{ID}'} \right], \quad (2)$$

q , ϕ_t , μ , Q_{IS}' , Q_{ID}' are, respectively the electron charge, thermal voltage, carrier mobility, channel charge density at source and drain; N_{ot} [5] is the effective number of traps [5] a technology parameter to adjust, and n is the slope factor [6]. The model in (2) considers only carrier number fluctuations integrated using the dc model in [6], and in this work it will be extended to consider also mobility fluctuations. The result resembles BSIM model in (12), but interpolation and approximations are avoided. A brief discussion is presented also about which of the terms in both BSIM and the new model are necessary to accurately represent flicker noise in MOS transistors for analog circuit design.

II. COMPLETE COMPACT, PHYSICS BASED MODEL FOR FLICKER NOISE

Back to the physical origin of flicker noise, localized mobility and channel carrier density fluctuations in a differential channel element, cause a differential noise current contribution. To integrate the elementary noise contributions along the channel the transistor can be split into three series elements: the upper transistor, the lower transistor, and a small channel element of length Δx and area $\Delta A = W \cdot \Delta x$ as in Fig.1. Small signal analysis can be carried out, considering the general expression for the source (drain) transconductance [6]:

$$g_{msu} = -\mu W Q_{Ix}' / (L-d) \quad g_{mdl} = -\mu W Q_{Ix}' / d \quad (3)$$

Q_{Ix}' (or simply Q_I') is the charge density in ΔA at a distance x from the Source. ΔA resistance is defined like in [4]:

$$\Delta R = \Delta V_x / I_D = -\Delta x / (\mu W Q_{Ix}') = -\Delta x / (\mu W q N') \quad (4)$$

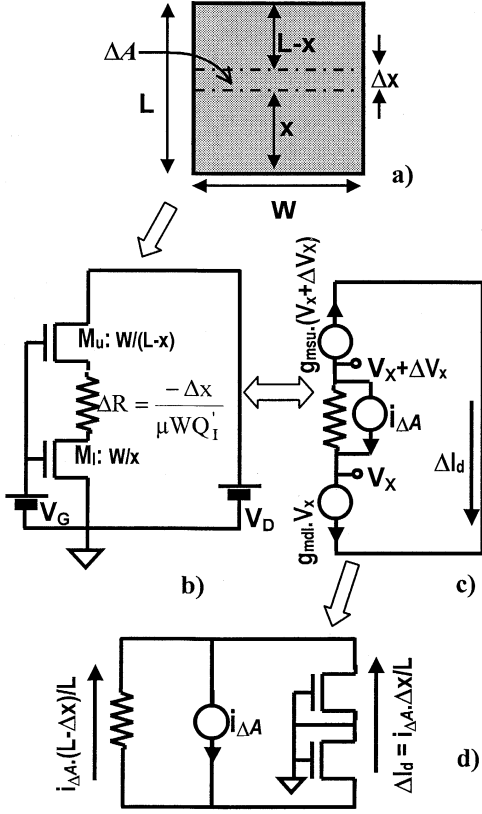


Figure 1. (a) MOS transistor channel and differential channel element ΔA (b) The transistor is separated into three series components (c) Small signal analysis to calculate the noise contribution to the drain current of the noisy element (d) Small signal equivalent circuit.

N' is the local carrier density in the channel. As shown in Fig.1(c), current division between the channel element and the equivalent small signal resistance of the rest of the channel result in $\Delta I_d = (\Delta x/L) i_{\Delta A}$. Thus after the small signal analysis, the drain current PSD can be integrated:

$$S_{I_d}(f) = \frac{1}{L^2} \int_0^L [\Delta x \cdot S_{i_{\Delta A}}(f)] dx \quad (5)$$

where $S_{i_{\Delta A}}$ is the PSD of the noise current generated in the differential channel slice $\Delta A = W \cdot \Delta x$. To relate the mobility, and carrier number fluctuation, to the noise current $i_{\Delta A}$, firstly the PSD of N'_A , the number of occupied traps in the oxide above the channel element ΔA , is derived using classical physical hypotheses. From [7]:

$$S_{N'_A} = \frac{1}{\Delta A} N_{ot} k_B T \lambda \cdot \frac{1}{f} = \frac{N_{ot}}{\Delta A} \cdot \frac{1}{f} \quad (6)$$

λ is the tunneling constant. Variations in N'_A are related to variations in N' through the Reimbold's r coefficient:

$$r = \left| \frac{\delta N'}{\delta N'_A} \right| = \frac{-Q'_I / \phi_t}{C_b + C_{ox} - Q'_I / \phi_t} \approx \frac{-Q'_I}{nC'_{ox} \phi_t - Q'_I} \quad (7)$$

C_b' is the depletion capacitance per unit area. Finally, variations in μ , N' are related to variations in current by a first order expansion of (4):

$$i_{\Delta A} = \frac{dI_D}{dN'_A} \delta N'_A = \left(\frac{\partial I_D}{\partial N'} \cdot \frac{\partial N'}{\partial N'_A} + \frac{\partial I_D}{\partial \mu} \cdot \frac{\partial \mu}{\partial N'_A} \right) \delta N'_A \quad (8)$$

where $\delta N'_A$ is the time fluctuation of the number of occupied states N'_A per unit area in the channel element ΔA . To evaluate

the derivatives $\frac{\partial I_D}{\partial \mu}$, $\frac{\partial \mu}{\partial N'_A}$ is necessary knowledge about the

dependence of the carrier mobility μ on N'_A . The only accepted model is the one based on Matthiessen's rule [2],[8], that is introduced into (8):

$$\frac{1}{\mu} = \frac{1}{\mu_n} + \alpha N'_A \Rightarrow i_{\Delta A} = \left[\frac{I_D}{N'} \cdot r + \frac{I_D}{\mu} \cdot \alpha \mu^2 \right] \delta N'_A \quad (9)$$

μ_n , α , are constants. Using (6) into (9) and taking the PSD:

$$\frac{S_{i_{\Delta A}}(f)}{I_D^2} = \frac{N_{ot}}{\Delta A} \left[\frac{r}{N'} + \mu \alpha \right]^2 \cdot \frac{1}{f} \quad (9)$$

The integration in (5) can be calculated following the procedure in [4], integrating the result of (9). Integration is

solved with the aid of $I_D = \frac{\mu W}{nC'_{ox}} (-Q'_I + nC'_{ox} \phi_t) \frac{dQ'_I}{dx}$ (from

[6]) to change the integration over the channel length in integration over the channel charge density. The integral is split in three terms corresponding each to a term in the expansion of (9).

$$\begin{aligned} \frac{S_{I_{d1}}}{I_D^2} &= \frac{q^2 N_{ot}}{W \cdot L^2} \cdot \frac{1}{f} \int_0^L \frac{1}{(nC'_{ox} \phi_t - Q'_I)^2} dx = \frac{q^2 N_{ot} \mu}{I_D n C'_{ox} L^2 f} \int_{Q'_{IS}}^{Q'_{ID}} \frac{dQ'_I}{nC'_{ox} \phi_t - Q'_I} \approx \\ &\approx \frac{q^2 N_{ot} \mu}{L^2 n C'_{ox} I_D} \cdot \ln \left[\frac{n C'_{ox} \phi_t - Q'_{IS}}{n C'_{ox} \phi_t - Q'_{ID}} \right] \cdot \frac{1}{f} \end{aligned} \quad (10.a)$$

$$\begin{aligned} \frac{S_{I_{d2}}}{I_D^2} &= \frac{2\alpha q N_{ot}}{W \cdot L^2} \cdot \frac{1}{f} \int_0^L \frac{\mu}{(nC'_{ox} \phi_t - Q'_I)} dx = \frac{2\alpha \mu q N_{ot}}{I_D n C'_{ox} L^2 f} \cdot \frac{1}{f} \int_{Q'_{IS}}^{Q'_{ID}} \mu \cdot dQ'_I \approx \\ &\approx \frac{2\alpha \mu^2 q N_{ot} (Q'_{ID} - Q'_{IS})}{I_D n C'_{ox} L^2} \cdot \frac{1}{f} \end{aligned} \quad (10.b)$$

$$\begin{aligned} \frac{S_{I_{d3}}}{I_D^2} &= \frac{\alpha^2 N_{ot}}{W \cdot L^2} \cdot \frac{1}{f} \int_0^L \mu^2 \cdot dx = \frac{\alpha^2 N_{ot} \mu}{I_D n C'_{ox} L^2 f} \cdot \frac{1}{f} \int_{Q'_{IS}}^{Q'_{ID}} \mu^2 (nC'_{ox} \phi_t - Q'_I) \cdot dQ'_I \approx \\ &\approx \frac{\alpha^2 N_{ot} \mu^3}{I_D n C'_{ox} L^2} \left[n C'_{ox} \phi_t (Q'_{ID} - Q'_{IS}) + (Q'^2_{ID} - Q'^2_{IS}) \right] \end{aligned} \quad (10.c)$$

Thus total flicker noise can be expressed:

$$S_{I_d}(f) = \frac{q^2 \mu}{I_D^2} \cdot \frac{1}{L^2 n C_{ox} I_D f^\gamma} \cdot \left[C_{NA} \ln \left[\frac{n C_{ox} \phi_t - Q_{IS}}{n C_{ox} \phi_t - Q_{ID}} \right] + C_{NB} (Q_{ID}' - Q_{IS}') + C_{NC} (Q_{ID}^2 - Q_{IS}^2) \right] \quad (11)$$

where C_{NA} , C_{NB} , C_{NC} , are constants defined respectively: $C_{NA} = N_{ot}$, $C_{NB} = (1/q)\alpha\mu N_{ot}(2 + \alpha\mu n C_{ox} \phi_t / q)$, $C_{NC} = (1/q)\alpha^2 \mu^2 N_{ot}$. Note C_{NB}, C_{NC} are correlated; in fact the model in (11) can be seen as a two parameter model (N_{ot} , α) but expression (11) is preferred to fit equation (12) form.

III. NOISE MODEL ANALYSIS

Equation (11) has the same functional dependence with Q_{IS}, Q_{ID} as BSIM model [2],[3] in strong inversion region (SI). But (11) is valid in the whole operation range of the transistor from SI to WI (weak inversion) and in saturation and the linear region. Also the model in (11) is inherently consistent regarding series-parallel association of transistors [1]. BSIM noise model is implemented in most SPICE simulators, and the foundries provide adjusted models expected to properly represent flicker noise. Some simulations were carried to check BSIM 1/f noise behavior in a 0.6 μ m technology, and to compare it to the models in (1),(2),(11). In Fig.2, simulated noise current (PSD square root in A/\sqrt{Hz}) plots are shown for a single PMOS $W=20\mu$ m, $L=5\mu$ m transistor while sweeping I_D . The normalized flicker noise PSD (S_{Id}/I_D^2) @1Hz is shown in Fig.3 for the same transistor using BSIM model (circles). Also the transconductance g_m , and Q_{IS}' , Q_{ID}' , were approximated with a dc analysis using BSIM3v3 model and (3). The results are shown in Fig.4 and were later employed to calculate flicker noise using (1) (dashed line) and (2) (continuous line) in Fig.3. K_F , N_{ot} , were adjusted in the logarithmic domain. Note the three models represent the expected behavior of S_{Id}/I_D^2 with a plateau in WI and decay as the transistor enters SI. For this transistor equation (2) with a single parameter to adjust and only the logarithmic term of Q_{IS}' , Q_{ID}' , accurately fits BSIM 1/f noise model. To further understand the behavior of equation (11), in Fig.4 Q_{IS}'/I_D , Q_{ID}'/I_D ratios are shown for the saturated PMOS of Fig.2, Fig.3. The g_m/I_D ratio is also shown to check the inversion level. Note $Q_{IS}'/I_D \gg Q_{ID}'/I_D$, as expected for a saturated transistor, and it is directly related to the contribution of (10.b) and (10.c) to the plot of Fig.3 when using the complete model of (11). Q_{IS}'/I_D term remains approximately constant in WI while it decays with a smaller slope than S_{Id}/I_D^2 of Fig.3 in SI. The terms (10.b) and (10.c) may help to correct the model in (2) if it underestimates flicker noise measurements in SI. Once adjusted, the complete model in (11) was very similar to the simulated BSIM of Fig.3 (not shown) just using the linear with Q_{IS}' term. Finally, in Fig.5, the simulated (and calculated) normalized flicker noise PSD (S_{Id}/I_D^2) @1Hz, is shown for a saturated NMOS in the same technology.

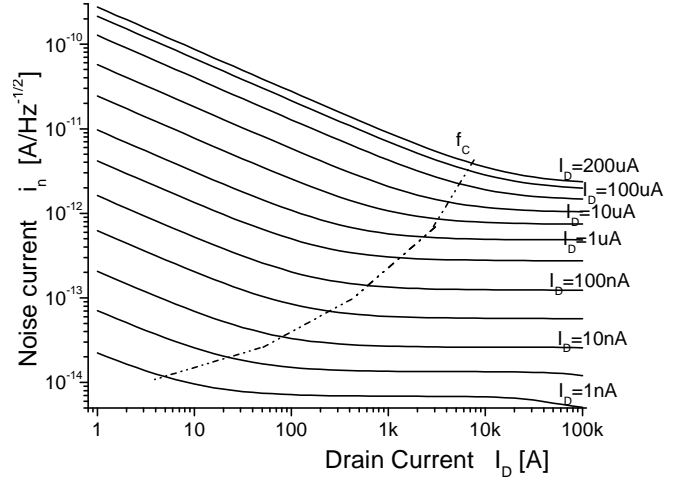


Figure 2. Simulated noise current of a $W=20\mu$ m, $L=5\mu$ m PMOS saturated transistor sweeping I_D . 1/f and thermal noise are included and approximated corner frequency f_c [1] is shown.

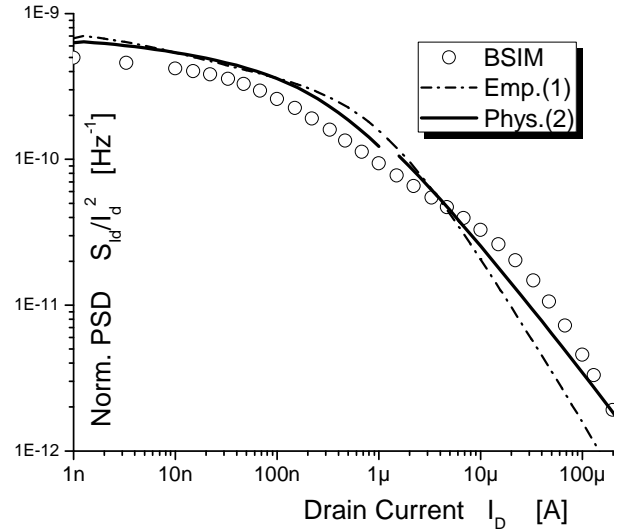


Figure 3. Normalized flicker noise PSD (S_{Id}/I_D^2) of a saturated $W=20\mu$ m, $L=5\mu$ m PMOS transistor at $f=1$ Hz. Circles: simulated BSIM noise (12); dashed line: calculated using (1); continuous line: calculated using (2).

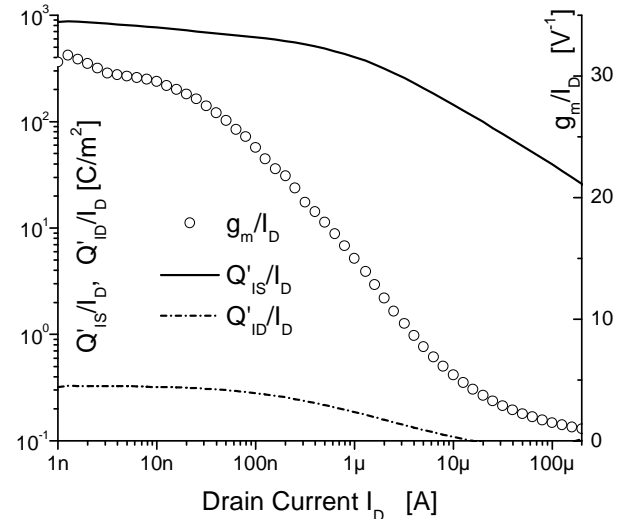


Figure 4. Simulated Q'_{IS} , Q'_{ID} , and g_m/I_D ratio.

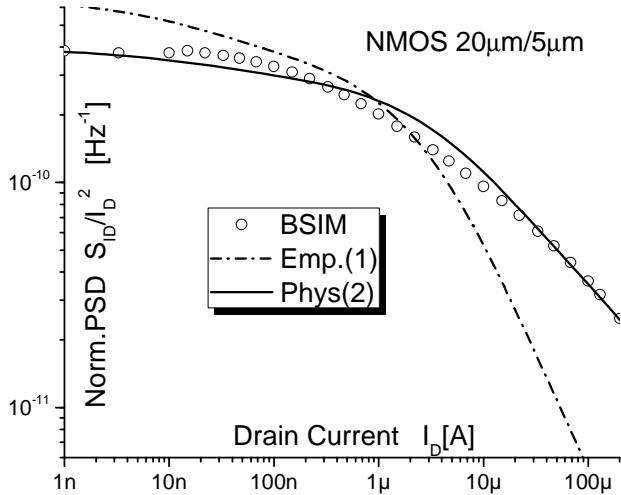


Figure 5. Normalized flicker noise PSD of a saturated NMOS at $f=1\text{Hz}$. Circles: simulated BSIM noise; dashed line: calculated using (1); continuous line: calculated using (2).

Simulated BSIM noise results are shown, as well as calculated flicker noise using (1) and (2) (K_F , N_{ot} , were adjusted in the logarithmic domain using this plot). Note in this case the empirical model in (1) underestimates BSIM noise simulation, but again the simplified model in (2) is a good approximation.

IV. CONCLUSIONS

A complete compact model for flicker noise in MOS transistors was presented. The proposed model is an extension of the one presented in [4], but considers both carrier number and mobility fluctuations using the Matthiessen's rule as in [2]. The result is a consistent, physics-based, one-equation-all-regions flicker noise model, which resembles BSIM model [2],[3] in the SI region. A few simulations were presented for a NMOS and a PMOS transistor, comparing BSIM (12), empirical (1), and carrier number fluctuation – only physical (2) models. The model in (2) using a single parameter to adjust properly represents BSIM model, and in [4] it was shown to accurately adjust several flicker noise measurements. The new model provides extra degrees of freedom to adjust noise measurements but on the other hand, too much noise parameters to adjust becomes a complex task that sometimes ends in misleading results.

Although a strong conclusion has to be supported by the analysis of several technologies, transistor sizes, and noise measurements, which cannot be presented in a moderate paper length, few preliminary comments follow:

- Interpolation like in (12) is not necessary, the proposed model can represent flicker noise PSD from weak to strong inversion, in saturation and in the linear region taking into account both carrier number and mobility fluctuation effects.
- In several situations, the carrier number fluctuations-only model of [4] was enough to accurately represent flicker noise. The new model using just 2 parameters to adjust or considering only the linear term of the charge density should result a good trade-off.
- But an extra parameter, or a correction to (11), should be necessary to take into account the flicker excess noise in short

channel transistors. A larger trap density is expected in the transistor boundaries, resulting in an additional noise term that is not being addressed in (11).

APPENDIX

From the latest BSIM technical manual available online [3], flicker noise model is split in two equations for different operating regions. In SI:

$$S_{I_{dSI}} = \frac{\phi_t q^2 I_D \mu}{L^2 C_{ox}' \cdot 10^{10}} \left[q \cdot \text{Noia} \cdot \ln \left[\frac{-Q'_{IS} + qN^*}{-Q'_{ID} + qN^*} \right] + \text{Noib} (Q'_{ID} - Q'_{IS}) + \frac{\text{Noic} (Q'^2_{IS} - Q'^2_{ID})}{2q} \right] \cdot \frac{1}{f^{E_f}} \quad (12.a)$$

$$\text{In WI:} \quad S_{I_{dWI}} = \frac{\text{Noia} \cdot q \cdot \phi_t \cdot I_D^2}{W \cdot L \cdot N^{*2} \cdot 10^{10}} \cdot \frac{1}{f^{E_f}} \quad (12.b)$$

Then flicker noise is interpolated:

$$S_{I_d} = S_{I_{dSI}} \cdot S_{I_{dWI}} / (S_{I_{dSI}} + S_{I_{dWI}}) \quad (12.c)$$

$N^* \approx n C_{ox}' \phi_t / q$, Noia , Noib , Noic , are model parameters to adjust, that can be each one related to C_{NA} , C_{NB} , C_{NC} , in (11). Note (12) in comparison to [3] is written in terms of charge densities Q'_{ID} , Q'_{IS} instead of carrier densities. Finally, the model in [3] includes term to account for the noise overhead in a short channel transistor, a problem that is not studied in this work.

ACKNOWLEDGMENTS

The authors would like to thank Agencia Nacional de Investigación e Innovación (ANII - Uruguay) grant FCE 7091, and PEACE EU program for the support to this work.

REFERENCES

- [1] A.Arnaud and C. Galup-Montoro, "Consistent Noise Models for Analysis and Design of CMOS Circuits", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.51, no.10, pp.1909-1915, Oct.2004.
- [2] K. K. Hung, P. K. Ko, C.Hu, and Y.C.Cheng, "A physics-based MOSFET noise model for circuit simulators", *IEEE Trans. Electron Devices*, vol. 37, no.5, pp.1323-1333, May. 1990.
- [3] H.Agarwal, S.Khandelwal, J.P.Duarte, Y.S.Chauhan, A.Niknejad and Chenming Hu, "BSIM6.1.0 MOSFET Compact Model - TechnicalManual", University of California, Berkeley, 2014.
- [4] A.Arnaud and C. Galup-Montoro, "A compact model for flicker noise in MOS transistors for analog circuit design", *IEEE Trans. Electron Devices*, vol.50, no.8, pp.1815-1818, Aug.2003.
- [5] Y. Nemirovsky, I. Brouk, and C. G. Jakobson, "1/f noise in CMOS transistors for analog applications", *IEEE Trans. Electron Devices*, vol.48, no.5, pp.921-927, May.2001.
- [6] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design", *IEEE J. of Solid-State Circuits*, vol.33, no.10, pp.1510-1519, Oct.1998.
- [7] A.Arnaud, and M.R.Miguez, "Very low frequency cyclostationary 1/f noise in MOS transistors" in *Procs. of the 22nd International Conference on Noise and Fluctuations (ICNF)*, Montpellier, Jun.2013. DOI: 10.1109/ICNF.2013.6578983
- [8] Yannis Tsididis, Colin McAndrews, *Operation and Modeling of the MOS Transistor*, Oxford University Press, 3rd Edition, Sept.2010, ISBN-10: 0195170156.