A Safe MOSFET Driver for Stimulation of Biological Tissue

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***Abstract*— Safety is one of the main concerns in ASICs for implantable medical devices. One general rule for safety is that the failure of a single circuit element in a circuit connected to tissue must not cause a DC current flow through the electrode connected to tissue larger than a few µA. In single electrodes and electrode arrays, there are many switches to deliver stimuli, to select the polarity, or to select the output electrode, etc., that are potentially harmful for example in the case of a punctured MOS switch gate. In this work the design, simulation, and test of a novel safe switch gate control circuit block is presented. The circuit was fabricated in a 0.6µm SOI HV technology, and is aimed at driving MOSFETs in direct contact to biological tissue to drive up to 18V stimuli.**

Keywords— safe stimuli; implatable devices; biomedical circuits; HV CMOS.

I. INTRODUCTION

In recent years, there has been a remarkable growth in the research and development of new implantable devices for the treatment of different pathologies [1]. Most active implants are battery powered embedded systems, which sense biological signals, and deliver stimuli to biological tissue. Stimuli are either current or voltage pulses (or pulse trains) to the patient ranging from a few hundreds of mV to well over 10V voltage or from a hundred µA to tens of mA. Stimuli section of the circuit may consist of the basic elements shown in Fig.1a: a stimuli generator (either a voltage or current source), electrodes which connect the tissue to the device, a switch that toggles the electrical connection of the electrodes, and a control block that decides when and for how long a stimulus should be applied. Two key concepts apply in the case of implantable electronics: reliability and safety. A reliable circuit is not likely to fail, and good design and implementation practices are followed to increase reliability of medical devices. But it is not possible to say that a circuit will never fail, thus in a failure condition the circuit must not be harmful to the patient. A safe device will not cause harm in the case of a single failure (for example a single transistor, a single capacitor fail, or a single software error condition). Uncorrelated multiple failures are not considered in a safety analysis, but if a failure causes a second element to fail, the whole event is considered as a single failure. Harmful events depend on the specific application like for example a too fast cardiac pace stimulation rate in a pacemaker. But a possible harm common to most stimulators and even bio-signal amplifiers connected to tissue, is the DC current flow to tissue larger than a few µA [3] causing an irreversible damage due to electrolysis like effects in the tissue. Thus all stimulators must deliver a null (balanced) average charge to tissue, and must be protected to semiconductor failures like the switch in Fig.1a. Several mechanisms have been proposed in the past like DC blocking capacitors in the stimuli or sensing path [4,5], a DC blocking capacitor in the bias connection [7], leakage current sensing [6], among others, to properly protect a circuit to make it safe for the patient. But not all these circuit strategies are possible on every stimulator, and normally is preferable to avoid complex circuitry like leakage detection. While academic papers do not always report a safe circuit, safety is essential in practical biomedical devices to be compliant with regulations. In this work, a fully integrated safe driver for a gate switch like in Fig.1 is presented.

II. SAFETY ISSUES IN STIMULI DELIVERY SYSTEM

In Fig. 1b the embodiment of a simple stimuli delivery circuit is shown using a single PMOS HV pass transistor [2]. High voltage transistors are necessary to withstand the large amplitude pulses in many therapies. The gate G_1 of the transistor M_1 is set to V_{STIM} to block current; the gate is set to GND to let the current pass to tissue to deliver a pulses. The control block in this case is for example a simple logic driver and eventually a level shifter [2] if V_{STIM} is higher than the logic supply voltage V_{DD}. Pulses are delivered at a low frequency basis, and are short in time, thus most of the time V_G is connected to V_{STIM} (or eventually V_{DD}), and a potentially harmful event may occur in the case of a simple circuit failure. In effect if the gate of M_1 is punctured, a direct path through tissue between V_{STIM} and GND appears, generating a large DC leakage current I_{leak} and causing harm. The traditional solution to cope with a single failure like a short in a device in the stimuli current path, is to place a large capacitor in series with tissue to block DC current [4][5]. But a series capacitor may distort the pulse shape, has to be discharged later (charge balance), and increase the component count. Thus it is not always possible to turn a circuit safe just by means of capacitors in series to tissue.

A traditional solution to the safety issue of Fig.1 b is presented in Fig. 1c. The protection scheme includes a capacitor in series with M_1 gate (not with tissue) and a resistor. A fast '0' to '1' transition of M_1 gate is guaranteed by C_1 capacitor and then

the value is held by the 2MΩ R_1 resistor. In case the gate of M_1 is punctured, R_1 appears in the DC current path limiting the leakage I_{leak} to a few µA within safety boundaries (while R_1 will be in all cases in the MΩ, a specific study shall be conducted to determine its value depending on the type of electrode, tissue, and V_{STIM}). The main disadvantage of this topology is that for a realistic M_1 size and pulse characteristics, C_1 result too large to be integrated. Normally M_1 has a minimum channel length of for example 2µm -5µm for a high voltage transistor, but a channel width of thousands µm [2,5] to reduce the switch impedance during stimuli to a few Ω thus the gate capacitance is large. Also pulses may be short in time with edges below 1µs so a large capacitor C_1 is required to drive G_1 fast. While the R-C approach of Fig.1c can be found in several medical devices, modern integrated circuit capabilities allow implementing much efficient solutions. In this work a novel safety control system is presented, to emulate the behavior of the circuit in Fig.1.c, but without the use of a large capacitor. The new circuit will be denoted as a safe driver, it was designed, fabricated in a 0.6µm HV technology (to comply with up to 18V V_{STIM}), and tested.

III. A NOVEL SAFE STIMULI CONTROL SYSTEM

The safe driver is presented in Fig.2. It protects the stimuli system against a gate puncture emulating the circuit in Fig.1c. The circuit limits current to V_{STIM} in the steady state (DC) by a 2MΩ resistor, but guarantees a fast '0' to '1' and '1' to '0' transition. The idea is to substitute the capacitor of Fig.1c with the HV transmission gate (TG) of Fig.2. A synchronous finite state machine (FSM) controls TG. The clock of the FSM is a slow 512Hz clock present in the system. The low voltage (0-V_{DD}) input signal IN is generated by de Digital Control block, and is shifted by the HV_BUF on Fig.2 to 0-V_{STIM} logic levels. This buffer is a classic level shifter [2]. The HV_BUF has a relatively large current drive capacity thus this signal is enough to turn on (V_G = GND) and off (V_G = V_{STIM}) M_1. But when M_1 is off (most of the time), a puncture in the gate may result in a harmful leakage. To limit DC current the HV_BUF controls the gate of the M_1 transistor through the 2MΩ R_1 high resistivity poly resistor. To guarantee fast transient response even if the gate capacitance of the M_1 transistor is large, a transmission gate is connected in parallel with R_1. A simple synchronous FSM closes the TG immediately after an IN low to high transition (to turn-off M_1), and keeps it closed for at least 1 extra clock period. In this way, after each positive IN edge, the TG is closed a short time to fast charge M_1 gate. After this period, V_G value is held by R_1. If the oxide gate of M_1 is broken, steady state leakages are limited to a few µA and only short time pulses of larger I_{leak} are possible when TG is closed. But it should be pointed that electrolysis is related to the net leakage charge thus short I_{leak} pulses are not harmful. HV transistors are used in the TG and its driving circuitry capable to withstand up to 18V $V_{GS(D)}$. Note the circuit at this point only protects the gate against leakages when M_1 is open; but in effect it has only sense to protect M_1 when open and when M_1 is closed tissue is being intentionally connected to V_{Stim} and a current flow in normal operation.

The FSM uses 2 FFDs named Q_0 Q_1, it is implemented with low voltage (0-V_{DD}) logic, and the output is shifted to (0-V_{STIM}) with a level shifter like HV_BUF with complimentary outputs [2]. Next state logic is simple:

$$Q_1^* = Q_1' \cdot Q_0 + \mathrm{INFSM} \cdot Q_0$$
$$Q_0^* = Q_0 + \mathrm{INFSM} \qquad (1)$$

while the output is

$$CTRL = Q_0 \cdot Q_1 \cdot \mathrm{IN}FSM \qquad (2)$$

A. SIMULATIONS

The safe driver control the transistor M_1 (Fig. 2), and guarantees a simulated ON-OFF time below 10µs while protecting the system against single failure event. The finite state machine FSM generates the signal CTRL, which is always opposite to IN (in fact the circuit shall be better described as a safe inverter instead of a safe driver) but must stay high for at least 2ms after IN is high. In Fig. 3 a simple FSM simulation is presented showing how the control signal remains high for at least one 512Hz CLK signal before going low.

In order to simulate a failure event the output of the safety inverter is connected directly to GND, the results are shown in Fig. 4, showing that the current drops to a less than 3µA after a few milliseconds

Simulated ON/OFF times for all transistor models (typical, worst slow and worst fast) were below 10µs utilizing a W=10000µm, L=3µm, PMOSHV M_1 switch

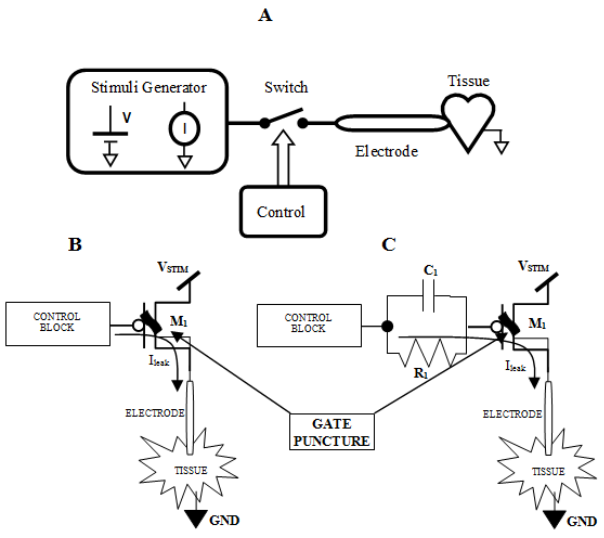

Fig.1. a) General schematic of a stimuli system b) Simplified stimuli delivery system c) A solution to safety issues.

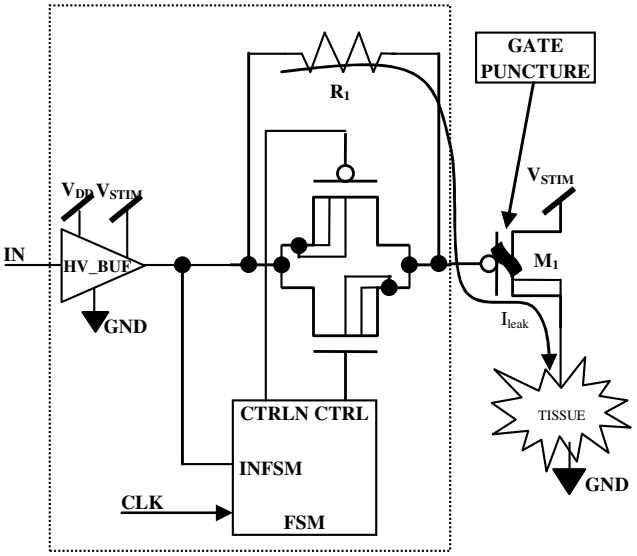

Fig. 2. Safety driver schematic.

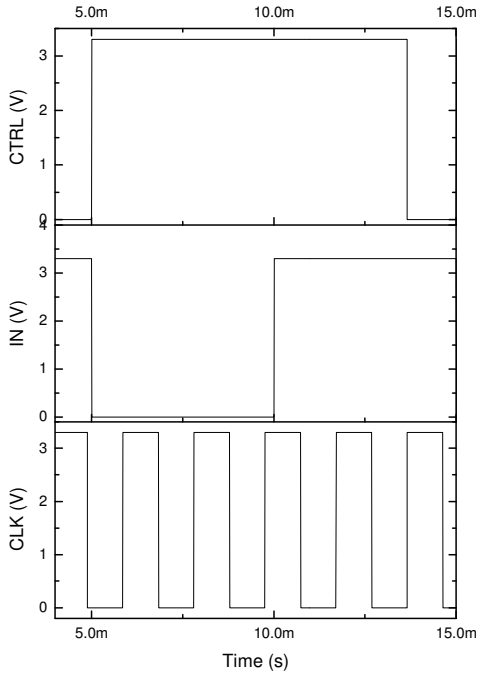

Fig. 3. Simulation of the FSM.

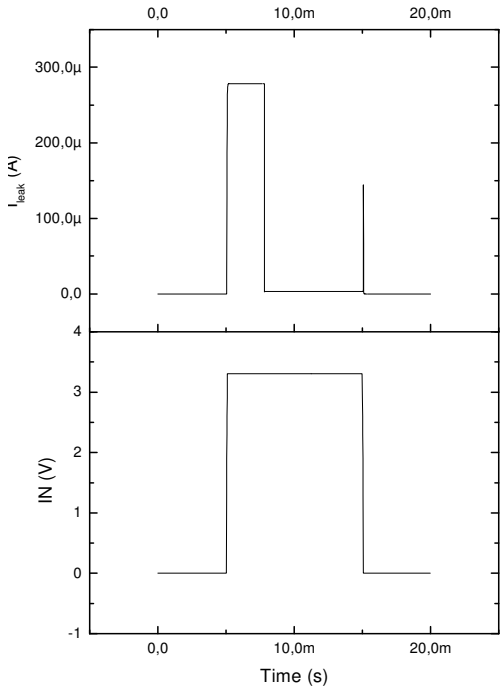

Fig. 4. M_1 oxide break simulation

B. Layout Design

A proper layout is necessary to maintain the circuit compliant with safety issues. It has no sense to protect M_1 against a gate oxide failure if within the ASIC a metal wire connected to tissue runs in parallel at a minimum distance of a V_{DD} wire. The following precautions were taken into account:

- Wires conducting V_{DD} or any other HV signals that are in the same metal layer as wires connected to electrodes, are not be closer to three times the minimum metal spacing (Fig. 5a).
- Wires conducting V_{DD} or any other HV signal shall not cross over wires connected to the electrodes. If not possible to follow this rule, wires are not drawn in consecutive layers (Fig. 5b).

In Fig. 6 (top) the complete layout of the safe driver is shown, the total occupied area is 157µm x 87µm. A microphotograph of a four safe driver array used in a more complex ASIC for implantable medical devices is shown in the bottom of Fig.6

C. MEASUREMENTS

The safe driver was fabricated in a 0.6µm HV technology in a SOI wafer [2], and measured. While it was not possible to artificially damage a gate oxide inside the chip, some electrical characteristics were characterized. In the fabricated circuit, M_1 was a W=10000µm, L=3µm, PMOS HV switch capable to withstand up to 18V V_{GS}, and up to 40V V_{DS}. The measured on-resistance of the switch was below 12Ω at V_{STIM}= 2.0V for 5 samples measured. The driver and switch

properly worked in a wide range of operating conditions with low voltage V_{DD} ranging from 1.8V up to 5V, and V_{STIM} ranging from 1.8V up to 18V. The power consumption was negligible, below 50nA in steady state, but it cannot be directly measured because this circuit block is part of a more complex stimulator array sharing the power supply. The time delay was less than 10µs but it is not possible again to separately measure the delay of this circuit block. Finally, in the plot of Fig.7, a measured pulse in a pacemaker like configuration (500Ω differential electrode, with a series capacitor on one side and the safe driver on the other [8]) is presented.

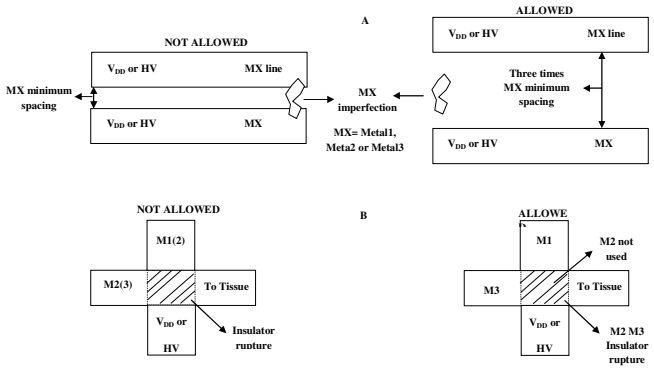

Fig. 5. Layout precautions taken into account.

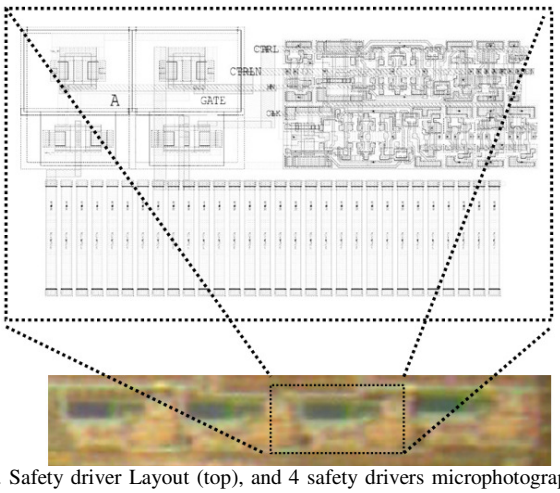

Fig.6. Safety driver Layout (top), and 4 safety drivers microphotography of 800µm x 100µm (bottom).

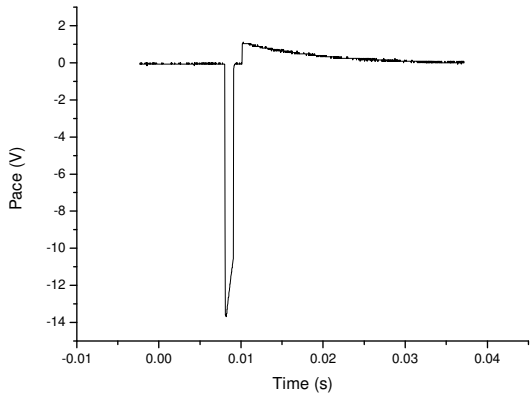

Fig.7. Measured pulse and charge balance in a pacemaker like configuration.

IV. CONCLUTIONS

In this work a brief analysis of safety issues in ASICs for implantable medical devices was presented. A novel fully integrated safe driver to control the gate of stimuli switches in contact to biological tissue, was presented. The circuit was designed, fabricated in a 0.6 µm HV technology, and tested, showing it can guarantee fast ON/OFF times (below 10µs) and also limit the leakage current in case a of a gate oxide failure event. The driver and switch properly worked in a wide range of operating conditions with low voltage V_{DD} ranging from 1.8V up to 5V, and V_{Stim} ranging from 1.8V up to 18V.

References

[1] Freedonia Group, *Implantable Medical Devices*, Study number: 2852 Cleveland Ohio,2012.

[2] A.Arnaud, J.Gak, M.Miguez, "An integrated switch in a HV-SOI wafer technology, with a novel selfprotection mechanism." Journal Integrated Circuits and Systems, March 2010. Vol 5. no 1; pp. 7-15

[3] R.V. Shannon, "A model of safe levels for electrical stimulation," IEEE Transactions on Biomedical Engineering, 1992, vol. 39, no. 4, pages 424-426

[4] D.Prutchi, M.Norris, "Cardiac Pacing and Defibrillation" Chapter 8 in *Design and Development of Medical Electronic Instrumentation*, Wiley-Interscience 2005, ISBN 0-471-67623-3.

[5] L. Lentola, A. Mozzi, A. Neviani, and A. Baschirotto, "A 1 µA front end for pacemaker atrial sensing channels with early sensing capability." IEEE Transactions on Circuits and Systems -II, vol. 50, no. 8, pp. 397–403, 2003.

[6] Moghe. Y, Lehmann T. "A Novel Safety System Concept and Implementation for Implantable Stimulators: A Universal DC Tissue Leakage Current Detector" ISCAS 2008 pp. 2498-2501

[7] M. Barú, "Implantable Signal Amplifying Circuit for Electroneurographic Recording", U.S. Patent 6,996,435 issued February 7th, 2006.

[8] J.G. Webster (Eds.), Design of Cardiac Pacemakers, IEEE Press: New York, 1995. ISBN0-7803-1134-5