An Integrated H-Bridge Circuit In A HV Technology.

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***Abstract*—H-Bridges are well known circuits to connect a load to a DC supply in both forward/reverse bias. These circuits are commonly used to drive DC and stepper motors among many other power electronics applications. In this work, a fully integrated 12V H-Bridge is designed in a 0.6µm HV technology as a replacement of an obsolete commercial part. The main objective is to provide an OEM in Uruguay with a flexible and low cost substitute of an off the shelf IC currently utilized on its products, that is being discontinued. The new H-Bridge was designed for the same package and improves some characteristics like power consumption, maximum switching frequency, over the old one. Because the cost is a major constrain to reach production stage in this project, the silicon area was reduced as much as possible. The resulting circuit is a low cost 12V H-Bridge, with a logic input '1' down to 2.8V, switching up to 300kHz, in a 1.8mm^2 die area.**

Keywords—H-Bridge; Motor driver; IC design; HV Technology.

I. INTRODUCTION

An H-Bridge is a common electronic circuit block used to apply a voltage across a load in either forward/reverse direction. H-Bridges are often used in DC-AC and DC-DC push–pull converters, to drive DC motors in consumer electronics and robotics allowing motors to run forwards and backwards, among other applications. Also most bipolar stepper motors are driven by two H-Bridges. Note in most cases, H-Bridges are used to drive an inductive load. In particular, this project started with proposal from a company in Uruguay [2] utilizing the same existing H-Bridge in two products: to drive the stepper of the paper feed in a portable thermal printer, and to drive the antenna coil in a LF RFID portable reader unit [3]. In the later, coil excitation is at 132kHz thus the H-Bridge has to switch fast. H-Bridges can use MOSFETs, BJTs, IGBTs, to switch the load, in this case a CMOS bridge will be developed. In Fig.1 a scheme of an H-bridge is shown and a schematic of a CMOS implementation is shown in Fig.2.

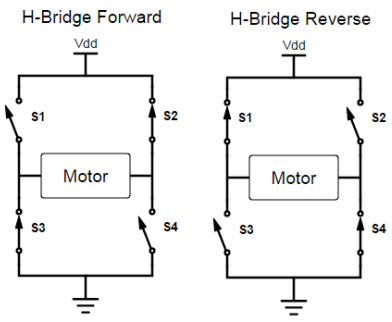
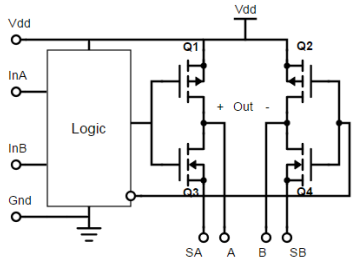


Fig. 1. H-Bridge connected to a motor. Left: motor running forward. Right: motor running backward.

A. Current H-Bridge

The discontinued H-Bridge is an integrated one with TTL compatible inputs, capable to deliver a continuous 1A current output at V_{DD} = 12 V (room temperature) at switching rates up to 200 kHz. Internal logic implements the switching scheme of Fig.2 and also prevents the upper and lower outputs of either half-bridge from being turned on simultaneously. Unique input codes allow both outputs to be forced low (for braking) or forced to a high impedance level. The circuit is available in 8-pin SOIC packages, specified to operate over a voltage range of V_{DD} from 3.8V to 13.2V in a temperature range of -40 °C to 85 °C.



Truth Table			
InA	***InB***	***OutA***	***OutB***
0	0	0	0
0	1	0	1
1	0	1	0
1	1	HiZ	HiZ

Fig. 2. The designed H-Bridge schematic with pinout and Truth Table.

B. The new bridge

The main objective of this work is to present the cost-oriented design of a new H-Bridge ASIC to substitute the discontinued one of section I.A, by an own ASIC implemented in a 0.6µm HV technology. The initial target production for this chip is few tens thousands units, this technology was selected because of the previous experience with it to avoid the setup cost of a new technology, and because resulted in the best trade-off between performance/cost between other technologies were the team had experience. Note the key aspect here to study is the switching transistors' size. Initial specifications were obtained from the current bridge datasheet and measurements, and applications data [2][3]. Initial specifications are: total bridge resistance below 1Ω in on-state, maximum switching rate above 200kHz, V_{DD} from 3 to 12V, logic input high from 2.7V to V_{DD}, pinout and SO-8 package must be the same as for the old bridge. Any possible improvement to the reference IC should be considered.

II. H-BRIDGE DESIGN

A. Primary transistor estimation.

The starting point to determine the type and size of the 4 main transistors in Fig.2 that compound the H-Bridge, are the maximum current value at the maximum voltage rated (1 A @ 12 V) . In order to withstand up to 12V V_{DD}, high voltage transistors are required. High voltage transistors have at least a diffused drain, a minimum length much higher than the technology feature, and in this case a thick oxide to withstand up to $18V_{GS(B)}$ voltages. The target technology has several kinds of transistors up to 60V V_{DS} but a medium voltage option was selected. These medium voltage transistors will be denoted as MV-PMOS (medium voltage lightly doped drain PMOS) and MV-NMOS (medium voltage lightly doped drain NMOS), and withstand up to 12V V_{DS}. A cross section of the mosfets is shown in Fig.3, they have a minimum length L_{minP} = 1.2µm and L_{minN} = 1.4µm respectively. Different options were evaluated, but larger voltage transistors (25-30V ones) have almost twice the minimum channel length, diffusion length, and almost 8 times the occupied area for the same on-resistance.

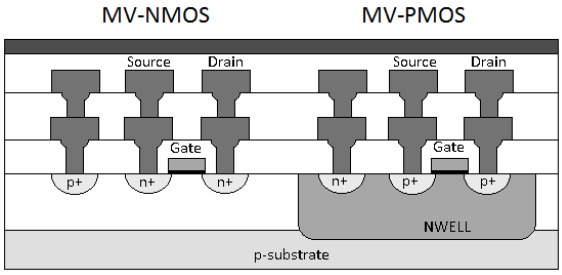


Fig. 3. MV NMOS and PMOS transistors structure.

R_{ON} denotes the on resistance of a single transistor in on-state and a starting estimation is 0.5Ω. Then using the classic approach [4]

$$R_{ON} = \frac{1}{k * \left(\frac{W}{L}\right) * \left(V_{GS} - V_T\right)} \quad (1)$$

The width W and length L of the four transistors of the H-Bridge could be estimated, using minimum channel length.

TABLE I. ESTIMATED SIZE OF TRANSISTORS

Dimensions	PMOS	NMOS
L	1.2 µm	1.4 µm
W	40000 µm	8000 µm

The complete H-Bridge circuit consists of the five blocks in Fig.4, each one with a specific function. Left and right branches of the bridge have an equal logic/driver circuit. A brief description if each block follows.

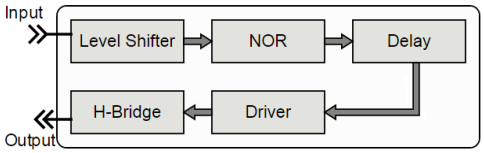


Fig. 4. Blocks diagram for each branch.

Level Shifters: As the H-Bridge described in section I.A has only one dedicated pin for V_{DD}, and there is no specific supply for the logic, a level shifter at each input is implemented in order to convert 0-V_{Log} logic signal inputs to a 0-V_{DD} level signal to control the load. V_{Log} ~ 2.7 V - 5 V typically corresponds to the supply of the microcontroller that turns on-off the H-Bridge. The level shifter is shown in Fig.5, MV-PMOS amd MV-NMOS transistors are used in the circuit.

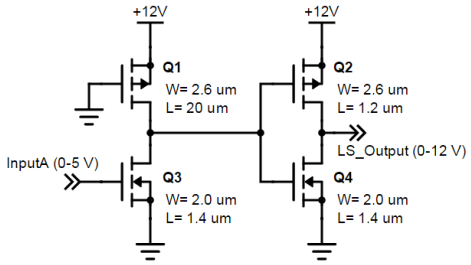


Fig. 5. Level shifter schematic. The input (left branch) operates as in open drain configuration with a pull-up resistor, while the output is a simple MV-MOS inverter.

Nor Gates: In order to meet the behavior of Fig. 2, MV NOR logic blocks are implemented after the Level-Shifters.

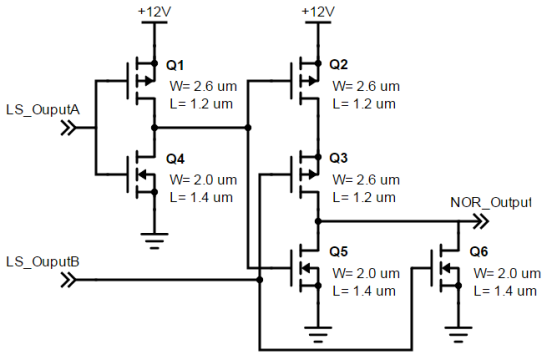


Fig. 6. NOR implementation using PGMV and NGMV transistors.

Delays: The main objective of the delay elements is to avoid short circuit currents on the H-Bridge, preventing transistor damage due to excessive current peaks, and reducing power consumption. These peak currents arise because of the non-immediate transistor shutdown, due to their large size (the larger the transistors are, the higher the capacity they represent is, and it entails in bigger switching time). Considering this phenomenon, delays of a few nanoseconds are implemented (24ns for the signal of PMOS and 21ns for signal NMOS) with two cascaded asymmetrical inverters with the proper size to generate the corresponding delay for each Bridge's transistor.

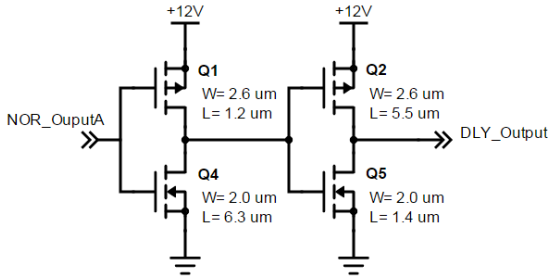


Fig. 7. The Delay circuit block for PMOS transistors.

Drivers: Their function is to handle the gates-entering signals of the transistors composing the H-Bridge. Since such transistors have a large size (to achieve low r_{on} and have small energy losses) it is necessary to condition the output signal blocks delay to be able to put the H-Bridge transistors on saturate state and do not leave them in the linear region, operating improperly in this case and consuming more energy than desired. The drivers are built in two versions with different sizes of transistors to handle the input of the NMOS or PMOS transistors.

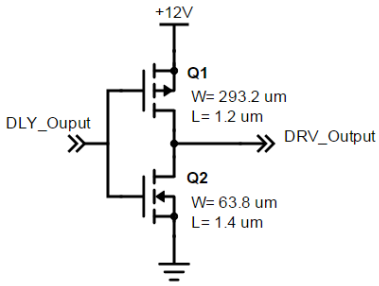


Fig. 8. *Implementation of the Driver block for PMOS transistors.*

IV. SIMULATIONS RESULTS AND FINAL DESIGN

The final layout of the circuit is shown in Fig.11. The area dedicated to logic circuitry is minimal in comparison to the bridge transistors and the metal wires that connect them to the output power PADs. The V_{DD}, GND, and output metal wires were carefully calculated to be wide enough to not aggregate a significant resistance to handle currents up to 1A. To meet the low resistance specifications, it was necessary to stack where possible; the three metal layers available in the process and connect them in parallel.

The four transistors of the bridge were drawn with an approximately square area distribution to minimize the connecting wire resistance. The finger layout recommended by the foundry was adopted dividing in 19 for MV-NMOS and 70 for MV-PMOS). Once the layout design was finished, the circuit was extracted with parasitic to obtain a simulation as realistic as possible. The resistances corresponding to the metal tracks and contacts were considered.

Fig. 9 and Table II, show simulation results for the complete circuit, where many relevant parameters were measured to compare the new H-Bridge with the old one.

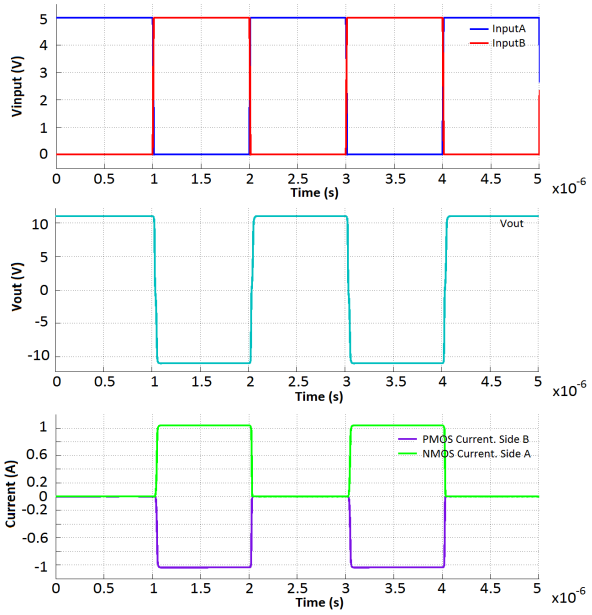


Fig. 9. H-Bridge operation. Upper plot: Square inputs of 5 V and 500 kHz of switching frequency. Middle plot: Differential output between ±11 V. Lower plot: Handled current on both sides of the bridge, 1.1 A.

TABLE II. PARAMETERS COMPARISON

Parameter	Current H-Bridge	Own Chip	Test Conditions
V_{DD}	3.8 V to 13.2 V	2.8 to 12 V	
Operating Continuous Current	1 A	1.2 A	
Input Current	1 µA	<20 nA [1]	InputA = InputB = High
Input Current	-1 µA	<20 nA [1]	InputA = InputB = Low
Output Voltage High	10.7 V	10.6 V	V_{DD} = 10.8 V, I_{OUT} = 500 mA
Input Voltage Low	0.2 V	0.25 V	V_{DD} = 10.8 V, I_{OUT} = 500 mA
Bridge Resistance	0.5 Ω	0.9 Ω	V_{DD} = 12 V, InputA = 5 V, InputB = 0 V
Switching Freq.	200 kHz	500 kHz	V_{DD} = 12 V
V_{DD} Supply Current	2 mA	104 µA	IN = 100 kHz, V_{DD} = 5 V
	300 µA	24 µA	IN_A = IN_B = 4.5 V, V_{DD} = 5.5 V
Propagation Delay Time	300 ns	95 ns	T_{PLH}, V_{DD} = 5 V
	100 ns	35 ns	T_{PHL}, V_{DD} = 5 V

[1] This value was measured by our group using standard and custom PADs for the same CMOS technology up to 5.5V.

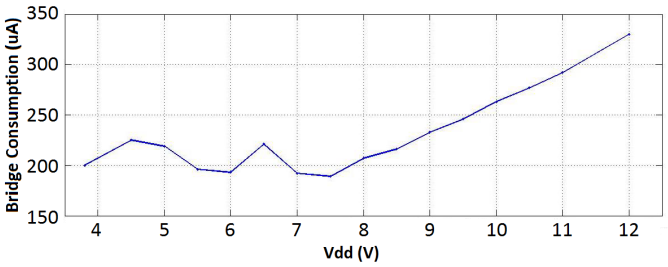


Fig. 10. Simulated current consumption vs Voltage. Input range: 0-3.3 V, Switching Frequency: 200 kHz, Vdd range: 3.5-12 V.

TABLE III. FINAL SIZE OF TRANSISTORS

Dimensions	PMOS	NMOS
L	1.2 µm	1.4 µm
W	44500 µm	9750 µm

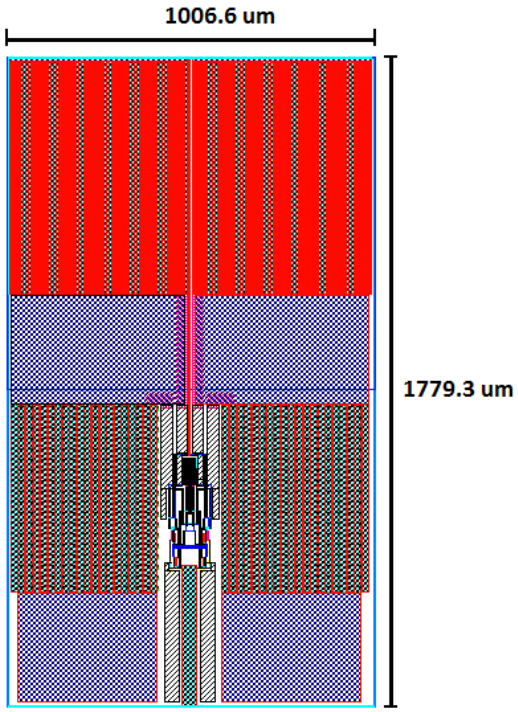


Fig. 11. Final layout design. Silicon area < 1.8 mm^2.

V. CONCLUSIONS

The design of a 2.8 to 12V V_{DD} H-Bridge IC capable to interface with a lower supply voltage microcontroller was presented. This circuit was developed as a pin to pin substitute for an of-the-shelve IC that is being utilized by a company in Uruguay but was announced to be discontinued. The final result has a slightly lower voltage operational range and slightly higher output resistance, but a much better performance on switching rate and power consumption.

The final layout occupies a 1.8 mm^2 area excluding PADs and ESD protection, where the four H-Bridge transistors and metal wires represent a 92% of the silicon area. The layout and transistor size were optimized to reduce silicon area and hence cost. 12V medium voltage transistors with a moderate area were selected, but an up to 60V H-Bridge can be implemented in this HV-technology (with a large area cost) and the output resistance can be reduced with the same medium voltage transistors just increasing their size.

The estimated cost of the designed H-Bridge in a 30k units engineering batch, including masks and SO8 packaging, is a bit lower than the original of-the-shelve equivalent. The cost drastically reduces on large production volumes. But for the company proposing this project, 30k bridges cover few years production. But for example in the application described in [2], also the RFID analog frontend can be integrated with the H-Bridge, with a minimum area overhead. This topology is currently being evaluated.

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