A Programmable Charge Pump Voltage Converter for Implantable Medical Devices in a HV Technology

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***Abstract*—In this paper, a multi-channel, 5bit programmable charge-pump voltage multiplier aimed at charging the output capacitors for the delivery of voltage stimuli in implantable devices, is presented. The circuit was fabricated in a 0.6μm HV-CMOS technology and tested, showing a measured charge efficiency close to 95% of the maximum theoretical value. The individual charge pump channels share the pump capacitors and can be programmed as 1X, 2X, or 3X multiplier. The circuit is capable to operate with a battery ranging from 1.6V to 5.5V.**

I. INTRODUCTION

A high voltage generator is a necessary circuit block in most active implantable medical devices for the stimulation of excitable tissues. Regular stimulation pulses range from hundreds of mV to few tens of Volts while the supply voltage V_{DD} range from 2V (end of life of a lithium-iodine pacemaker-like battery) up to 4.2V (a fully charged rechargeable medical grade battery). Charge pump voltage multiplier (VM) topology is known to be preferred for pacemakers because of its efficiency at a minimum output current [1][2]. While recent published work report efficient switched-inductor converters with μA-order output [3], switching-capacitor charge pumps still dominate pacemakers and most novel medical devices powered with primary batteries. Moreover, non-integrated capacitors in the nF or μF order are used in the VM to avoid fast switching and parasitic effects, and achieve an efficiency above 90%. The basic VM topology used in this work is shown in Fig.1, for a classic 3X voltage generator two pump capacitors C_{P1}, C_{P2}, are alternatively charged to the battery voltage V_{DD} ($\phi1$ is the charge phase) and then connected in series to the battery itself to achieve a $3{\cdot}V_{DD}$ output voltage. At this point the charge is transferred to an output storage capacitor C_{Sto} ($\phi2$ is the pump phase). A DC load can be connected in parallel to C_{Sto}, but in a pacemaker for example, the storage capacitor is just charged up to a target value V_{targ}. Charge stops when V_{targ} is reached and C_{Sto} is discharged later trough the tissue for a short time pulse when a stimulus is required. Finally C_{Sto} is re-charged again with the VM to prepare it for the next stimulus. While charge pumps are well known circuits, there is little detail available about how to switch voltages above V_{DD}. In this paper several practical aspects necessary for the implementation of a VM in a HV CMOS technology are discussed in detail.

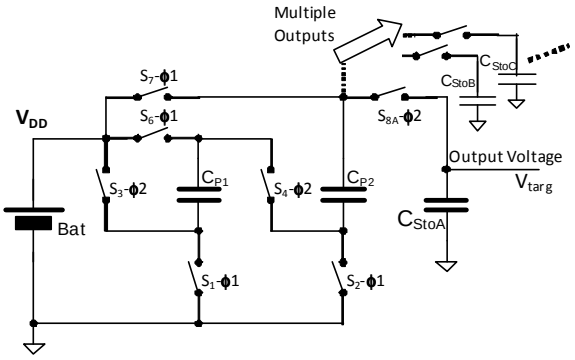


Figure 1. Simplified scheme of a 3X charge pump with multiple output channels. ϕ1 (charge phase) and ϕ2 (pump phase) are non overlapping phases.

A. Charge pump efficiency

Charge pump circuits achieve an efficiency well above 90% but only if the output voltage is a multiple of V_{DD}. In effect note in Fig.1 that in the 3X range, for each charge unit ΔQ pumped to C_{Sto}, it requires 3ΔQ charge from the battery. Therefore the average battery current $\langle I_{Bat} \rangle$ is three times the average output current $\langle I_{Out} \rangle$. Power efficiency η_P and charge efficiency η_Q can be defined as follows:

$$\eta_P = \frac{\langle P_{Load} \rangle}{\langle P_{Bat} \rangle} < \frac{V_{T\arg}}{N \cdot V_{Bat}} = \eta_{P\max} \quad (1)$$

$$\eta_Q = \frac{N\langle I_{Load} \rangle}{\langle I_{Bat} \rangle} < 100\% \quad (2)$$

Where N is the range of the VM (N=3 in the 3X range). From (1) it follows that if $V_{DD} < V_{targ} < 2{\cdot}V_{DD}$ then a voltage doubler (N=2, 2X range) will increase the efficiency respect to 3X

range. The characteristic is well known in the case of pacemakers, where N is adapted to better exploit the available battery power. The VM in this work allows independent range configuration of each output as well as each independent V_{targ}.

B. High Voltage (HV) Technology

The proposed VM can charge an output C_{sto} up to 16V, above the limits of standard CMOS technology, thus a high voltage (HV) process will be employed for the design and fabrication of the circuit. Introducing new process layers, a HV CMOS technology allows devices that can support elevated voltages. Regular 5V core CMOS, as well as double poly capacitors and high-resistivity poly (HPR) resistors can also be fabricated in the target process. In Fig.2 a HV NMOS transistor (named nhv) vertical cut is shown. Nhv has the usual structure of a HV transistor, incorporating a thick gate oxide (up to 18V V_{GS}, V_{GB}), and the drain diffusion is growth into an n-Well to complete a diffused drain that supports V_{DS} voltages up to 60V. In Fig.2 the symbols of the different transistor used in this work (high-medium-low voltage ones) are shown. HV transistors are not symmetrical, the drain which is designed to withstand the highest voltage, is marked with a double line.

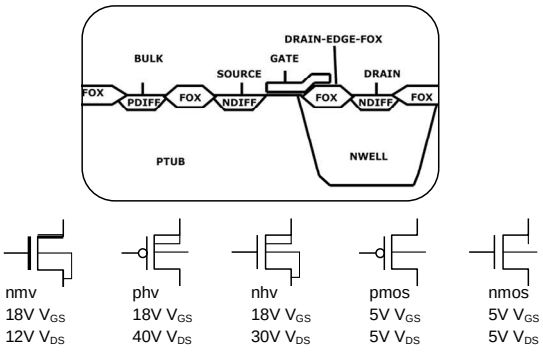


Figure 2. Vertical cut view of a typical HV NMOS (nhv) on top,and the symbols of the different kinds of transistors used in this work below: Medium, high, and low voltage MOS.

II. THE PROPOSED CHARGE PUMP

The VM module is responsible for charging each storage output capacitor C_{StoX} to a desired value V_{targX}. A complete block diagram of the proposed circuit is shown in Fig.3, while the detailed switch section (a single output channel is shown for the sake of simplicity) is shown in Fig.4. The VM is register-controlled, a microcontroller (µC) turns the VM on/off and programs the desired target voltage and range for each channel, as well as global charge speed and full scale value. A 32kHz primary clock is divided by a programmable factor to derive the FSM clock f_{Clk} between 256Hz and 4kHz. Once the µC starts the VM, the finite state machine (FSM) in Fig.3 generates corresponding low voltage control switch signals vector SS={ss1,ss2,ss5,ss7,ss8} for the matrix in Fig.4. The FSM periodically cycles between Charge - PumpA – Charge – Pump B – Charge – Pump C, and so on (Pump states are present only for those active VM channels) but different switches configurations are selected to connect a single (range 1X), two series (range 2X), or two series + battery (range 3X) capacitors. The table on Fig.4 shows the corresponding value of the signal vector (SS) according to the programmed range. V_{targX} can be programmed with 32 voltage steps of $V_{FS}/32$ each, where V_{FS} is the full scale voltage that also is register-configured. Once a given output reaches the corresponding V_{targX} the FSM stops the charge pump of the corresponding C_{StoX}. A voltage comparator with a 5-bit programmable reference is used to determine charge-complete condition after each Pump state. On charge completion of all C_{StoX} the analog comparator is turned off and the clock of the FSM is halted for minimum steady state power consumption.

A. The Voltage Detector

The voltage detector compares each output capacitor voltage to a programmable reference V_{Ref}. The reference is generated from a V_{BGap} = 1.02±1% bandgap consuming only 200nA, which is buffered and connected to a 32 tap resistor divider string inside V_{Ref} generator block of Fig.3 (string implemented with 32 - 400kΩ unitary HPR resistors). A 32:1 analog multiplexer (AMUX) is utilized to select the adequate voltage reference V_{Ref} from the string on each phase of the VM. V_{Ref} is modified each two FSM states and compared during Charge phase to the last pumped C_{Sto}. The output C_{StoX} voltage is scaled with a programmable grounded resistive divider to fit the bandgap range. This output resistor divider is inside the 4:1 AMUX block of Fig.3 and has a minimum 10MΩ series resistance ensuring a negligible leakage current from C_{Sto}. Because V_{Bgap} is fixed, the divider sets VM full-scale. The grounded resistor of the divider has 5 taps to program V_{FS} to be 2, 5, 8, 12, or 16V. A 4:1 AMUX is used to select the active output to compare. The voltage comparator schematic is shown in Fig.5. It is a standard symmetrical OTA to enhance as much as possible the input common mode range. Additionally, the bulks of the PMOS input transistors are deliberately connected to V_{DD}. In this way the V_{GS} of the input pair is larger than that of the NMOS mirrors, due to the Body effect. This effect ensures that the input common mode can be as low as GND for all possible V_{DD}'s and transistor corners. Large W·L=600µm^2 transistor are utilized in the comparator to reduce input referred offset below 2mV to achieve a good voltage precision even after dividing the output through the output resistor divider for the comparison.

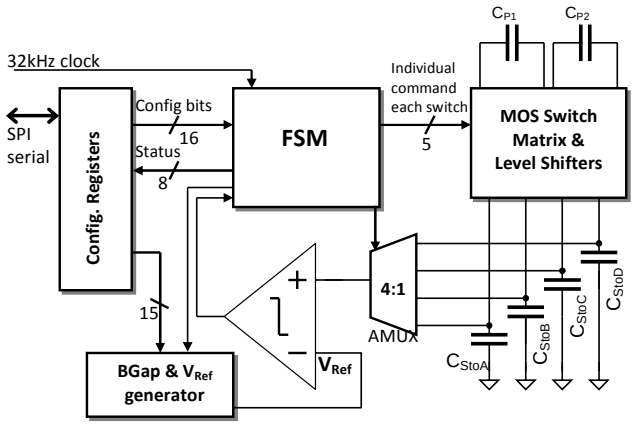
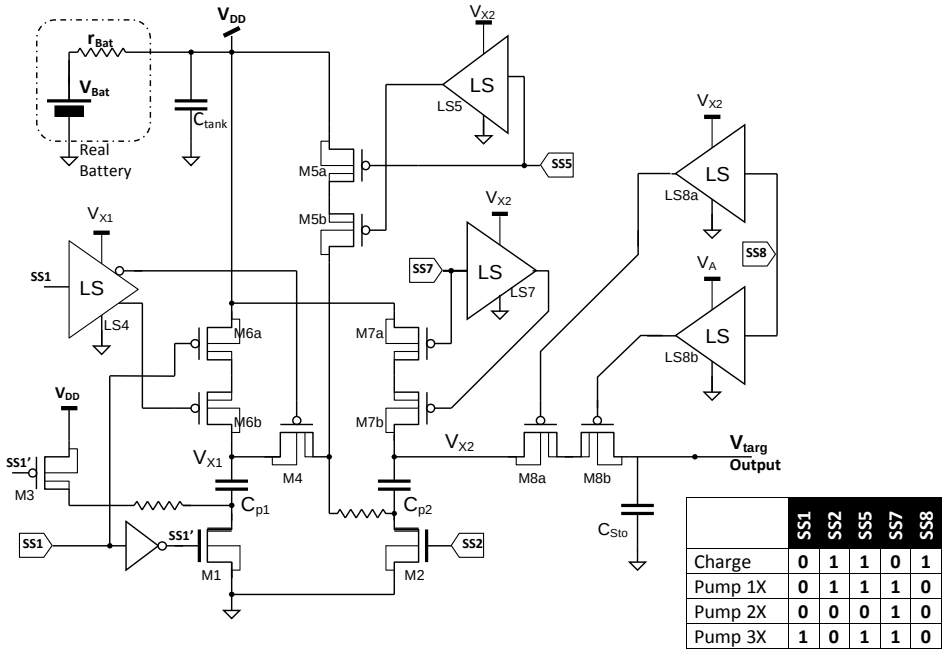


Figure 3. Block Diagram of the proposed Voltage Multiplier.



	SS1	SS2	SS5	SS7	SS8
Charge	0	1	1	0	1
Pump 1X	0	1	1	1	0
Pump 2X	0	0	0	1	0
Pump 3X	1	0	1	1	0

Figure 4. Detailed swithimg section of the charge pump. Only one output shown for simplicity.

B. The Switches

The MOSFETS in Fig.4 are associated to each switch of Fig.1 and Level Shifters (LS) [4] are necessary because a HV signal shall command the transistors. Note that dual switches shall be employed in several places to block current flow in both directions at the off-state. Additionally M5 (M5a and M5b) was introduced to directly connect C_{P2} in series to the battery allowing direct 2X operation at any V_{DD}. Proper LS are connected to the gate of the transistors to translate corresponding SS_X signal. The LS adapt a 0-V_{DD} digital signal, to a 0-V_{High} digital signal at the output. Special LS were designed to allow V_{High} to be any value between 0 and 18V (the LS utilized are similar but complimentary to the one in Fig.8 of reference [4]). In Fig.4 small (120Ω) resistors are connected in series to the current path avoiding undesired current spikes that may introduce noise in analog circuitry. Each switch has been carefully studied to avoid undesired conduction that may trigger latch-up at any circumstance. Transistor sizing were derived from simulated on-resistance r_{ON} curves. While a detailed design space exploration is not possible in this work, in most cases minimum transistor length switches were selected, while the width was chosen to guarantee that total switch r_{ON} in the worst case condition (using V_{DD} and WP, WS, TM models from the foundry) is below a maximum value. M1, M2 switches are nmv transistors sized W/L = 250µm/1.4µm, M5, M6, M7, M8, are phv transistors sized W/L = 600µm/2.5µm (2 series) and M3, M4 are single W/L = 600µm/2.5µm ones.

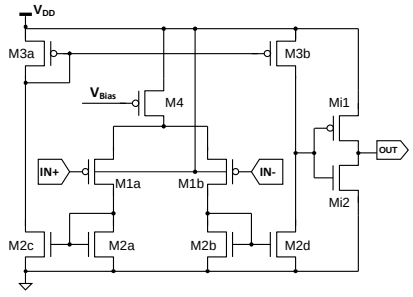


Figure 5. Comparator Schematic

C. Simulation Results

To better understand circuit operation, a simulated simultaneous charge of three capacitors is shown in Fig.6. Note the voltage steps at the output on each pump are not simultaneous. The battery voltage is 2.8V, C_{StoA} is charged at 3X to V_{targA} = 4.55V after 100ms, C_{StoB} is charged at 3X to V_{targB} = 7.5V (does not complete charge in this plot) but C_{StoB} is also discharged at t = 50ms to deliver a stimulus (stimulus condition stops channel B charge that is restarted by the µC at t = 60ms). Finally C_{StoD} is charged at 2X to V_{targD} = 3.8V starting at t = 60ms (the discharge at te beginning is because of an external test current not related to the VM).

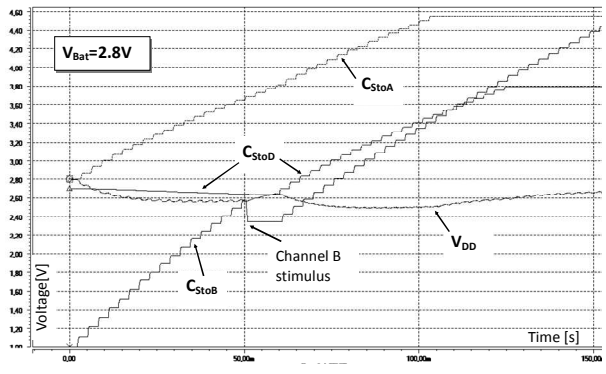


Figure 6. Simulation of three capacitors charge, and V_{DD} efective voltage.

The FSM is operating at a f_{Clck} = 2KHz frequency. Note also the V_{DD} drop during the charge. In effect, primary batteries normally show an elevated series resistance (hundreds or few kΩ) particularly at their end-of-life and a tank capacitor C_{Tank} like in Fig.4 is connected in parallel to withstand a short current pulse demand. But practical C_{Tank} tantalum (low leakage) capacitors are limited in value (100µF for example) and V_{DD} will decrease if the power demand is sustained in time. The effect is more visible after 60ms when the three channels are 'on'. A µC in a real device can handle the clock speed through the proper VM register to make sure V_{DD} does not decrease below any critical value, not only for the VM but for any other subsystem in the device as well.

III. MEASUREMENT RESULTS

The proposed circuit was fabricated in a 0.6µm CMOS-HV technology and tested. Several V_{DD} – range – target voltage combinations were measured and the result closely fit previous simulations, output voltages from 0.5 to 16V with supply voltages from 1.6 to 5.5V were tested (of course maximum target shall be below $3 \cdot V_{DD}$). In Fig.7 a microphotograph of the VM is shown, while in Fig.8 an acquired simultaneous charge of 3 channels (V_{targA}=4V, V_{targB}=5V and V_{targC}=6V) is presented. V_{DD}=3.3V, $C_{p1,2}$ = 220nF and C_{StoX} = 10µF in this experiment. The maximum VM clock speed of 4kHz was selected but the voltage steps of C_{StoX} still can be seen in the picture. Note that the output capacitor voltage resembles an exponential charge but after a capacitor completes its charge, the remaining capacitors charge faster because the FSM re-assigns the Pump time slots. In the Table I, several circuit characteristics are summarized. A pacemaker operation was emulated also, to measure the efficiency of the VM. Individual or multiple C_{Sto} are periodically charged and then discharged through a 500Ω resistor for a couple of ms. The battery average current, and C_{Sto} initial/final voltage is measured. Few typical efficiency measurements are shown in Table II (using four stimuli/second, single channel).

TABLE I. CIRCUIT CHARACTERISTICS

Charge pump characteristic	
Supply Voltage	1.6 – 5.5V
Output Voltage	Up to 16V
Circuit area [(a)]	1.7 mm^2
Active DC Current consumption	600 nA

(a) PADs & Resistors included, capacitors are external
(b) All analog 'on' including Bandgap, no switching.

TABLE II. MEASURED EFFICENCY

Efficiency			
Condition	η_Q	η_P	η_P/η_{Pmax}
V_{DD}=3.3V, V_{Targ}= 8.2V, N = 3X	96%	73%	89%
V_{DD} = 2V, V_{Targ}= 5V, N = 3X	98%	74%	89%
V_{DD}=2.8V, V_{Targ}= 5V, N = 2X	96%	79%	89%

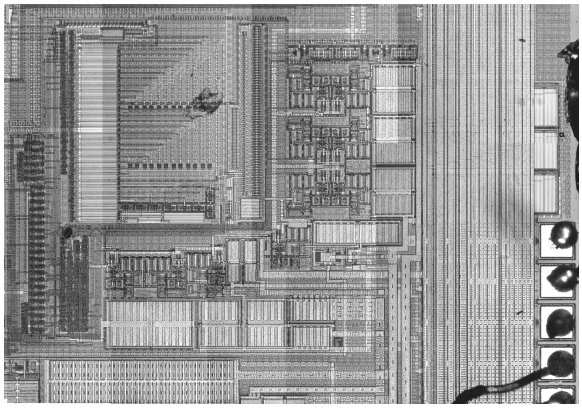


Figure 7. Microphotography of fabricated circuit.

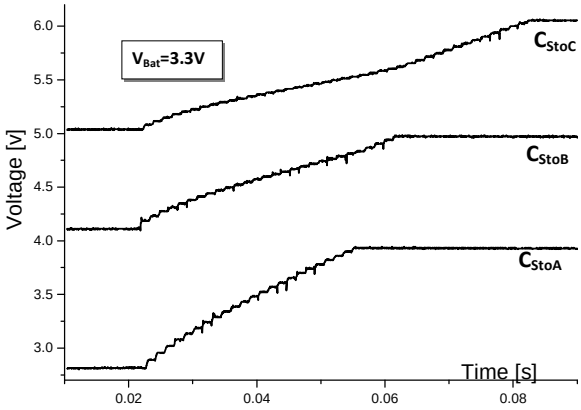


Figure 8. Measured capacitor charge.

IV. CONCLUSIONS

A multi-channel integrated 5bit programmable charge-pump voltage elevator circuit was presented. The charge pump utilizes external capacitors to maximize its efficiency sharing also pump capacitors, and can operate up to 3X range. Target voltage, range, speed, full scale, can be programmed by an external microcontroller to better adjust the circuit for a given medical device. The circuit was fabricated in a 0.6µm HV-CMOS technology and tested, showing a measured efficiency above 95% in charge and close to 90% of the maximum power theoretical value.

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