Blind range level shifters from 0 to 18V.

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***Abstract*— In this work the design, simulation and measurement results of high voltage level shifters (LS) is presented. A modification is introduced to the standard LS, and a design criterion was developed, for the level shifter to work in a very wide range of operation from 0 to 18V. Also, safety issues where addressed when the level shifters are used to deliver stimuli to biological tissue in medical devices.**

Keywords—Level Shifter, high voltage CMOS, medical devices.

I. INTRODUCTION

A Level Shifter (LS from now on) is a circuit block that translates standard logic levels between two domains for example $\{0,V_{CC}\}$ to a usually higher voltage $\{0,V_H\}$. In Fig.1 a standard level shifter [1] [2] is shown translating the logic '1' from V_{CC} to V_H. This circuit is preferred due to its simplicity, speed, and because has no static power consumption. V_H can be very large, up to the maximum V_{GS} that $M_{1\text{-}6}$ can withstand; to translate higher voltages current signalization is necessary at the penalty of a higher static power consumption [1]. In this work we are assuming high voltages up to 18V for V_H thus HV, thick oxide CMOS transistors will be utilized as depicted in Fig.1. LS can be useful in several applications: they can translate voltages to communicate for example a V_{CC}=1.8V CPU to a 5V peripheral (in this case V_{CC} and V_H are fixed), or can command the gate of a high-side pass transistor in switching converters, or in medical devices for stimuli delivery systems to tissue [3] among others. While in the first example the design of a LS is simple, the latter becomes a challenging problem because normally V_H is a 'blind' voltage, V_H can be either 15V, 5V or 300mV, either above or below V_{CC}. This work will focus in the implementation of blind LS with a wide input and output voltage range aimed at being part of medical circuits. The stimuli to deliver to tissue in medical devices are either current or voltage pulses (or pulse trains) to the patient, ranging from a few hundreds of mV to well over 10V voltage, or from a hundred μA to tens of mA. The stimuli section of the circuit may consist of the basic elements shown in Fig. 2: a voltage/current source, electrodes connecting the tissue to the device through a pass-switch, sensors and an intelligent control logic deciding when and for how long a stimulus should be applied. A LS can be used to open/close the switch in Fig.2.

In this work, different Level Shifters will be presented in a wide range for V_H=0-18V, V_{CC}=1.8V-5.5V, including design criteria, simulations, and measurement results. A final example is presented, an inverting-LS to safely deliver stimuli to tissue with a programmable amplitude (safe means in compliance with [4]).

II. FULL-RANGE LEVEL SHIFTERS

The target process in this work is a 0.6μm-HVCMOS with thin and thick oxide transistors (V_{GSmax}=18V for the latter), and several HV transistors with a diffused drain withstanding up to V_{DSmax} = 40V. Diffused drain and thick oxide transistors are indicated in Fig.1. Ideally, V_H must range from 0 to 18V (maximum V_{GS} in this technology), and V_{CC} must cover different types of battery powering the control CPU from 1.8V up to 5V. The "In" signal in Fig.1 controls the output "O_{UT}" which toggles from 0V to V_H. The LS itself is formed by the LV inverters and $M_{1,2,4,5}$ while M_3 and M_6 are large output transistors adequately sized for the load. The LS works as follows,

- "High" state: When the "In" signal is set to V_{CC}, transistors $M_{1,5,6}$ are turned on and $M_{2,3,4}$ is turned off making the output "Out" go to V_H.
- "Low" state: When the "In" signal is set to 0V transistors $M_{2,3,4}$, are turned on and $M_{1,5,6}$ are turned off making the output "Out" go to 0V.

The working logic is fairly simple. At a first sight the transistors size would be set: $M_{3,6}$ by the load at the output and all the HV transistor sizes will be set to de same value (W/L=10μm/3μm because L_{min}=3μm). V_H has a very wide range of operation from 0 to 18V, so three cases of study are presented, V_H close to V_{CC}, V_H much smaller than V_{CC} and V_H much larger than V_{CC}. In Fig. 3 the simulation result of these three cases are shown. Note in this first approach the LS properly works only in the case of V_H close to V_{CC}.

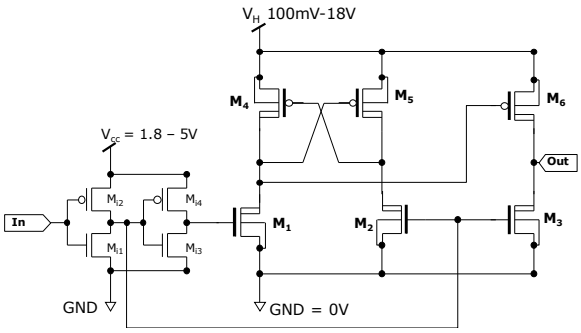

Fig. 1 Standard level shifter (LS) schematic.

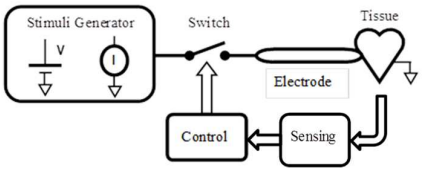

Fig. 2 Schematic of a stimuli system (top), level shifter block diagram (bottom)

A. V_H much larger than V_{CC}

According to Fig.3, if all the HV transistors are the same size then the LS doesn't work for V_H values much higher than V_{CC}. When the LS changes from the "Low" state to the "High" state M_1's gate changes from 0 to V_{CC} turning on the transistor. At this point M_1 is saturated because V_{DS1} is V_H much larger than a 300mV standard saturation value. M_4 transistor starts in the linear zone because $V_{DS4}\approx 0V$ (remember that the LS comes from the "Low" sate). The gate capacitance C_{G5} of M_5 is discharged then, until at some point the drain currents of M_1 and M_4 are equal. In a first approach, to guarantee that the LS is triggered, the intersection point of both I_{D4} , I_{D5} currents as depicted in Fig. 4, must be larger than $|V_{TP}|$; if this condition is not met M_5 and M_6 will not turn on. To develop a design criteria to size the LS to properly operate at any voltage condition first consider the inverter (M_{i3}-M_{i4}) imposing $V_{GS1}=V_{CC}$. Assuming M_1 transistor is saturated, in Strong Inversion (SI):

$$I_{D1} = \beta_1 \frac{(V_{GS1} - V_{TN})^2}{2} = \beta_1 \frac{(V_{CC} - V_{TN})^2}{2}, \quad (1)$$

Assuming M_4 transistor in lineal zone, and because the LS comes from the "Low" state, $V_{GS4} = V_H$ therefore:

$$I_{D4} = \beta_4 (V_{GS4} - V_{TP}) V_{DS4} = \beta_4 (V_H - V_{TP}) V_{DS4}, \quad (2)$$

In this point M_2 is open and V_{DS4} is fixed just by the charge in the parasitic capacitance C_{G5} in the node V_{G5}. While (I_{D4}-I_{D1}) is positive C_{G5} is discharged:

$$V_{G5}(t) = V_H - \frac{1}{C_5} \int (I_{D1} - I_{D4}) dt \quad (3)$$

When (V_H-V_{G5})>V_{TP} is possible to assume that M_5 is turned on and the LS rapidly completes state change. But if solving ec.(3) V_{G5} reaches a steady voltage (V_H-V_{G5}) < $|V_{TP}|$ where M_5 and M_2 leakages are equal, the LS will not change its state remaining in a metastable condition. A complete analytical solution to eq.(3) is complex because should consider also a coupled-analogous equation for V_{G4}-$C_{G4,6}$, but it is possible to establish a simpler criterion for the LS to properly change state. In effect if at $V_{DS4}=V_{TP}$, $I_{D1}>I_{D4}$, then it is certain that the LS will change state; thus a good trade-off for transistor sizing is to make the intersection point of M_1 and M_4 drain currents in Fig.3 to be at$V_{DS4}=V_{TP}$. From eq.(1) and eq.(2):

$$\beta_1 \frac{(V_{CC} - V_{TN})^2}{2} = \beta_4 (V_H - V_{TP}) V_{TP} \quad (4)$$

with $\beta_1 = \mu_N C'_{OX} \frac{W_1}{L_1}$ and $\beta_2 = \mu_P C'_{OX} \frac{W_4}{L_4}$. Then the ratio between M_1 and M_4 transistor sizes can be determined by

$$\frac{W_4/L_4}{W_{1/L_1}} = \frac{\mu_N}{2\mu_P} \frac{(V_{CC} - V_{TN})^2}{(V_H - V_{TP}) V_{TP}} \quad (5)$$

Ec.(5) shall be examined for a worst case condition, to set a criterion for transistor sizing. In this work all HV transistor lengths are set to the same value (the minimum value allowed by se selected technology) and worst case to examine is V_{CC}=2V (end of life primary battery for medical devices [5]) and V_H =18V resulting for the target technology,

$$\frac{W_1}{W_4} \approx 6.6 \quad (6)$$

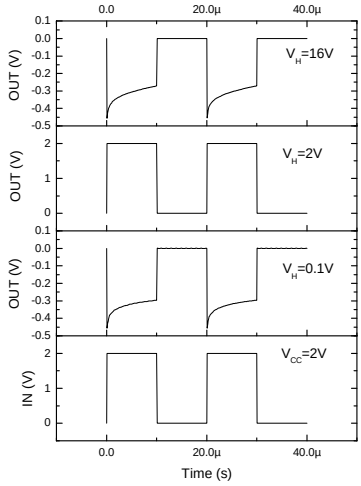

Fig. 3 LS transient simulation for V_H much smaller, close to and much larger than V_{CC}.

According to eq.(6), $M_{1(2)}$ aspect ratio must be between 6 and 7 times that of $M_{4(5)}$. It should be pointed that eq.(6) is not a hard limit since eq.(4) is an overestimated criterion to guarantee LS transition, that can be fine-tuned during simulations.

B. V_H smaller than V_{CC}

In Fig. 3, it is clear the LS does not properly work for V_H values much smaller than V_{CC}. The reason is that V_{GS} = V_H will not be enough to turn on the PMOS HV transistors when necessary. The on-resistance R_{ON} of $M_{4,5,6}$, drastically increases as V_H gets closer to GND. Our proposed solution to this issue as depicted in Fig.5, is to connect NMOS HV transistors ($M_{7,8,9}$) in parallel with the PMOS HVs resembling a transmition gate (TG) configuration, but the gate of these HV-NMOS is controlled in the V_{CC} domain. When V_H is high $M_{7,8,9}$ are transparent to the circuit behaving open, but they take the role of the PMOS when V_H becomes too low. The new configuration of the LS in Fig. 5 will be denoted as Full-Range level shifter or simply FR-LS. In Fig. 6 transient simulations are presented for a FR-LS showing proper operation at low and high V_H values.

C. Design Methodology

Summarizing, the following design methodology is proposed for FR-LS:

-First determine the size of M_3 and M_6 according to the load, calculate both gate capacitances, and determine the minimum width (assuming minimum Length) of the $M_{1,2,4,5,}$transistors to drive this load at a reasonable speed and V_H close to V_{CC}.

- Increase $M_{1,2}$ width in compliance with ec.(6)

- To complete a FR-LS determine the size of M_7, M_8, M_9 in a worst case with V_H = 0V.

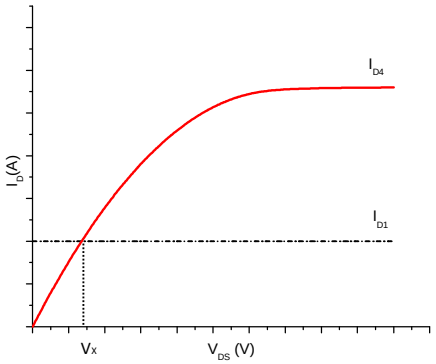

Fig. 4 I_D vs. V_{DS} for transistors M_1 and M_4 of the LS of Fig. 1

III. FABRICATED LEVEL SHIFTERS

Several Level Shifters were fabricated to test performance:

A. Standard Level shifter (LS)

A standard level shifter (Fig. 1) was implemented, in TABLE I a summary of transistor sizes is shown. The output HV transistors $M_{3,6}$ are large to handle a 200pF load. This LS was measured for V_{CC}=2V and V_H from 100mV up to 16V, the results are presented in Fig.7. Also, the LS delay was measured for a 200pF load for V_{CC} from 2V up to 5V, the results are shown in Fig. 9. As expected this LS work properly work for V_H values close and much larger than V_{CC}, but it did not work for V_H values much smaller than V_{CC} because it lacks the TG-like configuration shown in Fig. 5. The delay 0-V_H is independent of V_{CC} and the V_H-0 changes with V_{CC} as shown in Fig. 9 because M_6 transistor R_{ON} is independent of V_{CC} but M_3 transistor R_{ON} is V_{CC} dependent.

B. Full range Level shifter (FR-LS)

Using the design criterion of section II.A and II. B. a full range level shifter (Fig. 5) was implemented, in TABLE I a summary of transistors sizes is show, the output HV transistors ($M_{3,6}$ also sized for a 200pF load). This FR-LS was measured for a V_{CC}=2V and V_H from 100mV up to 16V, the measurements results are shown in Fig. 8. Also, the FR-LS delay was measured for a 200pF load for V_{CC} from 2V up to 5V, the results are shown in Fig. 9. The FR-LS work as expected, in the full range of V_H. The measured delay 0-V_H and V_H-0 changes with V_{CC} as shown in Fig.9, because in both cases a NMOS HV transistor is present.

C. A Safe Full range Level shifter (SFR-LS) for a medical application.

In Fig. 10 a possible stimuli delivery system is shown, where the tissue is connected to stimuli voltage V_{STIM} through the FR-LS of Fig. 5 (V_{STIM} can vary from 100mV to 16V) and is connected to GND when not stimulating (common GND device). When delivering stimuli, M_8 in Fig.5 is connected to V_{CC}. In case of a single failure event (gate of M_8 in Fig.5 punctures for example) a harmful DC current will flow through tissue not complying with safety rules [4] in medical devices. In Fig. 11 the schematic of a safe full rage level shifter (SFR-LS) that addresses this safety issue is presented. The solution consists in placing resistors ($R_{1,2,3,4}$, integrated high resistivity poly ones in series) with $M_{7,8}$ gates so in case of gate rupture the DC current will be limited to a few µA. The integrated capacitors $C_{1,2,3,4}$ are placed (two in series in order to support maximum applied voltages) in parallel to the resistors to improve the response time of the SFR-LS. A command pulse goes quickly through the capacitor and is its value is held by the resistors, in TABLE I a summary of the circuit elements are shown. In Fig. 12 a microphotography of the SFR-LS is show.

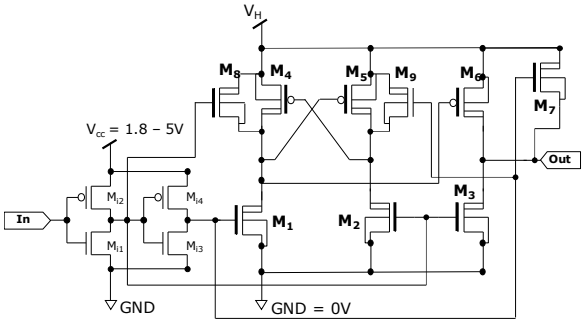

Fig.5 FR-LS schematic.

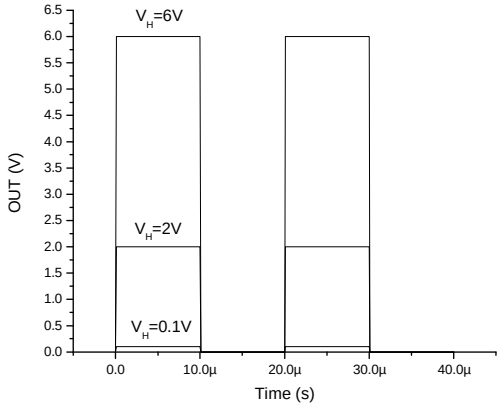

Fig. 6 FR-LS transitory simulation with V_{CC}=2V.

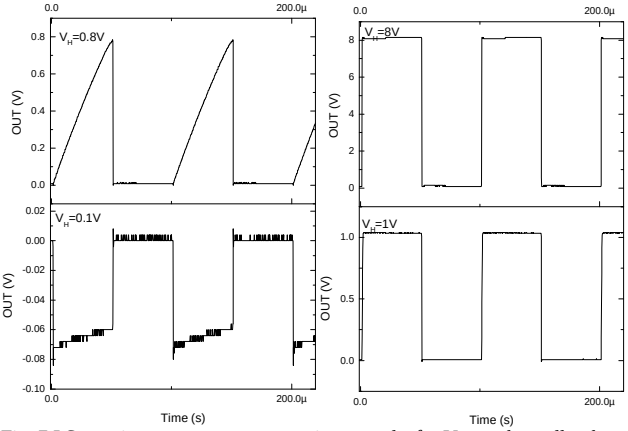

Fig. 7 LS transitory measurement transitory results for V_H much smaller than V_{CC} (left) and close/much larger than V_{CC} (right) with V_{CC}=2V.

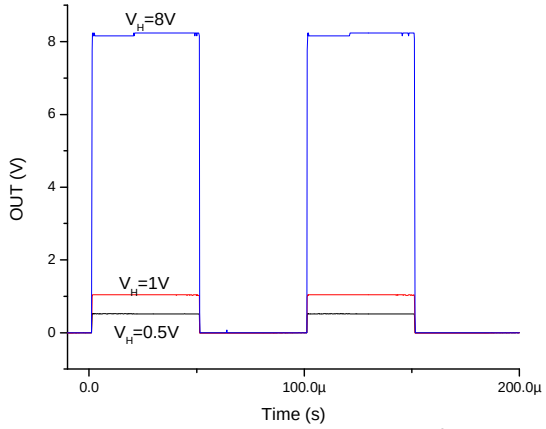

Fig. 8 FR-LS transitory measurement transitory results for V_{MAX} much smaller than V_{CC}, close and much larger than V_{CC} with V_{CC}=2V.

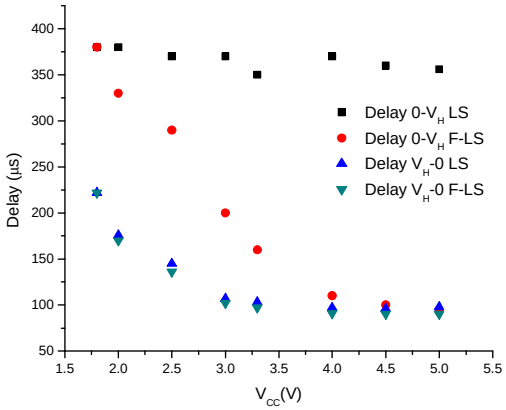

Fig. 9 Measured delay of the LS and FR-LS with 200pF capacitive load with V_H=16V.

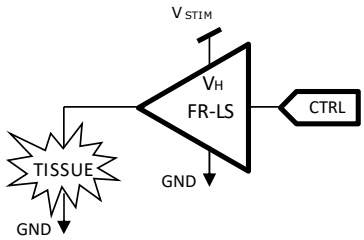

Fig. 10 Stimuli delivery system.

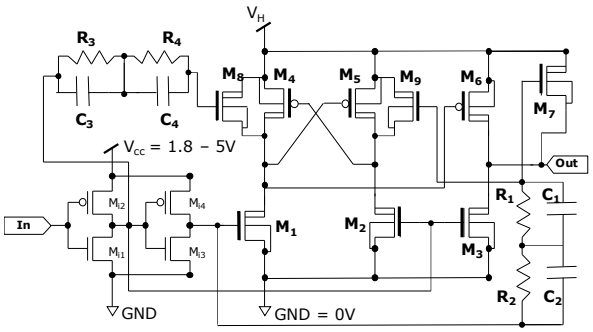

Fig. 11 SFR-LS schematic.

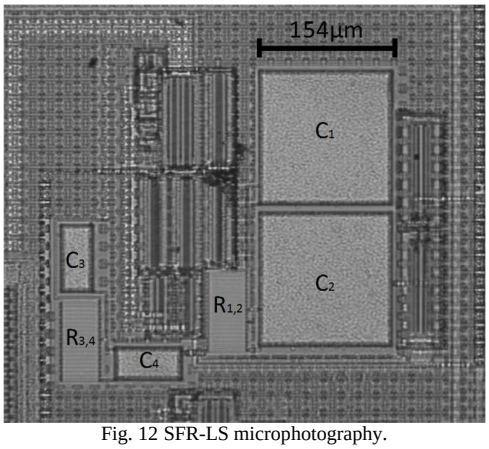

Fig. 12 SFR-LS microphotography.

TABLE I. LEVEL SHITFERS TRASISTOR SIZES AND INTEGRATED COMPONENTS VALUES

Transistors	**W/L (µm/ µm)**
M_{i1-4}	20/3
$M_{1,2}$	60/3
$M_{3,6}$	400/3
$M_{4,5}$	10/3
M_7 (F-LS,SF-LS)	400/3
$M_{8,9}$ (F-LS,SF-LS)	10/3
Component	**Value**
$C_{1,2}$ (cpoly-poly) (SF-LS)	20pF
$C_{3,4}$ (cpoly-poly) (SF-LS)	5pF
$R_{1,2,3,4}$ (rpolyh) (SF-LS)	500kΩ

IV. CONCLUSIONS

In this work the design, simulation and measurement results of three different level shifters were presented. At first glance the design seems simple but as shown in Section II, in order for the level shifter to work in a wide range of operation a modified topology, and carefully transistor sizing are necessary. Finally, a full range level shifter for an output 'high' from 0 to 18V in compliance with safety rules provided by [4] was presented.

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