Step Down DC/DC converter for Micro-Power Medical Applications

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***Abstract*—In this work, a step down DC/DC converter aimed at reducing the supply voltage in implantable medical devices is presented. The circuit was designed and fabricated in a 0.6 µm technology. The DC/DC converter was tested for a wide range of input voltages between 1.9V and 5V, output voltages between 200mV and 1.5V, and different load currents between 50µA and 200µA. In all cases the output voltage was regulated with less than 3% error and 5% ripple. The simulated efficiency varied between 60% and 75%, but the measured efficiency was 40%.**

Keywords—DC/DC converter, low power, medical applications

I. INTRODUCTION

In recent years, there has been a remarkable increase in the research and development of new implantable devices for the treatment of different pathologies. A major requirement for all implantable devices is the efficient use of the energy stored in the battery. For rechargeable implants, low power consumption increases the time between charging, improving patient's comfort and device reliability. For active implants with a primary battery, a change of battery requires a minor surgical procedure, therefore the battery must last as long as possible. Different methods have been suggested to reduce power consumption of implantable electronics; one of the simplest, and the most effective is reducing the supply voltage V_{DD} as much as possible. In the case of digital circuits it is well known that power consumption is proportional to V_{DD}^2. Analog circuits may also benefit from a low V_{DD} because the performance in terms of noise, and bandwidth, among other characteristics, is generally related to current consumption rather than to power consumption [1].

In most cases of implantable applications, the power supply is either a primary battery of approximately V_{BAT} = 2.7V nominal voltage, or a rechargeable one of approximately V_{BAT} = 4.2V nominal battery voltage. V_{BAT} may vary by a few hundreds of mV during normal operation from beginning to end of battery life/charge. On the other hand, modern digital circuits can be powered with a V_{DD} as low as 0.9V or even less for an off the shelf microcontroller [7], meanwhile, very low voltage processors have been reported in several research papers like [4][8]. Many high performance analog amplifiers, filters, and ADCs, with a supply voltage starting at a few hundred mV have been also reported. Because the battery voltage V_{BAT} is fixed (given by the battery's technology), V_{DD} must be much lower to fully exploit the available battery power.

To reduce the supply voltage in a medical implantable device, an efficient DC/DC converter must be included, with a typical load power consumption restricted from a few to a few hundred µWatts. DC/DC converters are employed in most electronic devices, but very few micro-power applications are reported. DC/DC converters can be classified into switched capacitor (charge pumps) and switched inductor converters. Charge pump have been traditionally employed for implantable electronics and other ultra-low-power applications [1][2][3]. These are used for the sake of simplicity, and because efficiencies close to 90% or more can be achieved for power consumption in the range of µWatts or less. However, charge pumps regularly require the use of a large number of external capacitors (in the case of efficient micro-power converters), and V_{DD} is limited to certain fixed values. Inductive DC/DC converters instead require only two external components (an inductor and a capacitor) and a single output pad. Traditionally these kind of converters have been limited to power consumption above 1mW in the best case. While there are thousands of integrated circuits and complete modules in the market implementing switched-inductor DC/DC converters, it is only very recently that a couple of commercial products [5][6], and a few published circuits (like the one in [4]) have been reported, implementing micro-power DC/DC converters with efficiency (efficiencies $\eta \approx 60$-90% are reported in the cited references). In [4] a micro-power inductive DC/DC converter is presented, that supplies voltage for the digital core of a medical system-on-chip with V_{DD} ranging from 0.5V to 1.0V that achieves its best efficiency close to 90%. However, the efficiency strongly depends on the operating point.

In this work, a micro-power inductive DC/DC step-down converter is presented, aimed at powering a low noise amplifier that consumes I_{DD} = 20µA with a supply voltage of V_{DD} = 0.6V. The strategy presented in [1] is used to minimize the power consumption of the amplifier. In addition a discontinuous-conduction-mode inductive DC/DC converter will substitute the charge pump converter, to minimize the number of circuit pads. The proposed DC/DC converter follows the topology presented in [4], but a different control strategy is used to avoid the appearance of spectral components of the switcher within the range interest of the signal to be

amplified (200Hz - 5kHz). The circuit was fabricated in a 0.6µm technology, and tested.

II. Design

A. Step down DC/DC converter

The basic topology of a step down DC/DC converter is shown in Fig. 1. The switch SW_1 is periodically closed at the beginning of phase A, connecting the battery to the inductor. In this phase the battery (V_{in}=V_{Bat}) discharges into the inductor that stores energy while it current increases; the capacitor replenishes its charge while the inductor's current is larger than the load current.

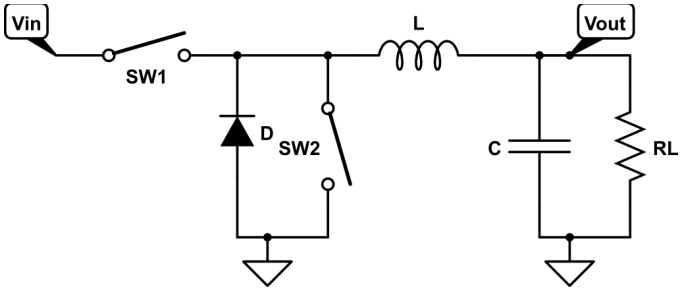

Fig. 1. Topology of a standard step down DC/DC converter

When the switch opens, phase B starts. The current continues to flow through the inductor that forward-bias the diode. In this phase the energy stored in the inductor is transferred to the capacitor and the load. To control the output voltage, the switching frequency and the time that the switch is closed (t_P) can be varied. To reduce the voltage drop in the diode, a second switch SW_2 is connected in parallel with D, SW_2, which must be closed a short time after SW_1 opens and opened when the current through the inductor is zero (to prevent draining of current from the capacitor). Fig. 2 shows an ideal plot of the current through the inductor. During phase C, both switches are open and the load drains current from the capacitor.

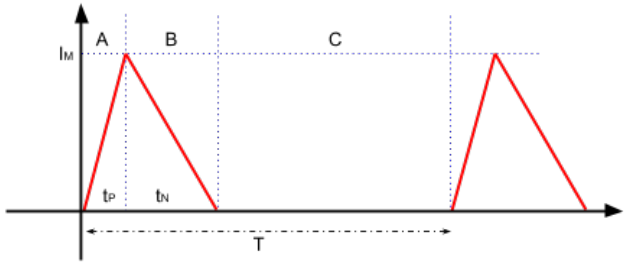

Fig. 2. Current through the inductor L in a step down DC/DC converter A- SW_1 closed SW_2 open; B – SW_1 open SW_2 closed; C- SW_1 and SW_2 open.

If we assume there are no losses, the output voltage can be calculated by equating the input power to the output power. After some calculations:

$$V_{OUT} = \frac{R_L V_{IN} t_p^2}{4LT}\left(\sqrt{1+\frac{8LT}{R_L t_p^2}}-1\right) \qquad (1)$$

where R_L is the load (modeled as a resistor), t_p is the time the switch SW_1 is closed, L is the inductance and T is the switching period, as defined in Fig. 2. Equation (1) shows that the output voltage is a function of the load; therefore, an active control mechanism is required. In general this mechanism includes a low-power comparator, to compare between an external reference voltage V_{Ref} with V_{OUT}, and a feedback loop to null the error signal.

B. Designed Circuit

The complete implemented circuit is shown in Fig. 4. It consists of an output stage SW_1-SW_2, a comparator, a zero-crossing detector (ZCD) and the control logic. The output stage comprises two large transistors (the PMOS is SW_1 and the NMOS is SW_2, having W=100µm and L=1µm) that are turned on/off by the control circuit.

The zero-crossing detection was adapted for this application based on the one implemented in [4]. The comparator was implemented using an uncompensated miller amplifier, similar to the one presented in [9], while the inductor (L=100µH) and capacitor (C = 47nF – 200nF) are external components. A 50nA current source is required for the comparator. Fig. 3 shows the schematic of the comparator and the ZCD circuit.

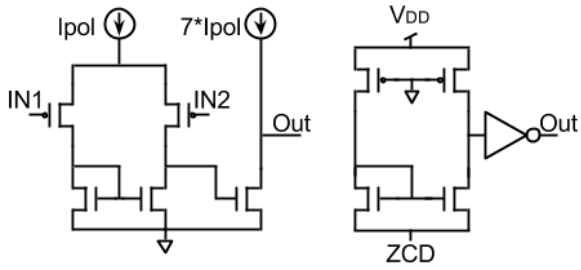

Fig. 3. Schematic of auxiliar circuits. Left the comparator. Right the ZCD circuit.

The control block is a digital circuit that begins operation on the negative edge of the digital input STR. It shall firstly close the PMOS switch for a fixed time of approximately 100ns (phase A). This time delay was generated using an asymmetric inverter chain [10]. After the PMOS switch opens, the NMOS switch closes, and it remains closed until the zero-crossing detection circuit indicates that the current through L is zero (phase B). Finally, the NMOS switch opens, and the circuit waits a fixed time of approximately 250ns before checking the comparator. The control logic then checks if the output voltage falls below the reference, to determine if another pulse is required. As the comparator is slow (to reduce consumption), the system delivers several pulses in a short burst, and then becomes idle for a longer time while the capacitor discharges. This strategy of pulse bursts pushes the switching frequency well above the load's bandwidth. A regular distribution of the pulses, usual in this family of converters, was also simulated, and it interferes in some cases with the 200Hz-5kHzband of interest. On the other hand, the proposed strategy results in a higher ripple.

C. Micro-Power Considerations

For this micro-power DC/DC converter, efficient blocks consuming as little as possible are required. The comparator was designed to consume less than 2µA in normal operating conditions. The ZCD circuit consumption is higher, so to reduce its consumption bellow 2µA it only turns on as required (during phase B). Finally, the low power logic family standard cell library provided by the foundry was used for the control circuitry.

A dead time was introduced to guarantee that both switches are not simultaneously on under any circumstances. The dead time ensures that SW_1 opens before SW_2 closes. During the dead time, the inductor's current flows through the parasitic diode of SW_2.

An efficient inductor with low resistance [11] and a low leakage capacitor were used in the circuit for test purposes.

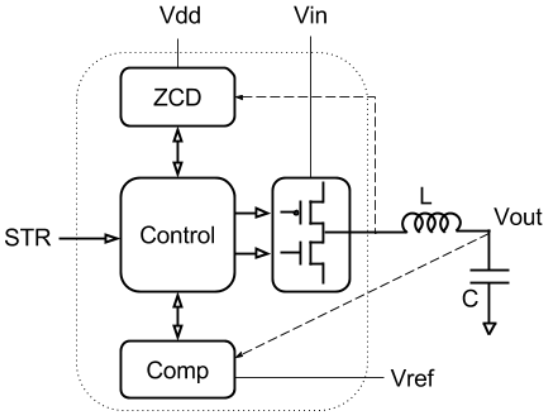

Fig. 4. Topology of the designed DC/DC converter. The pointed line indicates the limits between the integrated and not integrated parts of the circuit. The supply voltage (V_{DD}) may be different that the input voltage (Vin) In this circuit the PMOS is SW_1 and the NMOS is SW_2.

The circuit occupied a total die area of 150µm by 250µm excluding pads, and a total die area of 1000µm by 650µm including pads and all ESD protections. The circuit was located in the corner of a MPW die, as shown in Fig 5.

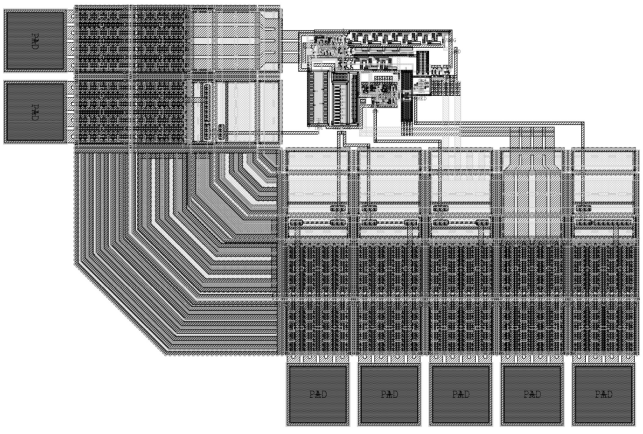

Fig. 5. Layout of the DC/DC converter. The cicuit was fabricated in a multi project chip. Only the bottom left corner shown.

III. MEASUREMENTS

The circuit was fabricated in a 0.6µm process, and tested under several operating conditions. The output follows in all cases the reference voltage with less than 10mV error. Unless noted, the typical test condition was an input voltage of 3.3V, an output voltage of 0.6V, and a resistive load of 6.5kΩ at the output resulting in a nominal output power of 55µW. Figure 6, shows the line regulation, with a reference voltage V_{Ref} = 0.62V (gray line). The DC/DC converter exhibits a variation of less than 5mV for an input voltage range from 1.8V to 5V.

The reference voltage V_{Ref} was varied, while keeping a fixed input voltage of 3.3V, to evaluate the wide range of output voltages that can be achieved. Figure 7 shows the difference between the reference voltage and the output voltage, which is always less than 10mV.

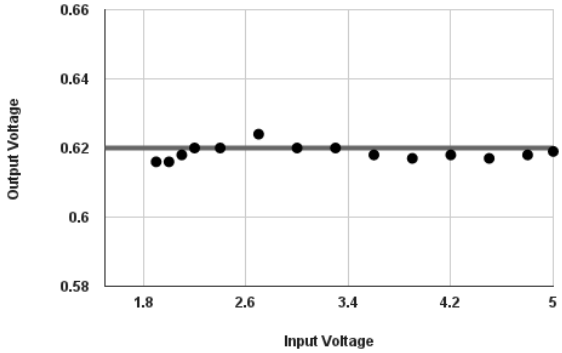

Fig. 6. Output voltage in terms of the input voltage, note the output is almost independent of input.

Figure 8, shows a close up of the output voltage waveform with a reference V_{Ref} = 1.03V. In the positive slope, the capacitor is being charged by a pulse burst, while the descending slope, corresponds to the discharge of the output capacitor trough the load. The ripple voltage is 50mV (around 5%) as expected, with a 20kHz frequency, above the 5kHz requirement. The measured efficiency was $\eta \approx 40\%$for most of the tested configurations. This efficiency is lower than the expected 60-75%.

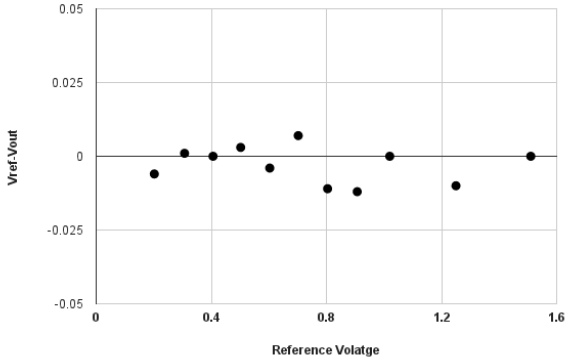

Fig. 6. Difference between the reference volatge and output voltage, as a function of the reference volatge for a constant input voltage and load.

With a 3.3V supply voltage, 0.64V output voltage and a resistive load of 6.5kΩ, the simulated efficiency was 70%. In

the same test condition the measured power consumption of the control loop (all the circuits except the output stage) was 21µW, which is similar to the simulated 19µW. The output power was 63µW, but the power consumption through the output stage was measured as 135µW (separated supply pad were included for the control loop and output stage), resulting in an efficiency of only 40%. While the measured efficiency is still much better than using a linear regulator or powering the amplifier with the battery voltage (> 19% efficiency) it is still much lower than expected. The efficiency was measured for different input and output voltages and for different loads, always with similar results (around 40%), attributable to the output stage consumption.

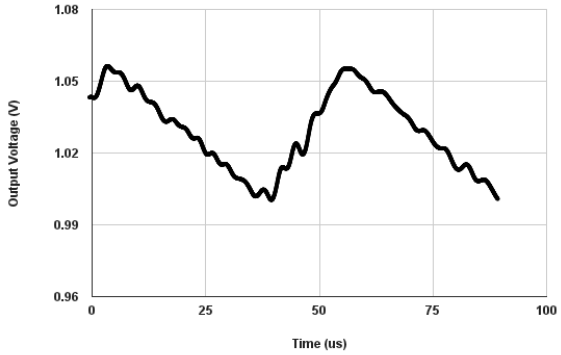

Fig. 7. A detail of a measured output voltage transient showing 50mV ripple @ 19kHz.

Since the missing energy is lost in the switches, the problem is either the short-circuit current through the output MOSFETs, or the ZCD not working correctly. Primary measurements indicate the ZCD circuit is working slower than expected causing an efficiency reduction.

Table 1, displays a list of the simulated, and measured characteristics.

TABLE I. SIMULATED CHARACTERISTICS

Characteristic	Simulated (range)	Measured (only actually measured cases shown)
Simulated Input Voltage	2.5V – 5.0V	1.9V – 5.0V
Simulated Output Voltage	0.3V – 1.5V	0.2V – 1.5V
Output Load	12 µW – 120 µW	55 µW & 160 µW
Commutation Frequency	15kHz – 40kHz	19kHz
Voltage ripple	<5%	<5%
Efficiency	60% – 75%	40%

IV. CONCLUCIONS

A DC/DC converter for micro-power applications was designed, fabricated in a 0.6µm technology, and measured. The circuit fulfilled most the initial requirements. It can operate from an input battery of 1.9V to 5V, and can generate an output voltage from 0.2 to 1.5V. Such a low output voltage may help to power very efficient analog and digital circuits without a significant battery current drain in the case of implantable electronics. The measured efficiency of the converter was only 40%, below the simulated 70% average expected. The preliminary evidence suggests the zero-crossing detector that is part of the feedback loop is not working as expected, being responsible for the energy loss. This work complements reported work in the field of micro-power converters. While the efficiency issue still has to be studied, the output voltage shown to be precise and stable in a wide range of operating conditions, particularly those with a large gap between the input and a low voltage output where some converters fail. Inductive DC/DC converters show promise as a way to efficiently reduce power consumption in implantable medical devices among other ultra low power applications. Inductive converters may reduce the component count of the power management system especially in the case of multiple output voltages, and unlike charge pumps have no major restrictions in the programmed output values. A few recent academic works and commercial products show the feasibility and the interest of the industry in the micro-power range of inductive converters.

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