Characterization of High Voltage MOS Transistors for Analog Design

Rafael Puyol
Electrical Engineering Department
Universidad Catolica del Uruguay
Montevideo, Uruguay
Email: rpuyol@ucu.edu.uy

Matias Miguez
Electrical Engineering Department
Universidad Catolica del Uruguay
Montevideo, Uruguay

Joel Gak
Electrical Engineering Department
Universidad Catolica del Uruguay
Montevideo, Uruguay

***Abstract*—This article presents the study and characterization of several MOS transistors in a HV technology. The analog characteristics of the transistors is analysed to determine the difference of using HV and LV transistors. The device under test (DUT) is the front-end differential pair of an operational transconductance amplifier (OTA). N-channel and P-channel pairs were tested for low voltage and high voltage transistors. The transconductance (g_m), and transconductance over current (g_m/I_D) were studied for strong, moderate and weak inversion regions. The OTA linearity and noise was also measured.**

I. Introduction

When designing for medical devices, special care must be taken for all the interfaces with the patient tissue, including sensing and acting elements. To achieve the desired medical outcome, high voltages are often required (>5V), and standard transistors cannot be used. Several CMOS technologies are offering several different medium and high voltage transistors, that can withstand the required voltages, but whose analog response is sometimes degraded.

In this work, an analog characterisation of both N-channel and P-channel transistors is realised for a 0.6μm XFAB HV technology[1]. A standard low voltage NMOS and PMOS transistors were tested as well as high voltage PMOS and NMOS transistor that withstands up to 20V, suitable for most medical applications. Different channel lengths were used including low voltage and high voltage transistors of similar sizes. Instead of measuring the characteristics of a single transistor, a matched differential pair was implemented for each different transistor to be analysed. This differential pair, implements the front-end stage of a standard symmetrical OTA, shown in figure 1 [2]. In the figure 1, transistors Q1 and Q2 are the DUT and are connected with an array of switches (not shown) to the rest of the OTA. Transistors Q3-Q8 are the same for all measurements, and have their dimensions selected to function correctly for a large range of currents. Table I shows all the different transistors used as DUT.

To characterize the different transistors as analog amplifiers, the gate transconductance (g_m) dependance on the transistor current was measured for all inversion regions [4]. Furthermore, the figure of merit (g_m/I_D), which shows the efficiency at which a transistor amplifies, for a given current consumption was plotted for all transistors. This value is specially important for low power design, used in implantable devices. Finally the linear range for LV and HV transistors, an analysis of the results follows.

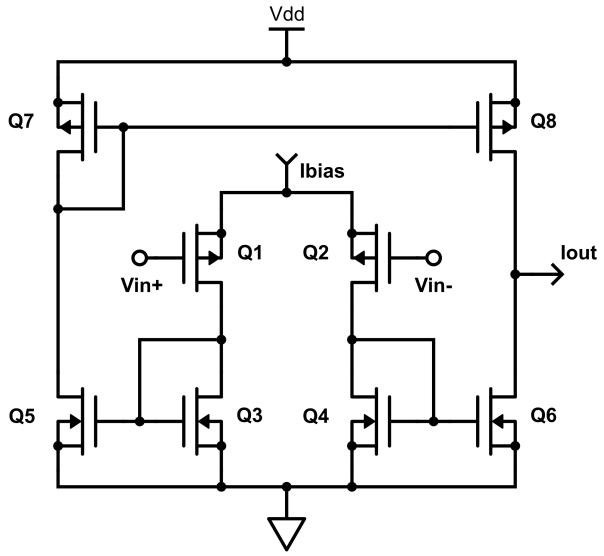

Fig. 1. OTA schematic. Q1 and Q2 are the different DUT, while the rest of the transistors are fixed.

TABLE I
Different DUT tested

name	type	length (μm)	width (μm)
Pmos1	Low voltage PMOS	2	8
Nmos1	Low voltage NMOS	2	8
Phv1	High voltage PMOS	8	32
Phv2	High voltage PMOS	3	4
Pmos2	Low voltage PMOS	1.2	32
Pmos3	Low voltage PMOS	2	4
Nhv1	High voltage NMOS	3	32
Nhv2	High voltage NMOS	3	4
Nmos2	Low voltage NMOS	3	32
Nmos3	Low voltage NMOS	3	4

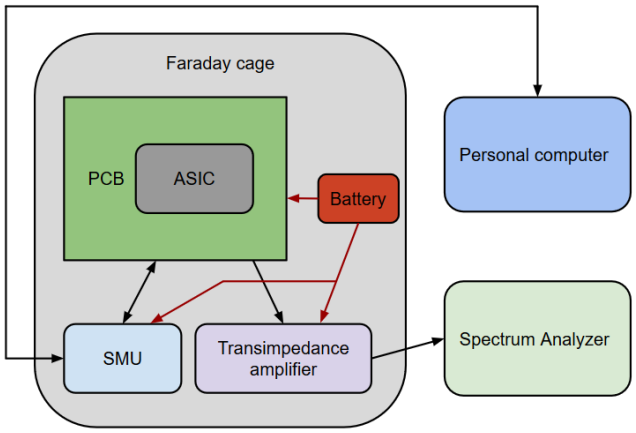

Fig. 2. Setup used for the measurements

II. Measurements

All of the differential pairs were tested using the same setup and configuration shown in figure 2 and explained in [3]. The Spectrum Analyzer was only used for the noise measurements. For the transconductance measurements a sweep of DC voltages was applied to the inputs of the OTA and the output current was measured for each of the input voltages. The DC voltage and the output current were generated and measured using a three channel Agilent U2722A source-measurement unit (SMU). The transconductance of interest for this article is that measured when the differential input voltage is zero, this is the largest transconductance of a differential pair when all other parameters remain unchanged.

The linear range is studied for NMOS low voltage and high voltage transistors, this value is derived from the transconductance measurements.

A. P-channel Transistors

Figure 3 presents the transconductance of each of the P-channel transistors. Figure 4 presents the transconductance over drain current as a function of the drain current for each transistor.

B. N-channel Transistors

Figure 5 presents the transcoductance as a function of the drain current for each of the N-channel transistors. On Figure 6 the transconductance over drain current as a function of the drain current is presented. The sizes of the transistors in the legend are included in table 1. A comparison of the linear range of two transistors, one low voltage and another high voltage is shown in Figure 7, both transistors as indicated by table 1 are the same size.

III. Analysis

A. Comparison of high voltage and low voltage transistors performance

For a given type of transistor the transconductance increases as the ratio width over length increses as predicted by classical

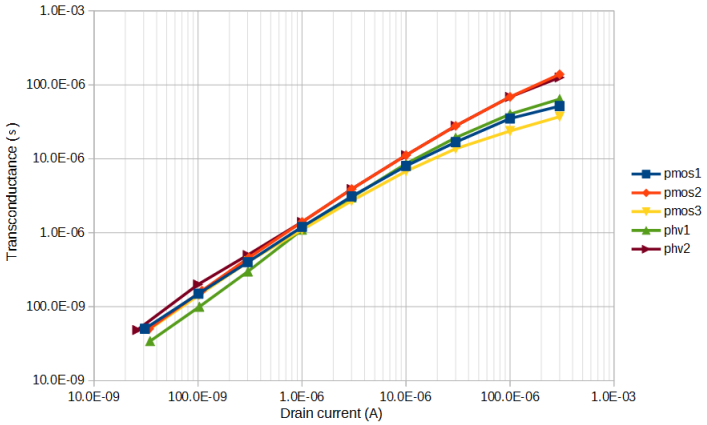

Fig. 3. Transconductance as a function of drain current for each P-channel transistors

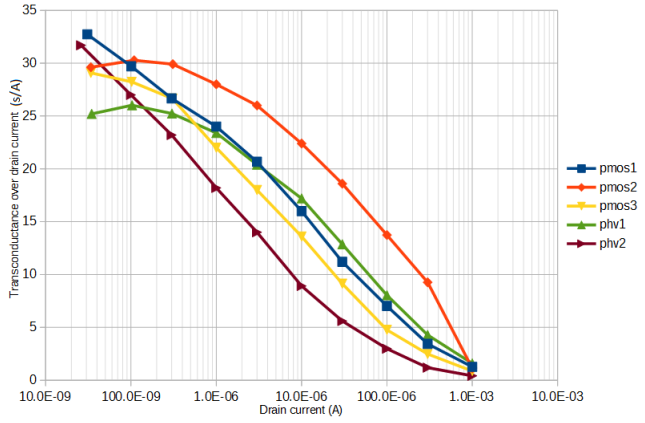

Fig. 4. Transconductance over drain current as a function of drain current for each P-channel transistors

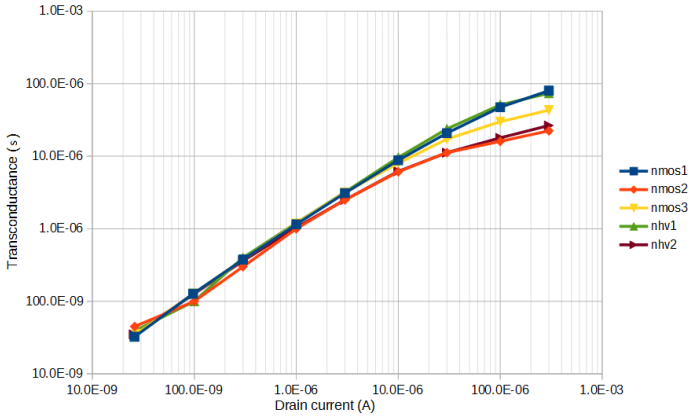

Fig. 5. Transconductance as a function of drain current for each N-channel transistors

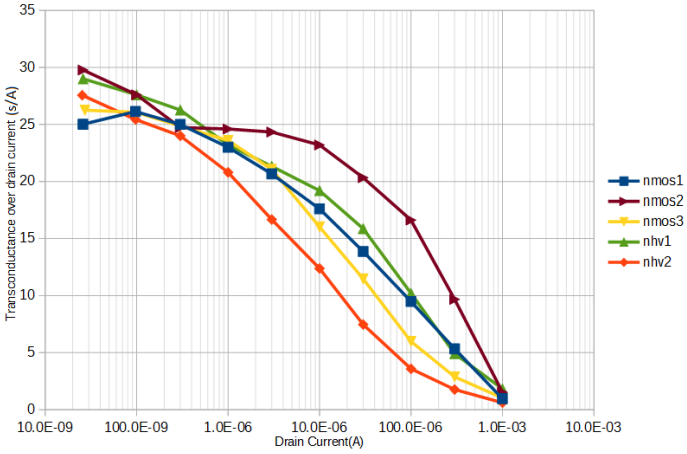

Fig. 6. Transconductance over drain current as a function of drain current for each N-channel transistors

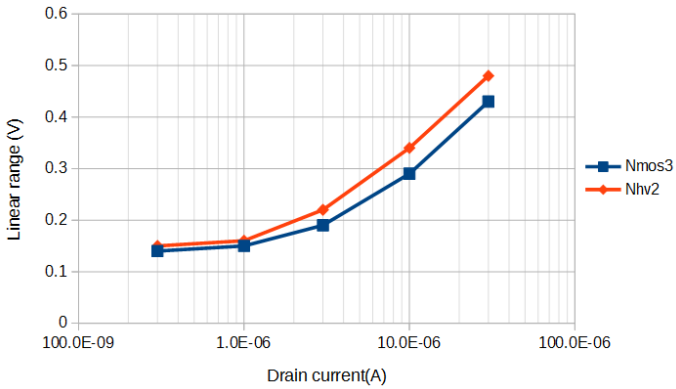

Fig. 7. Linear range as a function of drain current for one low voltage and one high voltage N-channel transistors

models. In figures 4 and 6 the regions of operation are clearly distinguishable, weak at the left, moderate in the middle and strong at the right. High voltage transistors have lower transconductance than low voltage for the same drain current, this was observed in P-channel as well as in N-channel transistors of similar sizes. It follows that high voltage transistors should have larger linear range. This was confirmed with the comparison of the linear range of Nmos3 and Nhv2 as shown in figure 8. These two transistors are exactly the same size. This results confirm the initial guess that HV transistors should not be used in analog block unless it is mandatory. The measured results closely follow the previously simulated values. On the other hand, this transistors may still be used for analog blocks, with this reduced performance taken into consideration.

B. Comparison of P-channel and N-channel transistors

The transconductance of PMOS transistors is lower than that of N-channel transistors. This behaviour was observed for Pmos1 and Nmos1 when operating in moderate and strong inversion but not in weak inversion where the transconductance of the P-channel is larger than that of the N-channel. These transistors are the same size. This phenomenon takes places in high voltage transistors as well, as exemplified by Phv2 and Nhv2. Weak inversion measurements were affected by noise and equipment limitations this could have led to misleading measurements. Also the g_m/I_D of PMOS transistors is greater than NMOS transistors, so for extreme low consumptions, PMOS inputs are preferred in this technology.

IV. Conclusion

The transconductance of several MOS transistors was studied and compared to theoretical predictions. Higher voltage transistors exhibit lower transconductance than comparable low voltage transistors for weak, moderate and strong inversion, confirming the suspicious that high voltage transistors must be used only if necessary. The g_m/I_D achieves greater values for PMOS transistors operating in weak inversion, suggesting the use of PMOS differential pairs for low power amplifiers.

A better setup, specifically a larger precision SMU, is needed for a better analysis of the weak inversion region at even lower drain currents.

Acknowledgment

The authors would like to thank ANII for supporting this project.

References

[1] http://www.xfab.com/home/
[2] R. Puyol, A. Arnaud, M. Miguez and J. Gak, "An ASIC for the Measurement of Low Frequency Noise in the MOS Transistors", in Instrumentation and Measurement Technology Conference, Montevideo Uruguay, 2014, pp. 812-815.
[3] R. Puyol, "A Precision Flicker Noise Measurement Setup", Latin American Symposium on Circuits and Systems, Montevideo Uruguay, 2015.
[4] C. Galup-Montoto, M.C Schneider, A.I.A Cunha, F. Rangel de Sousa, H. Klimach, O.F Seiebel, "The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design", Custom Integrated Circuits Conference, San Jose, California, 2007, pp. 519-526.