A Battery Charge Monitor Topology for Implantable Medical Devices

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***Abstract* — This work proposes a very low power circuit, able to monitor the charge of batteries used in implantable devices through voltage and impedance analysis. The battery monitor is composed of a sample-and-hold circuit and a Gm-C filter, in which the transconductance amplifiers employ series and parallel association of transistors. Besides, the system contains level-shift circuits that limit the signal within the range of the following A/D converter (0 V to 1.25 V). The system functionality was verified through both simulation and prototypes implemented on a 0.35 µm technologies.**

I. INTRODUCTION

Many biomedical applications such as pacemakers and implantable prostheses depend on the operation of a battery. Thus, implantable devices need some measuring circuit to determine the battery charge consumed and/or estimate the remaining charge. This information is critical to health professionals, who must recommend the replacement of the device, or postpone a delicate surgical procedure [1]. Thus, the circuit that monitors the battery charge is fundamental, requiring reliability, security, and very low power consumption.

Some kinds of battery monitors circuits are available in the literature [1] -[6]. In general, the majority of these circuits use the traditional topology of charge integration, shown in Fig. 1, which has continuous and undesirable energy consumption over the lifetime of the battery. This topology integrates the current of battery using a passive device as a resistor. In this example, the value of the charge consumed is stored in digital memory.

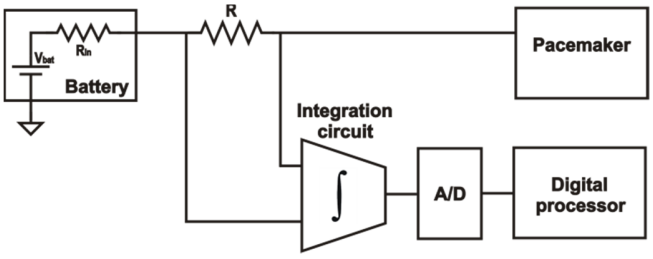

Fig. 1. Traditional topology of charge integration.

Other topologies estimate the residual charge using a current integration method and the impedance or voltage measurement throughout battery lifetime, since the batteries for implantable devices present physical characteristics such as voltage and impedance that present well defined dependencies in terms of the consumed charge [5], [6].

This work proposes an integrated and safe topology that monitors the battery charge of implantable devices from measurements of internal resistance and voltage taken in a specific period time over the battery lifetime. Unlike traditional systems of current integration, which have continuous energy consumption over the lifetime of the battery, the proposed system remains "on" only when the measurement is taken. Therefore, the average power consumption is extremely low.

In our topology, the battery impedance is measured from the variation of the battery voltage level in terms of a controlled variation of battery current in a short time slot. In order to achieve a good trade-off between area and power consumption a design-oriented current-based MOSFET model [7], [8] has been used.

II. THE PROPOSED TOPOLOGY

The proposed system is based on the monitoring of the impedance and voltage characteristics of battery at defined time intervals throughout battery lifetime. In order to reduce the power consumption, it is suggested that the measurements are taken once a day. The extracted values of impedance and voltage are processed by an A/D converter and converted into a digital signal, which is stored in a memory.

The developed topology is shown in Fig. 2. When switch S1 is closed and both S2 and S3 are open, the battery voltage value is stored in Csh1. When S1 is open and both S2 and S3 are closed, the additional consumption due to the current source of 5 µA (Iforce) forces a drop in the battery voltage, whose value is stored in Csh2. The difference between the voltages on the capacitors is processed through a differential amplifier. Thus, the internal impedance is inferred by measuring the voltage variation due to the current variation imposed to battery.

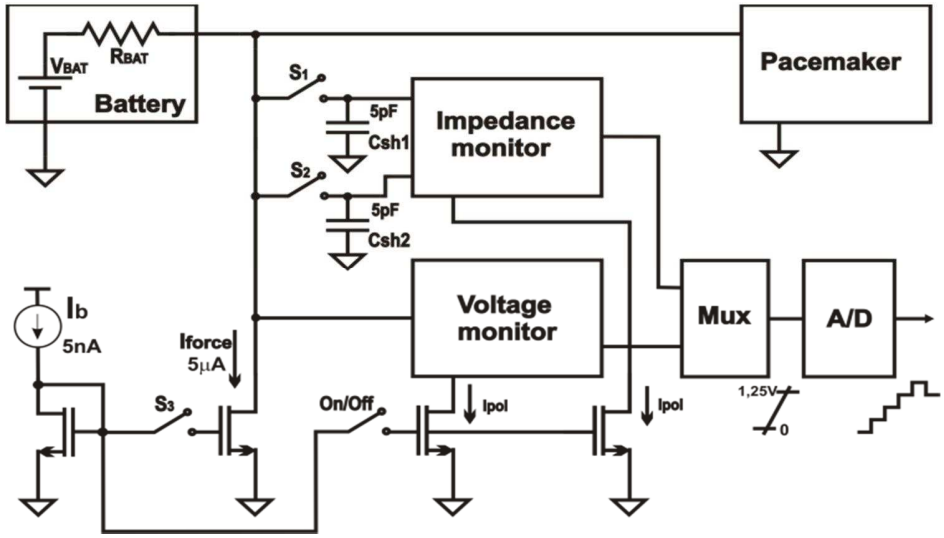

Fig. 2. The battery charge monitor topology.

TABLE I. TRANSISTOR MODEL

Variable	Expression
Drain current	$I_D = I_F - I_R = I_S(i_f - i_r)$
Specific Current	$I_S = \mu n C'_{OX} \frac{\phi_t^2}{2} \frac{W}{L}$
Source/drain to bulk voltage	$V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right]$
Pinch-of voltage	$V_P \cong \frac{V_G - V_{T0}}{n}$
Drain-to-source saturation voltage	$V_{DS,SAT} \cong \phi_t\left(\sqrt{1+i_f} + 3\right)$
Source transconductance	$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right)$
Power spectral density of thermal noise (saturated transistor)	$Sin_t = \frac{8}{3} k_B T g_m \frac{\sqrt{1+i_f} + 1/2}{\sqrt{1+i_f} - 1}$

Thus, the internal battery impedance R_{BAT} is

$$R_{BAT} = \frac{V_{Csh1} - V_{Csh2}}{Iforce} \quad (1)$$

When the measurements are taken the switch on/off is closed; otherwise, the switch is off and the power consumption of the monitor is negligible. Note that the current source Ib is always on, since it is employed for biasing the other parts of the implantable device. The battery voltage measurement is taken by a level-shift (source follower) circuit.

III. DEVELOPED CIRCUITS

A. The transistor model

The main expressions of the transistor model used in this work are summarized in the table I, where $i_{f(r)}$ is the normalized forward(reverse) saturation current, or the inversion level at the source(drain), μ is the mobility, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage, W is the channel width, L is the channel length, V_{T0} is the equilibrium threshold voltage, V_S is the source-to-bulk voltage, V_D is the drain-to-bulk voltage, V_G is the gate-to-bulk voltage, k_B is the Boltzmann constant, T is the absolute temperature, and N^* and N_{ot} are technological parameters related to number of interface traps.

B. The impedance monitor

The impedance monitor consists of a sample-and-hold circuit (S_1, S_2, C_{sh1} and C_{sh2} in the Fig. 2) which stores the battery voltage drop due to the forced current (Iforce). This circuit is composed of two poly capacitors and two minimal area PMOS switches. The small differential-voltage stored in the sample-and-hold circuit, is properly amplified through a differential amplifier, which also performs a low-pass filtering function to attenuate the spurious signals generated by the switching circuit. For the filtering and differential amplifier functions we have used the active low-pass OTA-C filter [8], [9] shown in Fig. 3, that presents a good trade-off between accuracy and silicon real estate. Its transfer function is

$$H(s) = \frac{V_{out}}{V_{bat+} - V_{bat-}} = \frac{Gm1}{Gm2} \frac{1}{1 + sC_f / Gm2} \quad (2)$$

where Gm1 and Gm2 are the tranconductance of each amplifier and C_f is the filter capacitor.

For low–frequency applications, large time constants and, thus, small values of transconductance are required. At the same time, the OTA (operational transconductance amplifier or simply Gm) at the output is required to operate at a relatively high differential voltage. To comply with the (sometimes conflicting) requirements of large time constant and high linearity as required by the filter, we used the current division technique of the OTA (differential pair) output

current through the series-parallel association of transistors [9], [10], as shown in Fig. 4. With this topology, it is possible to operate at higher linearity and small transconductance value, as required by the filter.

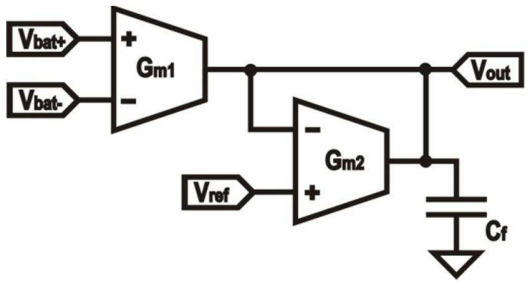

Fig. 3. Differential OTA-C filter used to amplify the signal from the impedance monitoring.

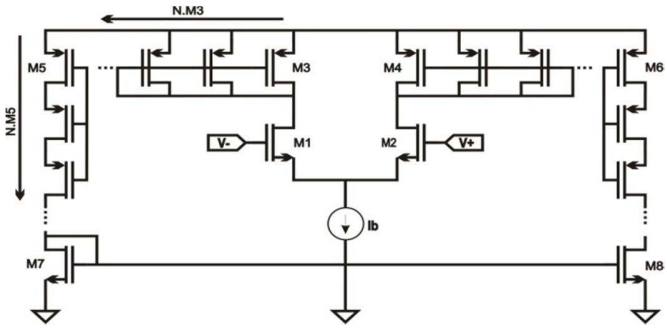

Fig. 4. OTA circuit that employs series and parallel associations of transistors for current division.

Analyses of noise and offset have been developed for the differential amplifier. Using the equations shown in the table I and references [8] and [9], the thermal (3) and the flicker (4) noise of the each OTA circuit is given by

$$\overline{Vn^2_{thermal}} = \frac{4nk_BT(f_2 - f_1)}{Gm}\left(\sqrt{1+i_{f1}}+1\right) \tag{3}$$

$$\overline{Vn^2_{flicker}} = \frac{2nk_BT\ln(f_2/f_1)}{N^{*}C'_{ox}}\left[\frac{N_{ot\_n}}{(WL)_1}+\left(\sqrt{1+i_{f1}}+1\right)^2\left(\frac{2N_{ot\_p}}{N(WL)_2}+\frac{N_{ot\_n}}{(WL)_3}\right)\right] \tag{4}$$

where f_1 is related to the time interval in which the filter is on and f_2 is the bandwidth of the filter.

Using (3) and (4), we can calculate the total noise of the differential amplifier considering the flicker and thermal noise terms as

$$\overline{Vn^2_{Amp}} = \overline{Vn^2_{Ota1}} + \overline{Vn^2_{Ota2}}\left(\frac{Gm2}{Gm1}\right)^2 \tag{5}$$

For the sake of simplicity, only variation in the threshold voltage, V_T, and in the current factor β will be considered for mismatch analysis [11]. Thus

$$\sigma^2_{VT} = \frac{A^2_{VT}}{2WL},\ \frac{\sigma^2_\beta}{\beta^2} = \frac{A^2_\beta}{2WL} \tag{6}$$

where A_{VT} and A_β are technology parameters. The total mismatch in each OTA is about

$$\sigma^2_{Vin} = 2\left[\left(\sigma^2_{VT}\right)+\frac{1}{\left(g_m/I_D\right)^2_{M1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)\right]+4\frac{I^2_{D1}}{N.gm^2_1}\left[\left(g_m/I_D\right)^2_{M5}\left(\sigma^2_{VT}\right)+\left(\frac{\sigma^2_\beta}{\beta^2}\right)\right]+\ldots$$
$$+2\frac{I^2_{D1}}{gm^2_1}\left[\left(g_m/I_D\right)^2_{M7}\left(\sigma^2_{VT}\right)+\left(\frac{\sigma^2_\beta}{\beta^2}\right)\right] \tag{7}$$

where the first term in square brackets refers to the source-coupled pair (M1 and M2), the second term in square brackets refers to the series-parallel current mirror (M3, M4, M5 and M6), while third term in square brackets refers to the current mirror (M7 and M8) in Fig. 4.

To reduce silicon area, the filter capacitor, C_f in the Fig. 3, was implemented as a gate capacitor biased in strong inversion, which leads to an area around five times smaller than that of a polysilicon capacitor on the same 0.35 μm process. Considering operation in strong inversion and the expressions of table I, the relationship between the inversion level and the gate capacitance C_G can be written as

$$C_G \cong C'_{ox}WL\left[1-\frac{2}{n\sqrt{i_f}+2}\right] \tag{8}$$

The differential amplifier presents a non zero common mode output signal. In order to move this signal to the appropriate range of the A/D converter, the source follower shown in Fig. 5 is used.

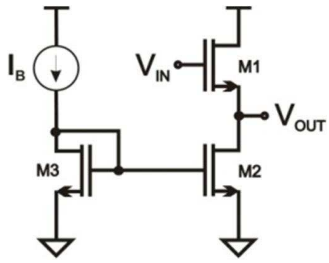

Fig. 5. Source follower circuit.

Using the expressions of table I, V_{OUT} in Fig. 5 is given by

$$V_{OUT} \cong \frac{V_{IN}-V_{T0}}{n}+K\phi_t \tag{9}$$

where

$$K = -\left[\sqrt{1+\frac{I_B}{I_{S1}}-2+\ln\left(\sqrt{1+\frac{I_B}{I_{S1}}}-1\right)}\right] \tag{10}$$

C. The voltage monitor

In order to monitor the voltage variation of the battery over its useful lifetime a level-shift circuit, which properly moves the signal for the range of the A/D converter, is used. The voltage monitor shown in the Fig. 6 presents the voltage output $V_{OUT}=V_{BAT}-2V_{GS}$. The value of the bias current and the aspect ratio of the diode connected transistors were designed for a proper value of V_{GS}.

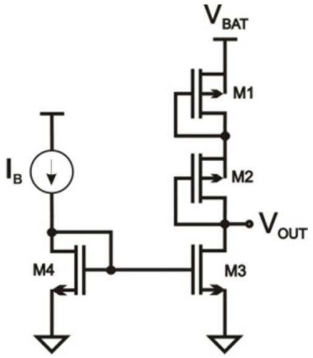

Fig. 6. Level-shift circuit, used to monitor the battery voltage. V_{BAT} is the battery voltage.

IV. Experimental Results

The design of the battery monitor whose layout is shown in Fig. 7, was implemented on the AMS 0.35 µm technology. For this design we considered the Li/I_2 battery [2], used as a standard for pacemakers. The voltage over lifetime of a Li/I_2 battery ranges from 2.8V to 2.0V and the impedance ranges from 100Ω to 10 kΩ. For the purpose of safety, we considered the minimum battery voltage equal to 2.4V and a maximum impedance of 5 kΩ. The analog blocks have been designed to provide inputs to the A/D converter ranging from 0 to 1.25V.

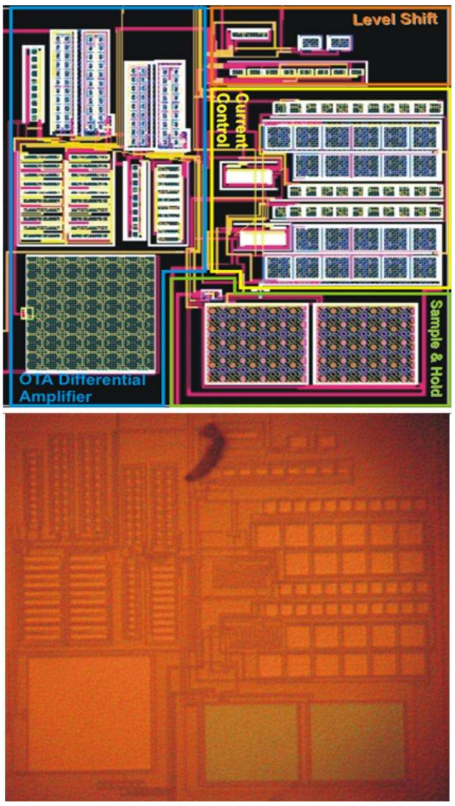

Fig. 7. Layout and micrograph of the battery monitor in the AMS 0.35 µm technology.

The experimental results of the monitor prototype are shown in Fig. 8 and Fig. 9. The characteristics of the battery were emulated by a power supply connected to a resistor. Fig. 8 shows the test of the impedance monitor circuit for a series resistance ranging from 100 Ω to 10 kΩ. In the Fig. 9 are shown both, the experimental and simulated (using BSIM 3v3.1 model) behavior of the voltage monitor considering the battery variation from 2.8 V to 2.0 V.

The table II summarizes the main characteristics of the implemented circuit.

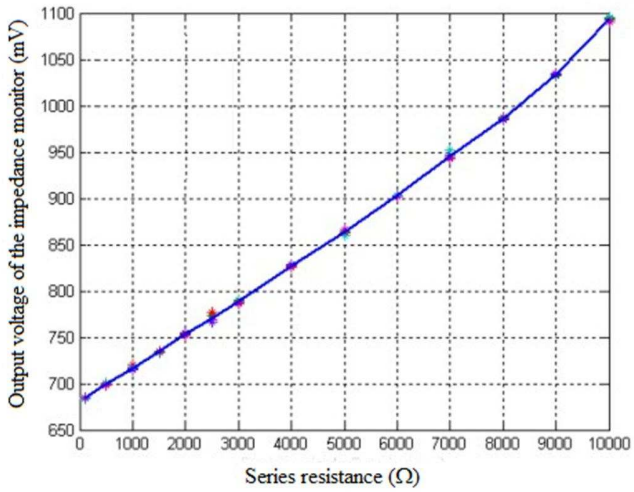

Fig. 8. Experimental measurement of the impedance monitor, considering a power supply in series with a resistor (100 Ω to 10 kΩ).

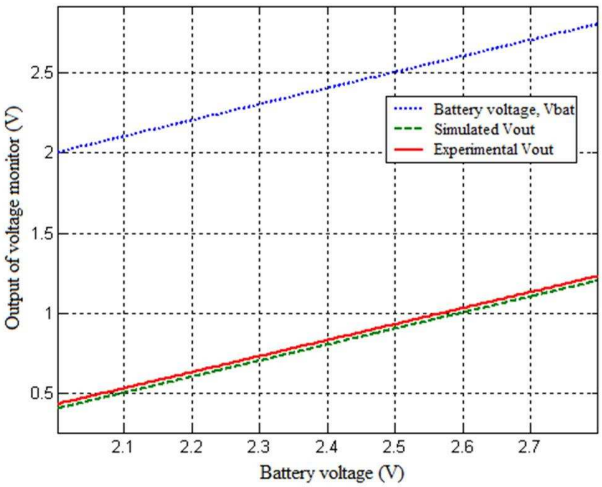

Fig. 9. Experimental and simulated measurement of the voltage monitor circuit in function voltage battery variation.

The results extracted from the test chip confirm the functionality of the circuit. The linearity of the circuit, especially in the range of the component under measurement (up to 5 kΩ, considering Li/I2 battery used in pacemakers) is quite acceptable. The stage of the digital control circuit was implemented using a FPGA circuit.

TABLE II. MAIN CHARACTERISTICS OF THE MONITOR CIRCUIT

Variable	Value
Gain of the differential amplifier	8
Gm1	56 nA/V
Gm2	7 nA/V
Voltage shift of the voltage monitor	1.6 V
Total area	~ 0.15 mm^2
Current consuption/day	~ 6.5 nAh

V. CONCLUSION

We have presented a battery monitor circuit. Its main advantages are the extremely low power consumption and the simplicity of the method. The monitor functionality has been experimentally verified for a prototype implemented in a 0.35 μm CMOS technology.

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REFERENCES

[1] A. E. Zadeh, "A micro-power precision switched-capacitor charge meter system for implantable medial devices,". IEEE Midwest Symposium on Circuits and Systems, Lansing, US, pp. 1068-1072, Aug. 2000.

[2] J. G. Webster, "Design of Cardiac Pacemakers," New York: IEEE Press, 1995.

[3] F. Silveira, D. Flandre, "Low Power Analog CMOS for Cardiac Pacemakers," Boston: Kluwer Ac. Pub, 2004.

[4] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas and h. Nääs, "A Very Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2446-2456, December 2004.

[5] M. Obel, N. Sköldengen, J. Lindber, "Method and Circuit for Determining the Battery Status in a Medical Implant," U.S. Patent 6,748,273, June 2004.

[6] C. R. Rogers, D. R. Merritt, C. L. Schmidt, J. Mukul, "System and Method for Monitoring Power Source Longevity of an Implantable Medical Device," U. S. Patent 6,901,293, May 2005.

[7] A. I. A Cunha, M. C. Schneider, C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design," IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1510-1519, October 1998.

[8] M. C. Schneider, C. Galup-Montoro, "CMOS Analog Design Using All-Region MOSFET Modeling," Cambridge University Press, 2010.

[9] A. Arnaud, R. Fiorelli and C. Galup-Montoro, "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors," IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 2009-2018, September 2006.

[10] C. Galup-Montoro, M. C. Schneider, I. J. B. Loss, "Series-Parallel Association of FET's for High Gain and High Frequency Applications," IEEE J. Solid-State Circuits, vol. 29, no. 9, pp. 1094-1101, September 1994.

[11] M. J. M Pelgrom, A. C. J. Dunmaijer, A. P. G. Welbers, "Matching Properties of MOS Transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433-1440, October 1989.