Integrated Switch for Implantable Medical Devices

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***Abstract*—In this paper, an integrated switch to control electrical stimuli in implantable medical devices is presented. Different tissue stimulations can be done in voltage ranging from a few mV to over 16 V or in current ranging from a few µA to tens of mA. To implement a widely general switch for all these cases, that fulfill also regular safety requirements, a high voltage technology in a SOI waffer has been selected.**

Keywords- HV-CMOS, switch, implantable medical devices.

I. INTRODUCTION

Most implantable medical devices are electrical stimulation systems, that deliver either current or voltage pulses to the patient according to different requirements. Microelectronics technology steadily contributes to the development of such devices. Stimuli section of the circuit may consist of the basic elements shown in Fig. 1: a stimuli generator (either a voltage or current source), electrodes which connects the tissue to the device, a switch that toggles the electrical connection of the electrodes, and a control block that decides when and for how long a stimulus should be applied. Stimulation can be done either by applying a voltage in the tissue from a few mV to well over 10 V or driving a current through it, ranging form a few µA to tens of mA. Although it appears simple, in this work we will focus in a circuit to implement the switch block of Fig.1. A high voltage (HV) technology was selected to enable stimulation up to 16 Volts, a 0.6 microns technology having a p-type SOI wafer with insulator trenches capability. Different medium and high voltage transistors can be fabricated with maximum ratings between 8V, 40V and up to 60V. Because of trench isolation, floating diodes can also be fabricated.

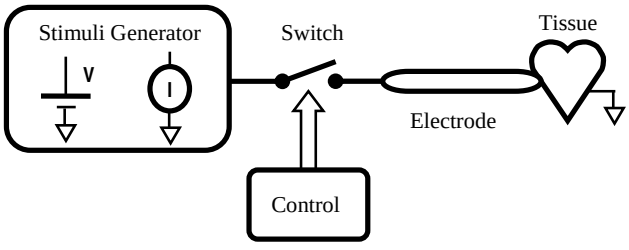


Figure 1. A scheme of stimulus section of an implantable medical device.

II. HV-TECHNOLOGY

Introducing new layers, a HV CMOS technology allows the fabrication of devices that can support elevated voltages, in this case, up to 60V. The selected technology uses dielectric isolation on SOI wafers, which allows unrestricted 60V high and low side operation of all devices, but also allows the use of diodes in direct, and prevents latch up. Regular 5V CMOS core is also present, as well as double poly capacitors and high-resistivity poly layer for resistors. As an example, in Fig. 2 a nhv NMOS transistor cut is shown. Nhv has the regular structure of a HV transistor, incorporating a thick gate oxide that enables up to 18V V_{GD}, V_{GB} voltage values, and the drain diffusion is growth into a NWELL to complete a diffused Drain to support elevated V_{DS} voltages. In table 1 some characteristics of the process devices' are shown, obtained from the manufacturer's public webpage.

TABLE I. SOME DEVICES AVAILABLE AND THEIR CHARACTERISTICS

MOS TRANSISTORS	**V_T(V)**	**I_{DS}@V_{GS} (µA/µm)**	**BV_{DSS} (V)**	**Max V_{DS} (V)**
NMOS 5V	0,87	470@5	13	5,5
PMOS 5V	0,9	230@5	12	5,5
NMOS with ESD implant	0,9	520@5	12	5,5
NMOS HV	0,82	220@12	60	30
PMOS HV	0,75	190@12	70	40
RESISTORS	**RS (Ω/□)**	**V_A (V) (lin/quad Temp. coeff.)**		**Max V_{CE} (V)**
Low TC poly0	580	-0.20 – 0.80		60
Hihg resistive poly0	3500	-3.3 – 10.9		60
FORWARD DIODES	**Vf (V)**	**Max If (mA/µm)**		**Max Vr (V)**
Rectifier diode	0,82	0,25		10
Rectifier HV diode	0,83	0,25		50
CAPACITORS	**BV (V)**	**Area Cap (fF/µm^2)**		**Max V_{CC} (V)**
poly0/poly1 cap	30	1,87		8
linear poly0/poly1 cap	20	1,02		8

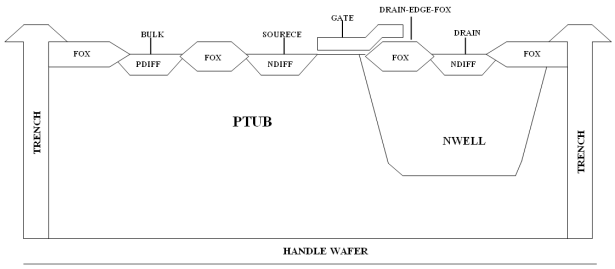


Figure 2. Vertical cut of a typical HV NMOS (NHV).

III. SPECIFICATIONS

The circuit is simply a switch that can connect/disconnect the electrodes from the electric pulse generator. In Fig. 3 a typical scheme is shown. A microcontroller commands this special switch through Ctrl signal.

Initial specifications are the following:

- The switch must operate correctly with commutation voltages V_{IN} from 100 mV to 16V.
- It must work with supply voltages V_{CC} from 2V (end of life of a lithium-iodine pacemaker like battery) up to 4.2V (a fully charged rechargeable medical grade battery) [1],[2].
- The switch must have an ohmic resistance of 5 Ω or less, in all ranges of operation. A voltage above V_{CC} was necessary to fulfill this requirement, thus a voltage doubler $2V_{CC}$ was included (uses an external capacitor)
- There must not be any static current consumption when not stimulating.
- The switch must be capable of turning on and off in less than 1µs.
- Current spikes during on/off time must be minimum, as well as current spikes through the switch when it is open and the tissue voltage varies.
- The switch must be completely symmetric ($V_{IN} - V_{OUT}$ can be exchanged).
- Safety: the failure of a single circuit element (for example a perforated MOS gate) must not produce DC current flow through the electrode larger than a few micro-amps because otherwise it may be a risk for the patient

IV. BASIC BUILDING BLOCKS

In this section the basic building blocks of the designed integrated switch will be examined. As different kind of transistors are used (HV and 5V), in Fig. 4 the symbols used for each case are shown. Since HV transistors are not symmetrical, the drain (which can withstand a higher voltage) is marked with a double line.

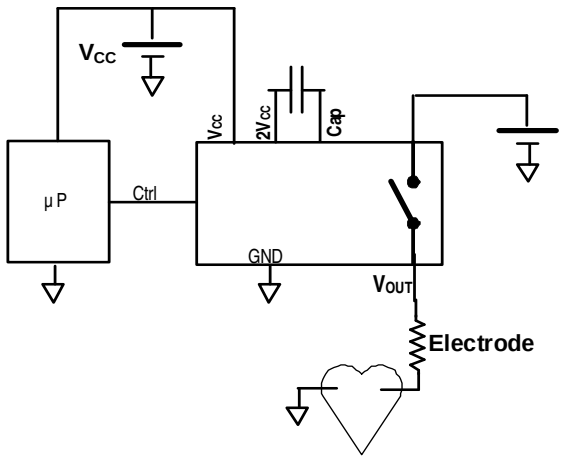


Figure 3. Typical application of designed switch.

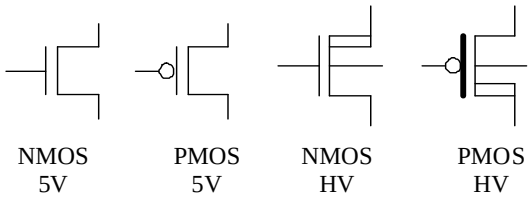


Figure 4. Symbols of different kinds of transistors.

In Fig. 5 the principal transmission gate is shown, including its driving circuitry. This transmission gate is the switch that allows the stimuli to pass or not to the tissue. It was designed to have an impedance below 5Ω, using high voltage transistors. M1, M2 and M3, M4 are connected in series but flipped, to prevent conduction through Bulk-Drain diode if $V_{OUT} > V_{IN}$.

In Fig. 6 the NMOS level-shifter (LS_N) is shown [3]. The "In" signal controls the output "Out". The LS_N has two states:

- High state: When the "in" signal is equal to V_{CC}, the transistors M1, M5 and M6 are switched on and the output "out" goes to a $2V_{CC}$ voltage which will be generated by a voltage multiplier.
- Low state: When the "In" signal is 0V, the transistors M2, M3 and M4 are switched on and the output "out" goes to 0V.

In Fig. 7 the PMOS level-shifter (LS_P) is shown. The LS_P is a variation of the LS_N, the output "out" goes to V_{ref} through a transmission gate M6 and M7. The transmission gate is necessary because V_{ref} can be very small (100mV) and M6 will not work properly; for small V_{ref}'s the conduction will be mainly done through M7. Transistors M8 and M9 were added for the same reason, to guarantee the stability of the level shifter at low V_{ref} values. Because V_{ref} voltage may be connected to the electrode, as the gates of transistors M7, M8 and M9 go to V_{CC} when there is no stimulation if there is a puncture in the oxide of one of these transistors, a direct path from V_{CC} to tissue may be created. To prevent this direct path,

the gates are commanded through a RC circuit, where R has an impedance of more than 1MΩ, to limit the current flowing into the patient in failure condition.

The LS_P has two states:

- State "1" or V_{ref} : When the "in " is V_{CC} the output "out" goes to V_{ref}.
- State "0": When the "in" signal is 0V the output goes to 0V.

Because at very low V_{CC} supply, the on-resistance of the principal switch in Fig. 5 is too high, NMOS transistors will be turned on with a $2V_{CC}$ voltage that must be generated 'on-chip'.

In Fig. 8 the $2V_{CC}$ generator is shown. This circuit generates a voltage equal to two times V_{CC} during stimulation. To achieve the duplication of voltage, an external pumping capacitor was necessary. The $2V_{CC}$ generator has two states:

- V_{CC} state: When the "In" signal is V_{CC} the capacitor C1 is charged to V_{CC} through M1 and M2. The transistor M3 is in a diode configuration, it is used in the start-up of the circuit.
- $2V_{CC}$ state: When the "In" signal is 0V the output "Cap" of the inverter goes to V_{CC}. As the capacitor is already charged, and cannot discharge as the level-shifter LS_2VCC cuts off the transistors M1 and M2, the output "$2V_{CC}$" is elevated to $2V_{CC}$ volts.

Note: C1 is an external capacitor, and its value can vary from 1µF to tens of nF, depending on admissible leakage and the stimuli duration.

Finally in Fig. 9, the level-shifter $2V_{CC}$ (LS_2VCC) is shown. LS_2VCC is a small variation of the LS_N. The LS_2VCC has two states:

- $2V_{CC}$ state: When the signal "in" is V_{CC} the output "out" goes to $2V_{CC}$.
- 0 state: When the signal "in" is 0V the output "out" goes to 0V.

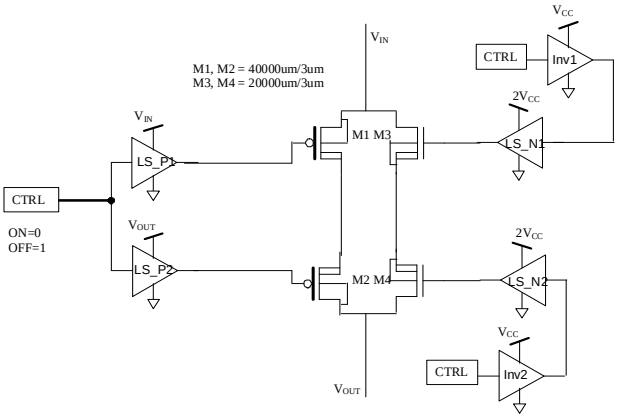


Figure 5. Complete integrated switch.

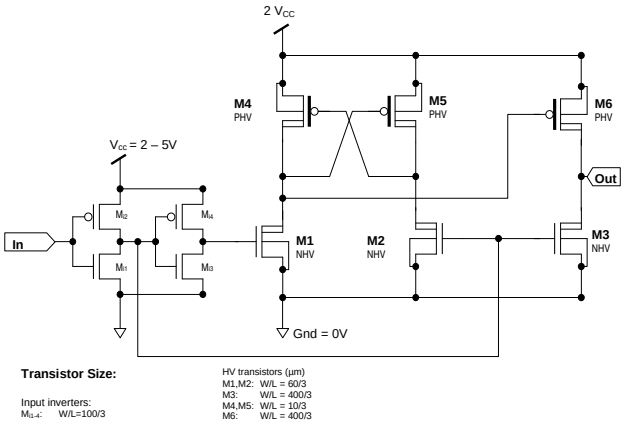


Figure 6. Level-shifter NMOS, schematic.

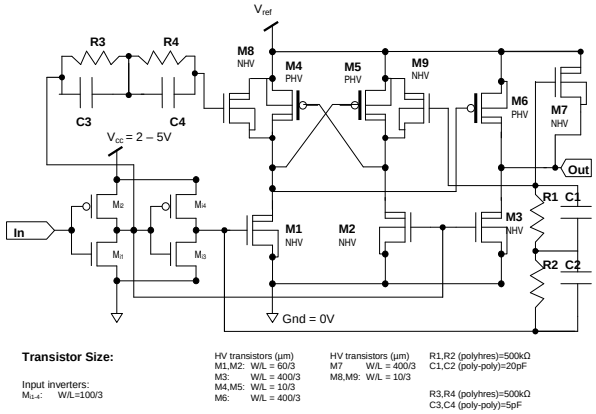


Figure 7. Level-shifter PMOS.

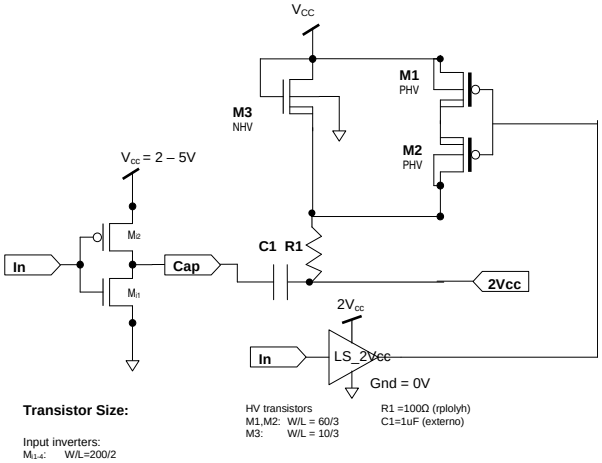


Figure 8. $2V_{CC}$ generator

V. THE COMPLETE SWITCH

In Fig. 5 the complete switch is presented. Stimuli current conduction is done through transistors M1, M2, M3 and M4 they are placed in a transmission gate configuration to ensure a maximum impedance of 5Ω in all circumstances of operation and corner transistors (V_{CC} from 2V to 5V and V_{IN} from

100mV to 16V). To turn the switch off M1 and M2 gates are connected to V_{IN} and V_{OUT} respectively and M3 and M4 to ground. To turn on the switch M1 and M2 gates are connected to ground and M3 and M4 gates to $2V_{CC}$. The $2V_{CC}$ voltage is generated during stimulation only.

To sum up the complete switch has two states:

- Closed state: When the signal "CTRL" is 0V the outputs of LS_P1(2) and LS_N1(2) are 0V and $2V_{CC}$ respectively, making conduction possible through M1, M2 and M3, M4. If the voltage difference V_{IN} - V_{OUT} is high, the M1, M2 branch will conduct most of the current, if not, the M3, M4 branch will transport most of the current. (Transmission Gate configuration).
- Open State: When the signal "CTRL" is V_{CC} the outputs of LS_P1(2) and LS_N1(2) are $V_{IN}(V_{OUT})$ and 0V respectively, cutting off conduction through M1, M2 and M3, M4.

In Fig. 10, a complete layout of the switch is shown.

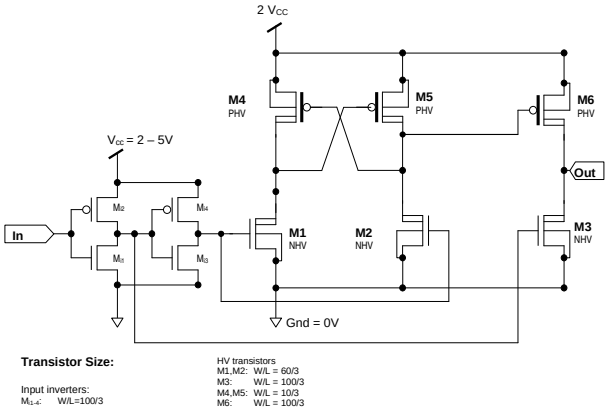


Figure 9. Level-shifter $2V_{CC}$

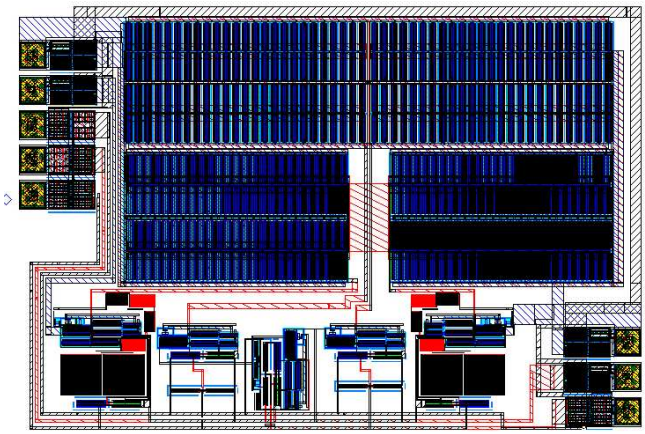


Figure 10. Switch Layout

VI. SIMULATIONS

The circuit is currently being fabricated. Some simulations of the designed switch will be presented in this section. In Fig. 11 the impedance of the transmission gate is shown (M1, M2, M3 and M4 of Fig. 5) using different models for the transistors: typical (TM), worst slow (WS) and worst power (WP). This simulation was conducted with V_{CC} = 2V (which is the worst possible case).

Fig. 11 shows that in all three cases the impedance of the switch is always below 5 Ω (careful design of the metal cables connecting the transistors to the pads was necessary to fulfill this condition). In Fig. 12, a second simulation is presented: V_{OUT} of Fig. 5 is shown for different V_{IN} with a load impedance of 1kΩ, showing that the switch works in all the necessary voltage ranges, for all transistors models.

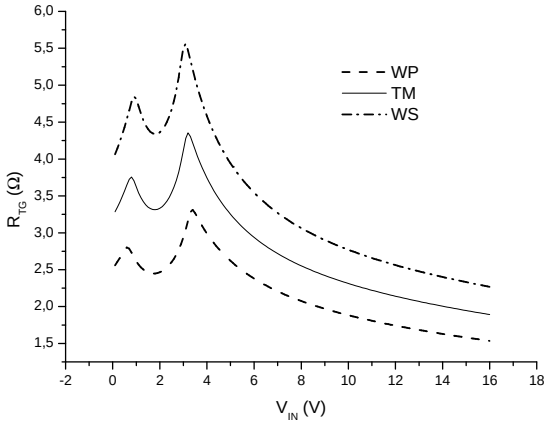


Figure 11. Transmission Gate impedance VDD 2V

Finally in Fig. 13, the current through the transmission gate is plotted, when V_{IN} is connected to ground and a square wave of 8V of amplitude was applied to V_{OUT} (see Fig. 13.b). This parasitic current is caused by the charges accumulating in the gate capacitance of M2, charging it to 8V, but no other currents enter the designed switch. In table 2, the simulated characteristics of the complete switch are summarized.

TABLE II. SWITCH SIMULATED CHARACTERISTICS

Characteristic	Value
Switch Impedance (Typical)	3 Ω
Power supply (V_{CC})	2 - 5 V
Commutation voltage (V_{IN})	0.1 -16 V
Commutation time	0,5 µS

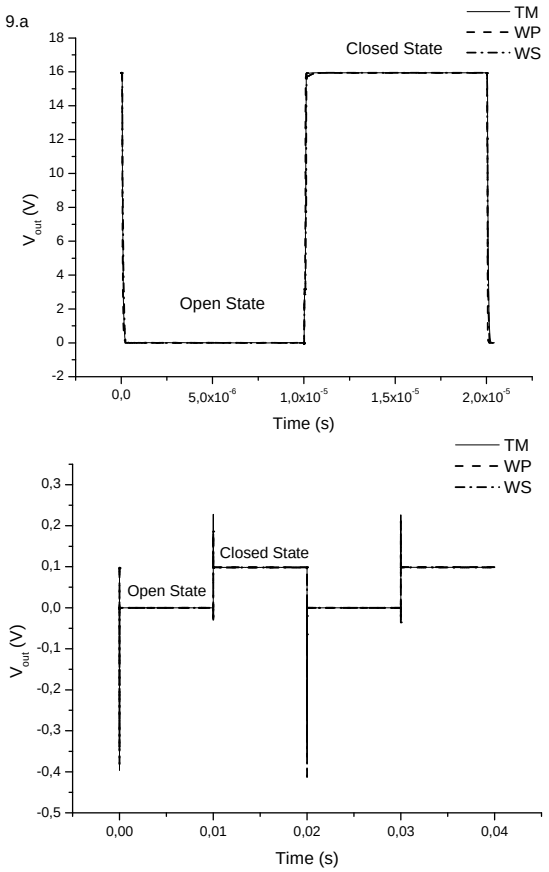
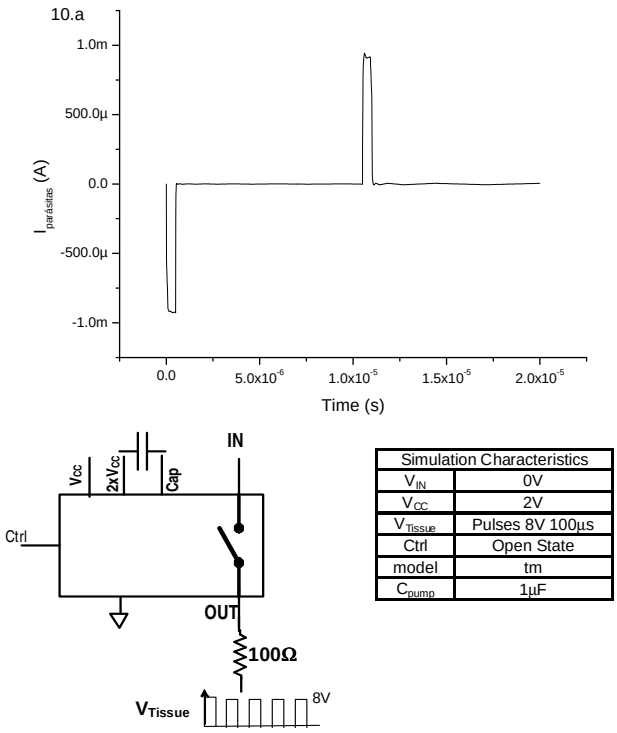


Figure 12. a) V_{OUT}, V_{IN} and V_{HIGH} 16V b) V_{OUT}, V_{IN} and V_{HIGH} 100mV



Simulation Characteristics	
V_{IN}	0V
V_{CC}	2V
V_{Tissue}	Pulses 8V 100µs
Ctrl	Open State
model	tm
C_{pump}	1µF

Figure 13. a) V_{OUT} with V_{IN} 16V b) V_{OUT} with V_{IN} 100mV

VII. CONCLUSIONS

A complete design for an integrated switch, to precisely control electrical stimulation in implantable medical devices (currently under fabrication) was presented. A HV CMOS technology was employed, and it is the first experience in our group with a 'trench-isolated' technology. The simulations of the designed switch fulfill all specifications and safety requirements, a complete testing will be realized when the fabrication is complete.

ACKNOWLEDGMENT

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