An ASIC for the Measurement of Low Frequency Noise in MOS Transistors

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***Abstract*— Cyclostationary (switched) operation of the MOS transistor has been proposed in recent years as a technique for reducing the flicker noise at the device level itself. Nevertheless accurate noise measurements covering a wide range of operation regions for the transistor are still required to support the proposed cyclostationary noise models. In this work, several noise measurement issues are discussed, and the development of an integrated circuit aimed at switched flicker noise measurements in different types/sizes of test transistors and at different bias conditions is presented. The proposed ASIC is a matrix of differential pairs (DUTs) connected to a GmC chopper-amplifier. The chopper modulators are disposed to amplify flicker noise from the DUTs while the remaining flicker noise sources in the circuit are cancelled.**

Keywords—noise measurement; flicker noise; MOSFET

I. INTRODUCTION

Flicker noise or simply 1/f noise is such that its power spectral density (PSD) varies with frequency (*f*) in the form:

$$S_{i_n}(f) = K / f^{\gamma} \tag{1}$$

where S_{in} is the PSD of a noise current i_n, K and γ are constants and $\gamma \approx 1$. In Fig.1(a) a typical MOSFET noise current PSD is shown, where i_n is a small signal random current which models noise, that is summed to the DC current I_D of the transistor. It is quite well accepted that the sources of MOS flicker noise are mainly carrier number fluctuations due to random trapping–detrapping of electrons in energy states, named 'traps', in the oxide near the surface of the semiconductor [1],[2]. From some time ago, switched biasing (cyclostationary operation) has been proposed as a technique for reducing the flicker noise at physical level in MOSFETs [3],[4]. Cyclostationary operation is not a circuit technique like chopper or autozero [5], instead just the transistor is periodically cycled between an 'off'-state and saturation ('on'-state). An intuitive explanation of the noise reduction phenomenon is that periodically turning 'off' the transistor's channel, periodically forces a significant fraction of occupied

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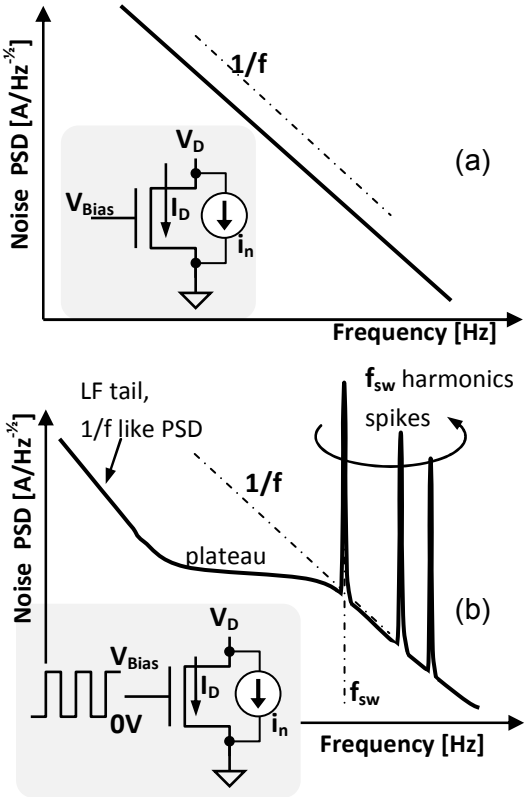

Fig. 1. Logarithmic plot of: (a) a typical MOS low frequency noise PSD, (b) a typical MOS cyclostationary noise PSD showing a plateau in the middle, and the 1/f PSD appearing again at lower frequencies.

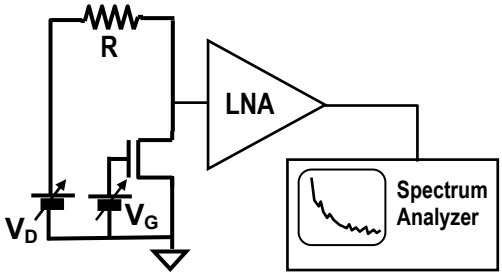

Fig. 2. Simplified typical low noise measurement setup for the characterization of flicker noise in the MOS transistor. The resistor *R* converts the noise current into voltage. LNA = Low Noise Amplifier.

traps to a known empty state, thus introducing some 'order' in the random process. Some reported (measured) cyclostationary MOS flicker noise PSDs resemble the plot in Fig.1(b) [6],[7]. The usual 1/f spectrum is observed above the switching frequency f_{sw}, but at lower frequencies the PSD increases with a much smaller slope like a plateau. Finally, at an even lower frequency the original 1/f spectrum shape can be observed again; the plateau in Fig.1(b) is predicted in [7],[8] among other models, but the latter effect is not properly addressed by current noise models. A possible explanation to the behavior of cyclostationary flicker noise at very low frequency was proposed in [9], but it is not conclusive. A different explanation may be that just another physical random process with a 1/f noise PSD affects the MOSFET but is only visible when the larger PSD of the trapping-detrapping mechanism is drastically reduced in cyclostationary operation. Further measurements while varying some parameters like the oxide thickness t_{ox}, the cycling voltage V_{Bias} of Fig.1(b), the inversion region of the transistor, the switching frequency (f_{sw}), or the duty cycle are necessary to understand cyclostationary noise behavior and to validate any noise model. Very low frequency and/or very low bias current noise measurements are difficult, and noise characterization is challenging when combined with a cycled bias like in Fig.1(b) to such an extent that very few clean spectrums are reported for long channel switched MOS transistors. In this work a specific integrated circuit (ASIC) is proposed for the characterization of flicker noise in the MOS transistor, either switched or not, for a wide range of the DC bias current I_D from tens pA up to few mA, to comfortably cover from deep weak inversion (WI) to strong inversion (SI) regime for the MOSFET.

While there is a lot of reported work in the development of low noise amplifiers, and theoretical noise models, there is much less effort in the development of accurate noise measurement techniques. Most reported measurement setups for the characterization of flicker noise in MOSFETs are based, with minor variations, in the simple one of Fig.2 [1]. A single MOS transistor is biased varying the gate and drain DC voltage, and the AC noise current is amplified and measured by means of a spectrum analyzer. The main problem with the setup in Fig.2 is that it is essentially a common mode circuit

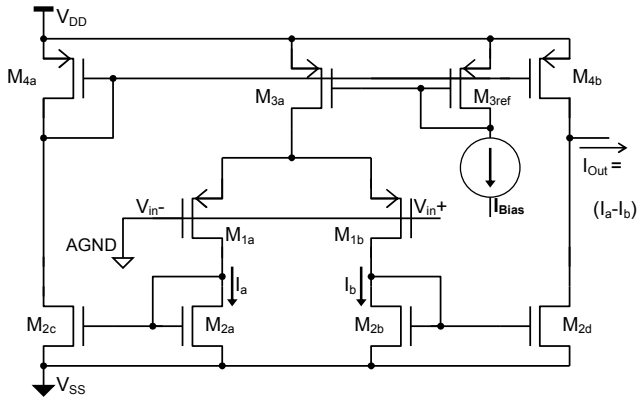

Fig. 3. A symmetrical OTA with shorted inputs to improve noise measurement: it is a differential structure with an active load. On the other hand several noisy MOSFETs affect the measurement. $M_{1a(b)}$ is the DUT.

highly sensitive to coupled noise, and that the small signal gain for the noise source is limited by the upper resistor *R*. Coupled noise is a major problem to solve at very low frequencies overlapping ambient mechanic vibrations. A much more efficient circuit may be the symmetric transconductor (OTA) of Fig.3 where the Device-Under-Test (DUT) are the two identical input transistors $M_{1a(b)}$. In this case the circuit is essentially a differential stage, and *R* is substituted by an active load with very high small signal impedance. On the other hand, the output current PSD contains the undesired noise contribution of every transistor M_i in the OTA. The ASIC developed in this work is based on the chopped OTA proposed in [9] but the modulating switches are modified to ensure the noise of the DUTs is amplified to the output, but the flicker noise of any other transistor in the circuit is cancelled.

II. The Proposed Flicker Noise Measurement Circuit and the Designed ASIC

The proposed circuit is shown in Fig. 4, it was designed in a 0.6µm HV technology as it allows MOSFETs with two different oxide thicknesses (t_{ox1}=12nm, t_{ox2}=41nm) to be characterized. Two circuits were designed: one to measure PMOS DUTs (Fig.4), and another for the NMOS DUTs (not shown). A switching matrix allows the connection of 8 PMOS (NMOS) differential pairs with different aspect ratios and oxide thicknesses (starting at a minimum W/L= 2µm/2µm) to a symmetrical OTA (Fig.4-top) that resembles the one in Fig.3. While 16 different differential pairs and two circuits where included in the ASIC only 1 pair and its corresponding circuit are shown in Fig. 4. $M_{2,3,4}$ are medium sized $(W \cdot L) = 120\mu m^2$ or larger transistors to reduce their flicker noise (flicker noise is inversely proportional to the gate area $W \cdot L$ [1],[2]). The circuit employs a differential structure to reduce coupled noise to a minimum. A chopped [4] operation of the DUTs to further reduce the noise introduced by the mirrors M_{2i}-M_{4i} is also used (Fig.4-bottom). This G_m-C chopper-amplifier was demonstrated in [9], but in the present embodiment three phases are utilized: during ϕ_1, ϕ_2, the DUTs are in 'on' state behaving as a differential pair, during ϕ_3 they are in 'off' state cycling at a switching frequency f_{SW}. A more detailed explanation of each phase follows.

- During ϕ_1: S_{1a}, S_{1b}, S_{in1} are closed, the inputs are shorted to a given common mode input V_{CM}, and S_{Out1} is closed thus the output current is directed to the first integrating capacitor C_1.

- During ϕ_2: S_{2a}, S_{2b}, S_{in1} are closed thus the differential pair is flipped, the inputs continue at V_{CM}, and S_{Out2} is closed thus the output current is directed to the second integrating capacitor C_2.

- During ϕ_3: S_{3a}, S_{3b}, S_{in2} are closed thus the differential pair is turned off (inputs to V_{DD}), and S_{Out3} is closed thus the output current is discarded to a DC voltage source V_{Ref}.

ϕ_3 is the 'off' state of cyclostationary operation, while ϕ_1, ϕ_2 are the 'on'state but the transconductance sign is flipped on each phase. Flipping the DUTs can be associated to flicker noise modulation exemplified with i_{n1} in Fig. 4, which is demodulated back in the output capacitors (chopper principle [4],[9]). On the other hand flicker noise from $M_{2a,b,c,d}$ and $M_{4a,b}$

is modulated only once thus shifted by the modulating frequency f_{SW} to a much higher frequency. At the output, the A_{diff} stage has a low-pass characteristic to eliminate $M_{2i,}$ M_{4i} noise exemplified with i_{n2} in Fig. 4, and further amplifies DUT noise. A B=4:1 copy factor was selected from the inner OTA branches to the output to provide some current gain. Larger copy factors were not selected to avoid large parasitic capacitances in M_2 gates limiting the measurement bandwidth at very low bias currents. The S_{3a},S_{3b} switches are not strictly necessary unless noise at a very low I_{Bias} is measured; these switches are closed during ϕ_3 to make sure I_a, I_b are kept at their steady state value thus reducing the recovery time when the differential pair is turned on again. M_{3b}-M_{2e} is a dummy circuit branch solely included to set V_X node voltage. The S_5 switch is always closed to short the inputs V_{in}+, V_{in}- like in Fig.3 for noise measurements, where both inputs are cycled through V_{CM} (ϕ_1,ϕ_2) and V_{DD} (ϕ_3) like in Fig.1(b) ($V_{CM} = V_{Bias}$). But the switch S_5 was included to separately drive V_{in}+, V_{in}- to measure the DC transconductance and other characteristics with a Source-Measurement Unit (SMU). All S_{ix} (i=1,2,3) switches are minimum length NMOS transistors. The S_1 to S_3 switches are replicated for each of the 8 DUT pairs in each circuit and an integrated digital decoder (not shown) helps to select the proper switch bank. All the pairs share the same input nodes and are connected to the same output as depicted in Fig.4. Switches are controlled by digital signals from an external FPGA or microcontroller.

It should be pointed that though it looks simple, it is very complex to describe with analytic expressions the chopped G_m-C of Fig.4. A deep analysis using the Switched Continuous Time Filter (SCTF) theory is presented in [9] including a white noise analysis showing the effect of noise aliasing can be neglected. The objective of this work is to present the ASIC to accurately measure MOSFET flicker noise in continuous and cyclostationary operation, and not to discuss complex signal processing issues related to the G_m-C chopper that are well detailed in [9]. From [9], the output noise PSD for frequencies below f_{SW} is:

$$S_{V_{Out}}(f) \approx 2 \cdot S_{DUT}(f) \cdot \left| \frac{4 \cdot g_{mDUT} \cdot R \cdot A_{diff}}{(1 + j2\pi f \cdot 2RC)} \right|^2 \qquad (2)$$

where C_1=C_2=C, g_{mDUT} is the DUT transconductance, and R_1=R_2=R in Fig.4(bottom). R, C and the differential low-pass stage A_{diff} are external circuits to set the proper gain and pole frequency f_P=1/(4πRC), to best fit each measurement.

III. SIMULATION RESULTS

The circuit of Fig.4 was designed in a 0.6µm technology, and is currently being fabricated. Meanwhile, some simulated results are presented. The circuit was simulated with a bias current I_{Bias} ranging from 200pA to 2mA in different configurations; this range comfortably covers from WI to SI regime. The circuit was simulated in steady state (ϕ_1 or ϕ_2), as a chopper for a continuous biased DUT (cycling ϕ_1-ϕ_2), the non-chopped cyclostationary DUT case (cycling ϕ_1-ϕ_3), and the complete ϕ_1-ϕ_2-ϕ_3 case. In Fig.5 a transient SPICE simulation is presented in the latter case, for a sinusoidal $5nA_p$ input noise

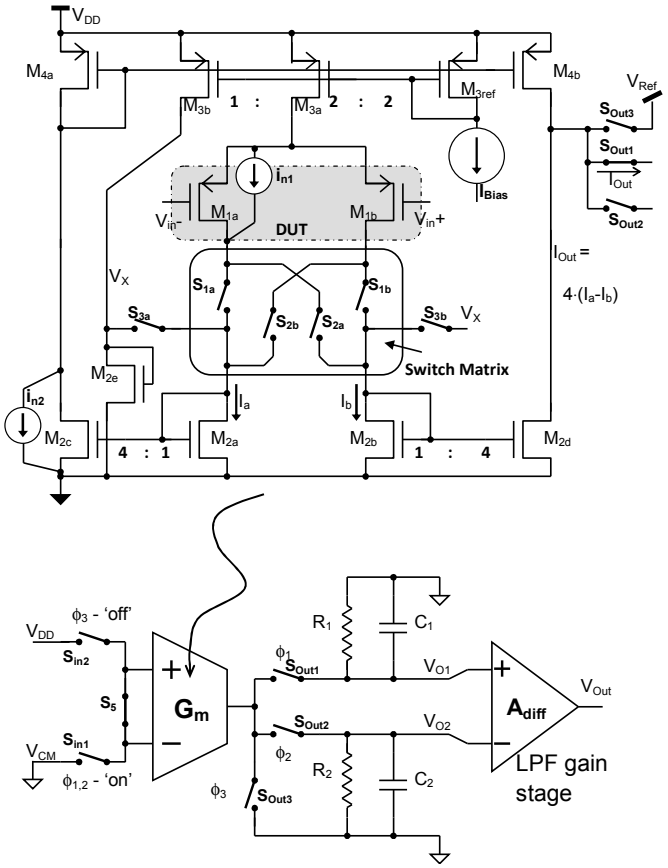

Fig. 4. A symmetrical OTA with a B=4 copy factor to its output is connected by means of a Switch Matrix to a set of 8 PMOS pairs. The matrix allows flipping the input transistors to build a G_mC chopper as proposed in [9] but the input modulator is placed ahead of the input transistors, not before. Thus the DUT noise is amplified to the output. The OTA inputs are shorted and cycled between 'on' and 'off' states to measure cyclostationary flicker noise.

current i_{n1} in parallel with the DUTs of the top, and for a $20nA_p$ sinusoidal noise current i_{n2} in parallel with M_{2c} mirror transistor (bottom). The plots in Fig.5 were obtained using W/L = 8µm/2µm M_1 DUTs, a 200nA bias current I_{Bias}, and ϕ_1-ϕ_2-ϕ_3 phases equal in time and alternating at f_{SW} = 1kHz. While a sinusoidal noise current is an unrealistic test, it helps to verify the flicker noise cancellation. In these simulations R=1MΩ, C=2.2nF, and the differential amplifier A_{diff} of Fig.4 was substituted by a 3rd order Sallen-Key low pass filter with unitary gain and a cut-off frequency of 400Hz. Note on the top of Fig.5 the output simulated amplitude is $V_{Out} \approx 13mV_p$ in agreement with the expected value: $V_{Out} = (B \cdot i_n \cdot R \cdot D_{ON}) = (4 \cdot 5nA \cdot 1M\Omega \cdot (3/2)) = 13.3mVp$. D_{ON} is the 'on' time duty cycle (ϕ_1+ϕ_2). For i_{n2} in the bottom of Fig.5 only a 200µVp residual voltage is observed at the output. Using a C = 220pF capacitor the bandwidth for noise measurement of the G_mC in eq.(2) was extended to 720Hz but is limited to 400Hz by the Sallen-Key. Up to this frequency V_{Out} due to i_{n1} was simulated at ~ 13mVp (Fig.6) and V_{Out} due to i_{n2} also remains ~ 200-400 µVp. The proposed chopper as expected amplifies DUTs' low frequency noise while canceling mirror transistors' low frequency noise.

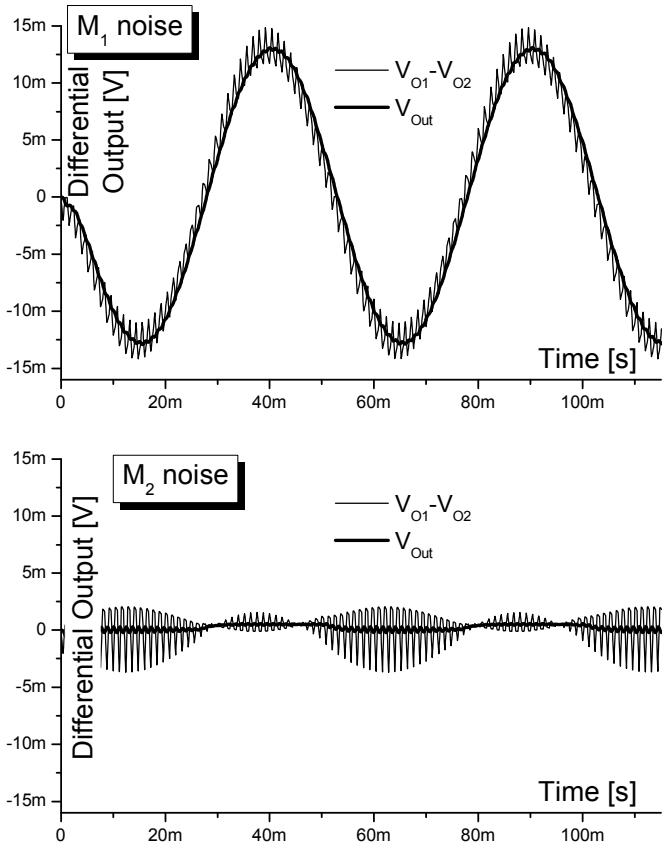

Fig. 5. Simulated transient output noise for an hypothetical 5nA$_p$-20Hz sinusoidal i_{n1} DUT noise current on the top, and simulated transient output noise for an hypothetical 20nA$_p$-20Hz sinusoidal i_{n2} mirror noise current at the bottom. f_{SW} = 1kHz, R=1MΩ, C=2.2nF, A_{diff} is a 400Hz 3rd order LPF, $g_{mDUT} \approx 2\mu S$, and the three phases are equal in time.

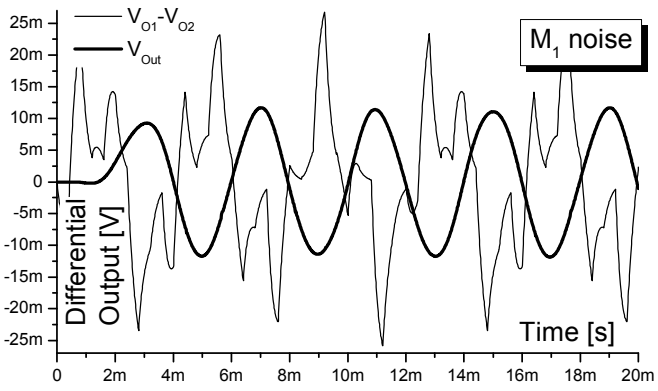

Fig. 6. Simulated transient output noise for an hypothetical 5nA$_p$-250Hz sinusoidal i_{n1} DUT noise current. f_{SW} = 1kHz, the circuit is the same of Fig.5 but C=220pF.

IV. CONCLUSIONS

Very low frequency flicker noise, particularly cyclostationary flicker noise, is known to be difficult to measure. The main experimental problems are the low currents down to few nA or less involved in the WI region, coupled noise when an isolated DUT is measured, and the noise of other devices in the experimental setup. To overcome these difficulties, a specific integrated circuit (ASIC) aimed at flicker noise measurements in different types/sizes of test transistors and at different bias conditions was presented. The circuit is a GmC chopper as proposed in [9] but the input modulator is placed ahead of the input transistors, not before. Thus the DUT noise is amplified to the output while the remaining transistors' noise is cancelled. The circuit was simulated in a wide range of operating conditions.

The proposed ASIC is a flexible tool for the measurement of low frequency noise that may be operated for a continuous biased or cyclostationary DUT transistor, either like a chopper or not. This circuit may help to implement accurate noise measurements in a compact way avoiding complex, large, and expensive isolating structures like Faraday cages. The proposed ASIC may help to acquire a wide set of cyclostationary flicker noise PSD spectra as needed to validate cyclostationary flicker noise models that are being proposed.

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