

# A fully integrated preamplifier for cardiac sensing in a HV-CMOS technology.

J. Lasa, G. Member, A. Arnaud, Member, M. Miguez, G. Member

**Abstract**—A novel fully integrated preamplifier stage for cardiac activity sensing is presented. The proposed design takes advantage of the High Voltage CMOS (HV) technology properties to comply with the safety requirements of implantable devices without the addition of external decoupling capacitors. The power consumption is minimum; while the input referred noise is kept well below the minimum signal to be sensed. This first stage is a high pass filter with a cut off frequency at 75Hz, and 25db gain. Simulation results are presented, the circuit is being fabricated in a 0.6 $\mu$ m technology.

## I. INTRODUCTION

Pacemakers sense the natural electric activity both of the atrium and the ventricle of the heart to determine whether is necessary to stimulate it or not [1]. But also modern pacemakers may perform intracavitary electrocardiography (ECG) to record patient's information for the physician. These features are based in a sometimes complex amplifier at the input stage. There is at least an amplifier for each chamber [1] [2] [3].

Microelectronics steadily contributes to the development and improvement of medical devices. Three crucial, specific, aspects in the design of implantable devices are: low power consumption to extend as much as possible the battery life, to avoid the use of external components like resistors and capacitors to reduce the size, and to develop safety and reliable circuits in contact with the patient. In the case of amplifiers, combining low noise and low power becomes also a challenge [5].

A 2.8V (nominal) Lithium-Iodine battery normally power most modern pacemakers. To achieve the larger voltages required during operation, efficient voltage multipliers can be employed [6].

Manuscript received March 30, 2010. This work was fully supported by the "Agencia Nacional de Investigación e Innovación" under Grant "Fondo Clemente Estable – FCE2007\_592".

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Regarding to the safety of an implantable device, it shall comply the following rule: any single failure (may be a punctured gate in a MOS transistor, software bug, among others) must not cause a catastrophic event. In the case of a circuit in contact with the heart, a catastrophic event may be a significant (for example larger than few  $\mu$ A) DC current flow to tissue, or a too high artificial pace rate. In this work the focus will be on the former that is closely related to the design of analog circuits directly connected to the electrodes. The traditional solution to attain safety in a cardiac sensing amplifier is to include capacitors in series with the amplifier's input [1] [2] [3] [4]. If any transistor at the input of the amplifier fails, the series capacitor blocks DC current. Series capacitors also help to fix a low frequency pole in the transfer function of the input filter-amplifier. But the use of series capacitors (two for each amplifier) increases the external components count, thus it will be valuable to develop inherently safe circuits that avoid them. In this work, the so called high voltage (HV) CMOS technology, and fully isolated NMOS transistors, will be combined with low noise and low power designed techniques, to develop a preamplifier aimed to be the input stage in a pacemaker that avoids the use of external capacitors. A 0.6 $\mu$ m HV-CMOS technology was employed for the circuit; it includes transistors capable of withstanding even tenths of volts. In spite of the existence of several techniques for the use of standard CMOS technology with relatively high voltages, HV technology is preferred because medical equipment manufacturers strictly follow the integrated circuit (IC) manufacturer rules. Even in the case of pacemakers that deliver stimuli with voltages up to 7.5V or a bit more. In the case of this work also, the use of a HV technology allows the implementation of a safe preamplifier.

## II. SPECIFICATIONS

The general architecture of the proposed system, shown in Fig.1, is to sense cardiac signals. It includes a 25dB gain input stage (the preamplifier), a band pass filter-amplifier between 75Hz and 200Hz, and a low offset programmable comparator to trigger cardiac

activity detection [3]. In the case of intracavitary ECG the preamplifier can be shared, but the rest of the signal path shall be different. In this work we will focus on the preamplifier stage because it is the one in electrical contact with the patient thus safety issues must be taken into account.

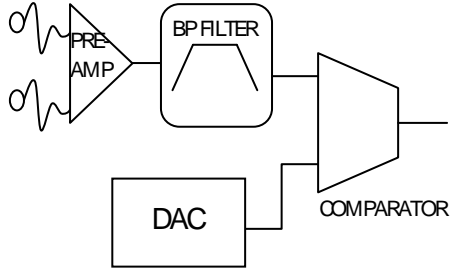


Fig 1. The complete system for cardiac sensing.

The preamplifier is a high pass one, with a cut off frequency at 75Hz and a 25 dB gain. In Table I, detailed specifications are shown. The very high supply voltage  $V_{dd}$  used (8V or approximately three times the battery voltage), was already generated for the stimulation circuits using a standard pacemaker battery, and a voltage multiplier like the one in [6].

TABLE I  
FIRST STAGE SPECIFICATIONS

Specification	
Supply Voltage ( $V_{dd}$ )	6-8.4V
Power Consumption	$\ll 1\mu W$
High pass, cut off Frequency	75Hz
Gain	$>25dB$
Area	$<1mm^2$

### III. CIRCUIT DESCRIPTION

The selected HV technology, allows implementing several types of transistors, the proposed design uses, apart from regular low-voltage ones, the following:

1) PHV: This is a HV-PMOS uses thick gate oxide and a diffused drain to withstand  $V_{GS}$ ,  $V_{DS}$  voltages up to 18V, and 40V respectively.

2) NHV: Is the equivalent HV-NMOS, can withstand  $V_{GS}$ ,  $V_{DS}$  voltages up to 18V, and 30V respectively.

3) NISO: This is a completely isolated HV-NMOS transistors, it can withstand  $V_{GS}$  voltages up to 18V and  $V_{DS}$  voltages up to 50V.

The high pass filter's schematic is shown in Fig. 2, it has a differential input  $V_{in}$  directly connected to the electrodes, and differential output  $V_{out}$ . It consists of a PHV current mirror,

a NISO differential input pair, a NHV current mirror and a symmetric transconductor (OTA)  $G_M$ .

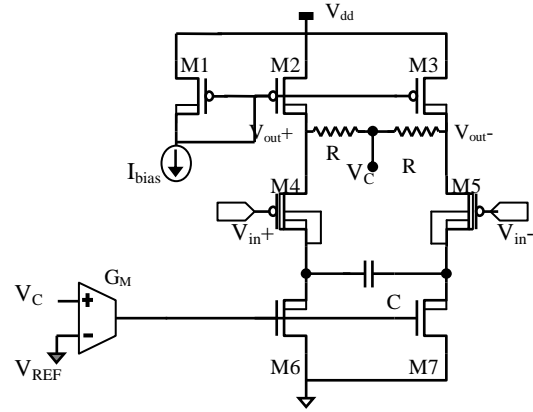


Fig 2. First stage: high pass filter. Specifications of transistors M1:M7 are shown in Table II.

The circuit is a variation of the one presented in [9][10] but uses a symmetric OTA in a common mode feedback loop to set the common mode of the output  $V_C$ . By controlling the current through M6 and M7, the OTA responds to variations of  $V_C$  and fixes it equal to a reference voltage  $V_{REF} \cong V_{dd} - 0.8V$ .

Conducting a small signal analysis in Fig.3, the high pass filter's transfer function  $H_1(j\omega)$  can be determined in (1) to (5).

TABLE II  
M1:M7 TRANSISTOR TYPE, SIZE

MOS	Type	W-L ( $\mu m$ )
M1, M2, M3	PHV	40-20
M4, M5	NISO	50-9
M6, M7	NHV	40-20

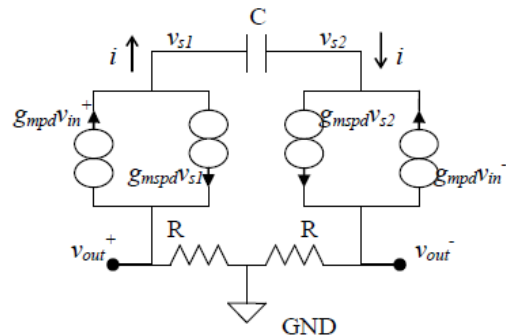


Fig 3. High pass filter small signal model.

$$i = g_{mpd} \cdot v_{in}^+ - g_{mspd} \cdot v_{s1} \quad (1)$$

$$g_{mspd} = \eta g_{mpd} \quad (2)$$

$$i = -g_{mpd} \cdot v_{in}^- + g_{mspd} \cdot v_{s2} \quad (3)$$

$$i = (v_{s1} - v_{s2}) \cdot Cj\omega \Rightarrow v_{s1} - v_{s2} = \frac{1}{Cj\omega} \quad (4)$$

$$H_1(j\omega) = \frac{R \cdot g_{mpd} \cdot j\omega}{j\omega + \frac{\eta g_{mpd}}{2C}} \quad (5)$$

where  $R$ ,  $C$ , are those in Fig.3,  $g_{mpd}$ ,  $g_{mspd}$ , are the gate and source transconductances of the differential input pair respectively,  $\eta=1-1.5$  is the slope factor [12].

The idea is to avoid the use of external capacitors. According to the available area budget, the largest capacitor that could be used is a 400pF poly-poly one that occupies an area of  $0.22\text{mm}^2$ . To implement the 25dB gain and a cut off frequency at 75Hz, and setting  $C$  to 400pF, results:

$$g_{mpd} = \frac{4\pi \cdot C \cdot f}{\eta} = 0.314 \mu\text{s} \quad (6)$$

$$\frac{G}{g_{mpd}} = R = 56.6\text{M}\Omega \quad (7)$$

At such a low  $g_{mpd}$  all the MOS transistors were biased in weak inversion, an all region model was used for the design space exploration [12]. The bias current  $I_{bias}$  for the preamplifier is only 20nA that results in very low power consumption even with a large  $V_{dd}$ . Because of the low  $I_{bias}$  current, careful noise verification is necessary. The total input referred noise of the preamplifier is estimated in  $4.5\mu\text{V}_{rms}$ , a value several times lower than the minimum atrial signal that shall be detected [1][2].

The total power consumption of the circuit, including the common mode feedback OTA ( $G_M$ ) is 600nW at a nominal  $V_{dd}=8\text{V}$ .

#### IV. SAFETY CONSIDERATIONS

Regarding safety, the amplifier in Fig.2 does not deliver a DC current to the tissue even in the case of a single failure. In effect the electrodes are connected to the gate of M4 and M5, in the case of a punctured gate, or gate to source (drain) conductive path, the current through the mirrors is limited to the 20nA  $I_{bias}$  copy. Thus no external decoupling capacitors are required. To complete the safety analysis it should be pointed that the OTA ( $G_M$ ) is also HV, and that under regular operation (no extra failures) the bias voltage of the electrodes is such that all parasitic diodes in the MOS transistors are reverse biased. Also special electrostatic discharge (ESD) protections were included, but the discussion of ESD is avoided for the sake of simplicity.

#### V. FILTER SIMULATION RESULTS

The circuit was simulated, and the physical layout of the filter can be seen in Fig. 4. The total occupied silicon area is  $0.97\text{mm}^2$ . All simulations presented are post-layout ones, including parasitic effects.

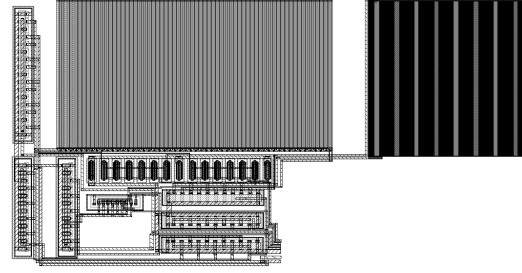


Fig 4. Complete filter layout. Top right, capacitor C, to the left resistors R, and below isolated transistor and in the bottom, the common mode feedback transconductor.

In Fig. 5, the transfer function of the preamplifier is presented. The simulated gain is 26dB and the cut off frequency is 75Hz. It should be noted that the filter acts as a band pass filter because it is powered by a very low current, and the parasitic capacitors of the large transistors employed result in a low pass pole at approximately 1kHz, which is much greater than the largest frequency of interest. Simulations were also carried for corner cases using the different transistor and resistor models provided by the foundry, the results can be seen in Table III. Two transient simulations are also presented in Fig. 6, with a sine wave input of  $V_{max}=1.2\text{mV}$  and 100Hz. In Fig.7 the output of the preamplifier is shown, when the so called Tokyo wave was used as the input signal. This wave is the standard one defined to test sensing amplifiers for cardiac pacemakers [11]. In Fig.7 both a positive and a negative Tokyo signal with  $V_{max}=2.9\text{mV}$  were simulated.

TABLE III  
FILTER SIMULATIONS (WS = worst slow, larger  $V_T$  transistors; WP = worst power, smaller  $V_T$  transistors)

	Typical Model	WP Model	WS Model
Gain (dB)	26	24	27.5
Cut-off Frequency (Hz)	75	97	66.5
Consumption ( $\mu\text{W}$ )	0.60	0.60	0.60

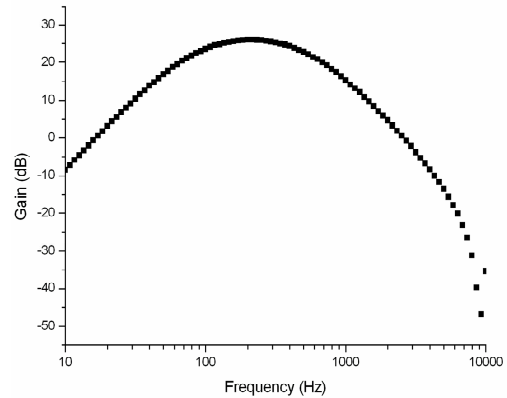


Fig 5. High pass filter transfer function. Gain = 26dB,  $f_c = 75\text{Hz}$ .

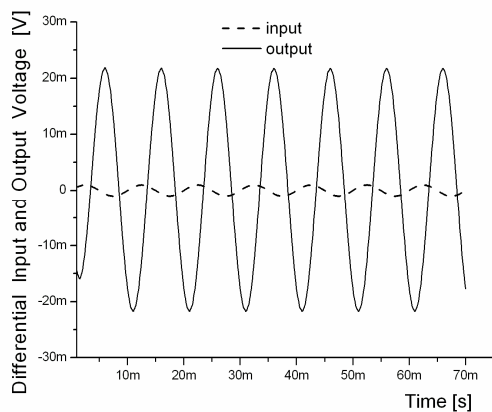


Fig 6. Transient analysis with a sine wave input of 1.2mV and a 100Hz frequency.

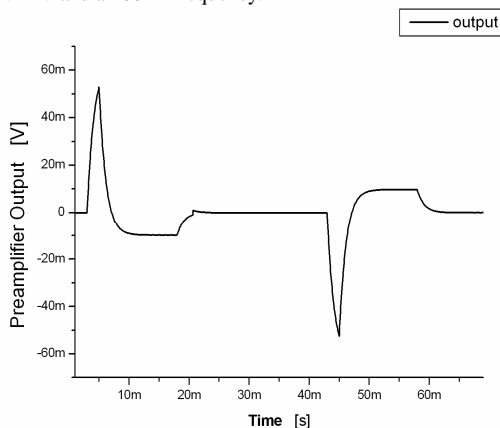


Fig 7. Output when the input is a positive(negative) Tokyo signal of  $V_{max}=2.9mV$ . At 3ms the positive Tokyo signal starts and at 42ms the negative one.

## VI. CONCLUSION

A completely integrated high pass preamplifier, with 25db gain,  $4.5\mu V_{rms}$  input referred noise (70-200Hz), and 600nW power consumption was successfully designed in a  $0.6\mu m$  HV technology. Due to the low bias current, the use of HV and isolated input transistors, the preamplifier does not necessarily require the use of decoupling capacitors. Although a specific safety analysis must be completed on each circuit specially taking in to account the bias voltage of the electrodes when sensing, the proposed technique enables to remove external decoupling capacitors.

Future work on this circuit includes precise noise measurements, and intracavitary ECG signal recording capability.

## REFERENCES

- [1] J.G. Webster (Eds.), *Design of Cardiac Pacemakers*, IEEE Press: New York, 1995. ISBN0-7803-1134-5.
- [2] F. Silveira, D.Flandre, *Low power analog CMOS for cardiac pacemakers—design and optimization in bulk and SOI technologies*, Kluwer Academic Publishers, 2004. ISBN 140207719X.
- [3] D.Prutchi, chapter 8 in *Design & Development of Medical Electronic Instrumentation*, Wiley-Interscience, 2004. ISBN 0471676233
- [4] L. Lentola, A. Mozzi, A. Neviani, and A. Baschirotto, "A 1  $\mu A$  front end for pacemaker atrial sensing channels with early sensing capability" *IEEE Transactions on Circuits and Systems -II*, vol.50, no. 8, pp. 397–403, 2003.
- [5] A. Arnaud and C. Galup-Montoro, "Consistent noise models for analysis and design of CMOS circuits.", *IEEE Transactions on Circuits and Systems -II*, vol. 51, no. 10, pp. 1909–1915, 2004.
- [6] Wong, L. S. Y., et al. (2004). A very low power CMOS mixed signal IC for implantable pacemaker applications. *IEEE Journal of Solid State Circuits*, 39(12), 2446–2456.
- [7] D. Linden and T.B. Reddy (Eds.), *Handbook of Batteries*, 3d ed., McGraw Hill, 2002, ISBN-0-07-135978-8.
- [8] A.Arnaud, J.Gak, M.Miguez , "A self-protected integrated switch in a HV technology", in Proc. 22th Symposium on Integrated Circuits and Systems Design - SBCCI 09 - Natal, Brazil - Sep.2009.
- [9] Sacristan, J., & Oses, M. T. (2004). Low noise amplifier for recording ENG signals in implantable systems. *IEEE International Symposium on Circuits and Systems (ISCAS'04)*, IV, 33–36.
- [10] A.Arnaud, M.Miguez, J. Gak, M. Bremermann, "On the Reduction of Thermal and Flicker Noise in ENG Signal Recording Amplifiers". *Journal Analog Integrated Circuits and Signal Processing (AICSP)*, Volume 57, Numbers 1-2 / nov.2008 pp.39-48
- [11] European Standard EN 45502-2-1 "Active implantable medical devices. General requirements for safety, marking and information to be provided by the manufacturer", 1998.
- [12] A.I.A. Cunha, M.C. Schneider, C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998