

# Complete Integrated Cardiac Sensing Channel for Pacemakers

J. Lasa, M. Miguez, A. Arnaud

**Abstract**—A novel complete integrated circuit for cardiac sensing is presented. The design eliminates the use of external components, while also keeping up with the safety requirements and low power consumption of implantable medical devices. The work was developed using a high-voltage technology (HV, XC06 technology was selected [1]). The first stage consists of a completely integrated high pass preamplifier, with 25db gain,  $4.5\mu V_{rms}$  input referred noise (70-200Hz), and 600nW power consumption. The second stage is a 55-180Hz GmC filter that incorporates the ability to filter input signals with a high common mode input up to 15V. Moreover, a novel full wave precision rectifier and a low power comparator are presented to complete the cardiac sensing channel.

## I. INTRODUCTION

The circuit block for sensing the cardiac activity is one of the main blocks of a pacemaker. The task of the circuit is to amplify natural electric signals from a cardiac chamber, and provide a single bit digital output that indicates when this signal is above a given programmed voltage level (the output of the sensing channel normally triggers an interruption, a sense event in the pacemaker's microcontroller). This block generally consists of a preamplifier, a band pass filter, and a programmable voltage detector [2][3][4][5]. In this implementation it includes a band pass filter with two cut off frequencies, 70Hz and 200Hz approximately, followed by a full-wave precision rectifier and a comparator that perform the signal detection [3]. Usually, the lower cut off frequency is set using an external capacitor, but in this work a complete integrated ASIC without external components is designed. Commonly, the cardiac sensing is made directly over the electrodes connected to tissue; therefore the designer must be aware of possible failures and shall prevent causing damage to the tissue in case one of this occurs. For example, if the gate of an input MOS is punctured, a DC current must not circulate through the tissue, because this could cause an irreparable damage to the patient.

The general architecture of the whole proposed system to sense cardiac signals is shown in Fig. 1. It includes a 25dB gain input stage (the preamplifier), a band pass filter-amplifier between 75Hz and 200Hz, a full wave precision rectifier and a low offset programmable comparator to trigger cardiac activity detection. All the elements in Fig. 1, with the exception of the DAC, will be presented in this work.

J. Lasa, A. Arnaud and M. Miguez are with Electrical Engineering Department, Universidad Católica del Uruguay, Montevideo, Uruguay. (phone: +5982 4872717 / 464, fax: +5982 4872842, jlasa@ieee.org).

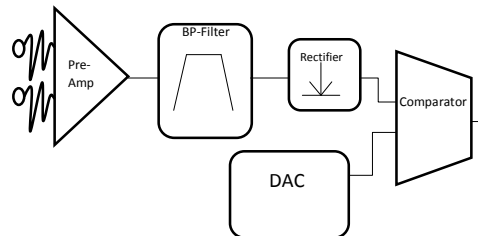


Fig. 1. System's Architecture.  
(The DAC is not part of this work)

In the second section, the design of a fully integrated preamplifier capable of sensing cardiac activity is presented. In section III, a biomedical G<sub>m</sub>C filter, which would also work as a second stage amplifier is discussed.

The design of a full wave precision rectifier and a low offset comparator is presented in the following section, in order to complete the cardiac sensing channel. By rectifying the signal, the detection can be completed in a single comparator for both positive and negative voltage peaks. Finally in section V, the simulated results of the full circuit is shown, followed by some conclusions.

## II. PRE-AMPLIFIER

The design of the Pre-Amplifier has three main objectives:

- Reduce as much as possible the number of external components (to zero if possible).
  - Comply with all the safety specifications and requirements for implantable medical devices.
- Minimize the power consumption

The preamplifier is a high pass filter, with a cut off frequency at 75Hz and a 25 dB gain. In Table I, detailed specifications are shown. As a second stage is used, the preamplifier can have a larger bandwidth to enable both traditional sensing and intracavitary electrocardiography recording with the same preamplifier (not shown in Fig. 1). Additionally, the preamplifier is able to sense signals with a high common mode voltage, up to 8V and is also powered with a high voltage power supply. High voltages are regularly employed for the electrical stimulation of tissue. In this case the high supply voltage  $V_{DD}$  used is generated from the battery with an x2 or x3 charge pump voltage multiplier [7] and is used to deliver voltage stimuli of up to 7.5V.

The preamplifier schematic is shown in Fig. 2 and it has a high-pass filter characteristic. It has a differential input  $V_{in}$  directly connected to the electrodes, and a differential output  $V_{OUT}$ . It consists of a PHV (high voltage PMOS) current mirror, a NISO (isolated NMOS) differential input

pair, a NHV (high voltage NMOS) current mirror and a symmetric transconductance (OTA) Gm.

TABLE I  
PRE-AMP SPECIFICATIONS

Specification	
Supply Voltage ( $V_{dd}$ )	6-8.4V
Power Consumption	$<1\mu W$
High pass, cut off Frequency	75Hz
Gain	$>25dB$
Area	$<1mm^2$
Noise	$<10\mu V_{rms}$

The circuit is a variation of the one presented in [8, 9] but uses a symmetric OTA in a common mode feedback loop to set the common mode of the output  $V_C$ . By controlling the current through M6 and M7, the OTA responds to variations of  $V_C$  and fixes it equal to a reference voltage  $V_{REF}$ .

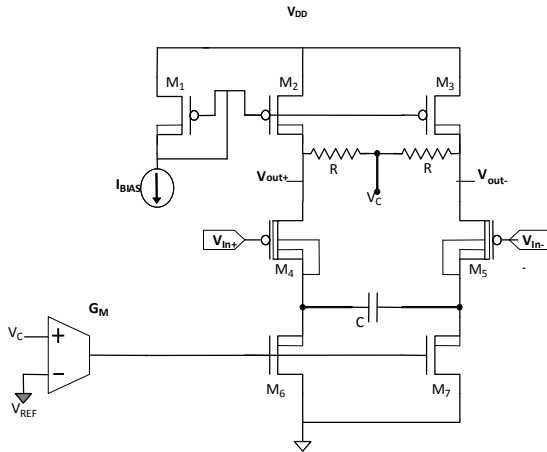


Fig. 2. First stage: high pass filter-amplifier.

A completely integrated 25db gain high pass preamplifier, with only  $4.5\mu V_{rms}$  input referred noise, and 600nW power consumption was designed and simulated. Due to the low bias current and the use of HV and isolated input transistors, the preamplifier does not necessarily require the use of decoupling capacitors, reducing external components to zero.

### III. GMC FILTER

The second stage is a GmC filter to remove undesired spectral components and also to further amplify the signal. As pointed in [3] the information to detect natural electrical cardiac activity is mostly contained in the band from 70 to 200Hz, thus the GmC filter shall be a band pass one approximately in that range. Low power consumption and low noise where the two most important aspects taken into consideration when designing this stage. Because transconductance element's value suffer from a high degree of uncertainty due to technology parameters fluctuations between an IC to another (and a fabrication batch to another), a detailed analysis was performed to keep the filter response within the 5% boundary imposed by common pacemaker standards (no trimming or filter tuning is assumed).

In [5][7] a discrete time switched capacitors filter is proposed for a similar task, while in [4][10] a continuous time RC one is presented but the circuit requires precise

external components. In comparison to the mentioned approaches, GmC filters may result in minimum power consumption and a fully integrated solution. But while filter accuracy is not crucial for the application as cardiac sensing level is adjusted by the physician in a pacemaker therapy; the standards may impose certain minimum accuracy in the response of the circuit. Therefore to avoid individual trimming of the devices, the GmC filter must be precise. The standard in [11] for example, uses the so called Tokyo signal as the normalized test signal; and defines a mandatory 5% accuracy in the detection. Fig. 3 presents this wave (consecutive positive-negative pulses). It is important to highlight that the signal to detect has amplitude between a minimum of  $200\mu V$  and maximum of 10mV approximately. But note from the Tokyo signal Fourier transform in Fig. 4 and the analysis of Fig. 5 that the high frequency pole does not necessarily have to be as accurate (a 10% variation in it results in much less than  $\pm 5\%$  variation of the signal amplitude at the output); while the position of the low frequency pole has a limited yet still significant impact (around 8% for the maximum expected pole variance). Both results (Fig. 4 and Fig. ure5) were obtained using a Scilab script that filters an ideal Tokyo signal with a band pass varying the position of the poles.

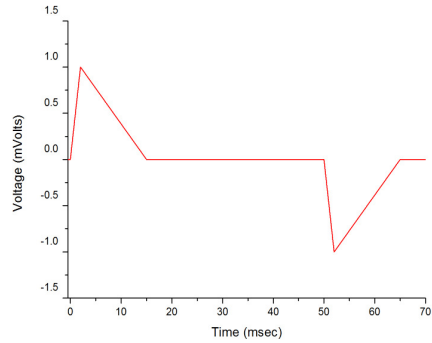


Fig. 3. Tokyo signal

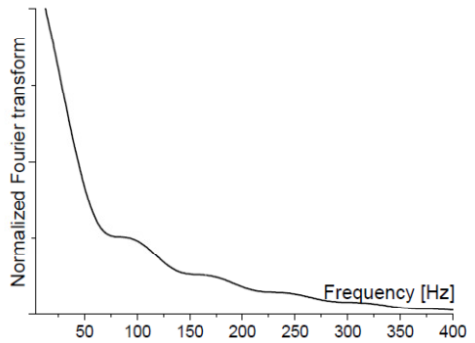


Fig. 4. Fourier transform of the Tokyo signal.

The proposed GmC is shown in Fig. 6 and Table II. The selected band pass filter topology in the picture has a total stage gain of  $G = 22 dB$ . The filter is composed of a low pass gain structure (given by  $G_{m1}$ ,  $G_{m2}$ ,  $C_2$  similar to that proposed in [12] for a capacitive microphone), and a DC cancellation loop (given by  $G_{m3}$  and  $C_1$ ). Capacitors are integrated and of the double poly type.

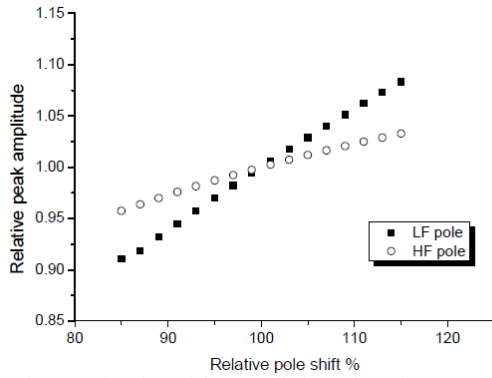


Fig. 5. Estimation of the overall channel sensing accuracy.

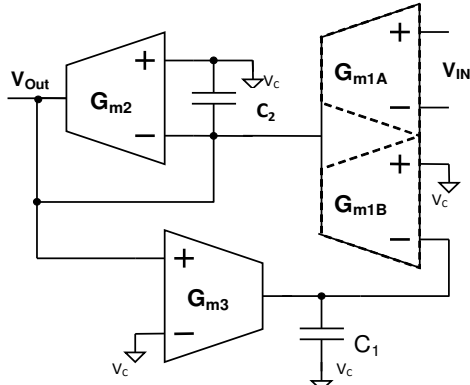


Fig. 6. A schematic of the designed  $G_mC$  filter for the sensing channel.

TABLE II

	Value	Comments
$G_{m1}$	$1\mu S$	Dual input. HV input capacity on one side
$G_{m2}$	$80nS$	Resistor-linearized OTA $\pm 500mV$ range
$G_{m3}$	$1.6nS$	Resistor-linearized OTA $\pm 500mV$ range
$C_1$	$105pF$	Poly-Poly Capacitor
$C_2$	$45pF$	Poly-Poly Capacitor

$G_{m1}$  is a double differential input transconductor. The first input is connected to the preamplifier stage output, thus it shall support a high voltage common mode input. The second input is used as a feedback port for DC cancellation in the scheme of Fig. 6. Only the first OTA input is connected to a high voltage supply (High  $V_{DD} = 8V$ ); the feedback input is powered by a lower  $V_{DD}$  to preserve reduced power consumption. Therefore the  $1\mu S$  double input OTA, shown in Fig. 7, is divided in two parts.

- The HV part has a HV-NMOS differential pair input that was implemented with complete isolated transistors (NISO) biased in Weak Inversion with an  $80nA$  current. The two MOS transistor that bias the input mirror (NHV) and the four PMOS transistor located at the top part of the circuit are also high voltage ones (PHV). The remaining MOS transistors are standard NMOS.
- The low voltage part has a standard PMOS differential input pair also biased in weak inversion with an  $80nA$  current. The current mirror was also implemented with standard PMOS transistors.

To complete the full  $G_mC$  filter, two resistor linearized transconductors (Fig. 8) were designed using the same topology. The input pairs were biased in moderate inversion (MI) and the resistor's value is  $7M\Omega$ . The total current consumption of each transconductor is  $160nA$ .

#### IV. FULL WAVE PRECISION RECTIFIER AND COMPARATOR

The final elements of the cardiac sensing channel are the comparator and the full wave precision rectifier.

The reasons a rectifier was included in the channel design are the following:

- As the cardiac signal may be either positive or negative (depending on how the electrodes where implanted on the patient), two different comparisons were required.
- Because of the previous point, also two DACs were going to be needed. One for each comparator.

Since both positive/negative trigger level are the same in a cardiac sensing channel, another possibility was to use a full wave precision rectifier between the  $G_mC$  filter and the comparator.

This section presents the design of both the comparator and the rectifier designs. Fig. 9 presents the block diagram of the final stage.

A new design was developed for a full wave precision rectifier. Fig. 10 presents the proposed design scheme.

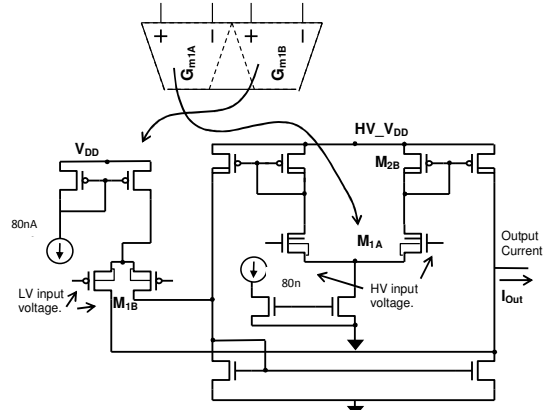


Fig. 7. Double input  $G_m$  Schematic.

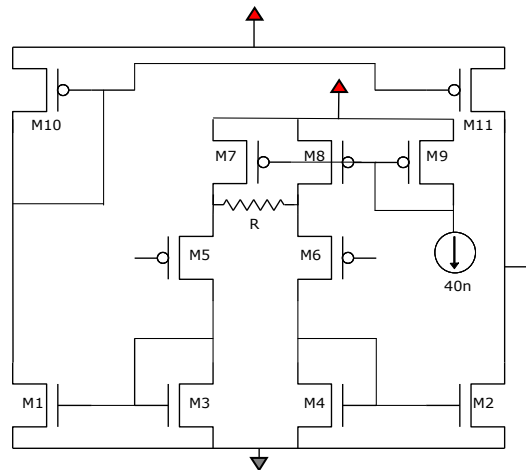


Fig. 8. Schematic of  $G_{m2}$  and  $G_{m3}$ .

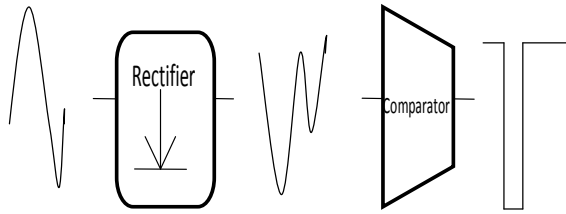


Fig. 9. Final stage block diagram.

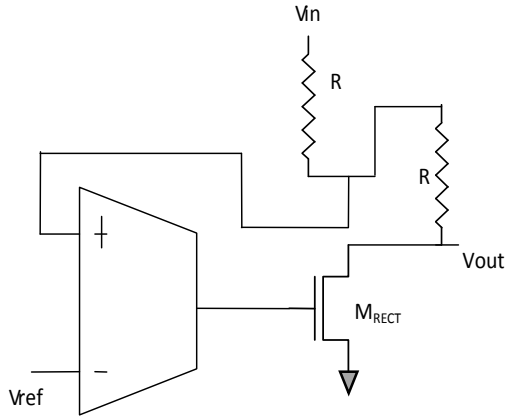


Fig. 10. Full wave precision rectifier's schematic.

When  $V_{in} < V_{ref}$ , the transistor is cut-off. Therefore  $I = 0$  and  $V_{out} = V_{in}$ .

In the case that  $V_{in} > V_{ref}$  the NMOS transistor conducts. Therefore, a feedback loop is established and  $V_+ = V_-$ . As both resistors have the same value:  $V_{out} = V_{ref} - (V_{in} - V_{ref}) = -V_{in}$ .

In Fig. 11, the schematic of the rectifier's OTA is shown.

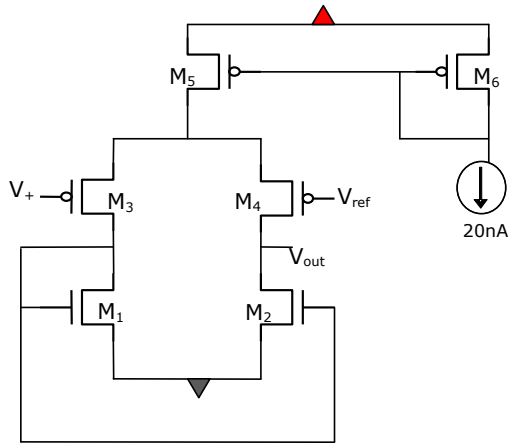


Fig. 11. Rectifier's OTA schematic.

$M_1$  and  $M_2$  were designed with big areas so as to minimize the offset. For the same reason,  $M_3$  and  $M_4$  were designed with big areas as well.  $M_{RECT}$  must behave as a virtual resistance. The resistors  $R$  should be as big as possible to reduce current consumption, and the  $7M\Omega$  value was selected.

Figure 12 shows the schematic of the comparator. The topology includes a simple OTA and three inverters. This topology was used as it was already developed and tested by the research group.

When the voltage difference at the input pair is positive, the current at the OTA's output increases and the voltage goes up. The two inverters attached to the OTA's output were included to increase the output's slope. The resistors decrease the effect of the current peaks when the inverters are changing its state. The circuit has a current consumption of  $60nA$ .

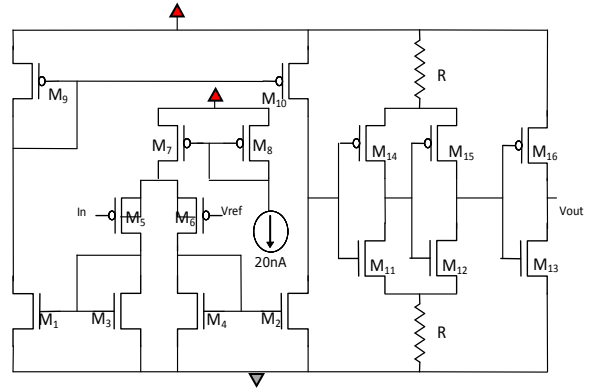


Fig. 12. Comparator's Schematic.

## V. SIMULATIONS

The wave used to simulate and test pacemaker devices is the so called Tokyo wave [2][3][11] (see Fig. 3).

In Fig. 13, the AC transfer function of the preamplifier is presented. The simulated gain is  $26dB$  and the cut off frequency ( $-3dB$ ) is  $75Hz$ . It should be noted that the filter acts as a pass band filter because it is powered by a very low current, and the parasitic capacitors of the large transistors employed result in a low pass pole at approximately  $1KHz$ , which is much greater than the largest frequency of interest. The effect can be exploited also as an antialiasing filter in the case of a possible switched filter second stage.

Simulations were also carried for corner cases using the different transistor and resistor models provided by the foundry. The results can be seen in Table III.

TABLE III  
PRE-AMP AC RESULTS

	TM	WS	WP
Gain (dB)	26	24	27.5
Cut off frequency (Hz)	75	97	66.5
Consumption ( $\mu W$ )	0.60	0.60	0.60

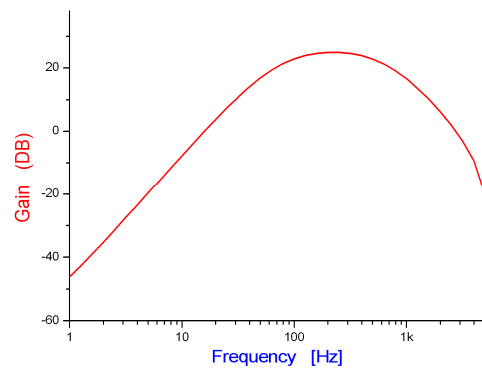


Fig. 13. AC Simulation (TM) of pre-amplifier.

In Fig. 14 the output of the system is shown, when the so called Tokyo wave was used as the input signal. Both positive and negative Tokyo signals with  $V_{\max} = 2.9\text{mV}$ ,  $t_{\text{positive}} = 3\text{ms}$  and  $t_{\text{negative}} = 12\text{ms}$  were simulated.

In Fig. 15 the AC transfer function of the whole system. In this case the simulations results with variation of the transistor's models (TM, WS, WP) of the  $GmC$  and the resistors and the capacitors values within the range provided by the manufacturer.

As Fig. 15 shows, only a 0.42dB gain difference, a 6Hz difference in pole1 and a 13Hz difference in pole2 are observed between the worst case curves. In Table IV the different results are detailed.

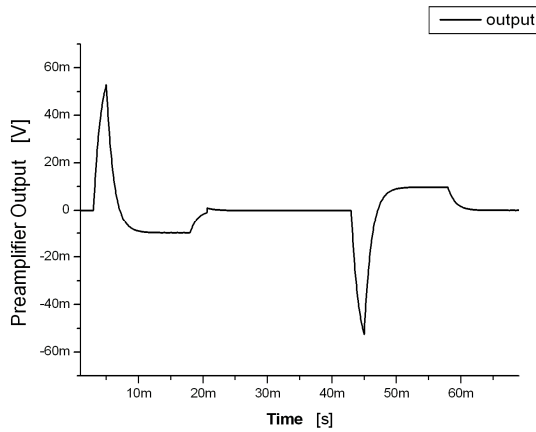


Fig. 14. Output for a positive and negative Tokyo input with an amplitude of 2.9mV.

TABLE IV  
GMC AC RESULTS

	TM	WS	WP	C+	C-	R+	R-
Gain (dB)	46.97	46.91	47.28	46.82	47.12	47	46.86
Low Pole (Hz)	67	64	67	65	70	66	67
High Pole (Hz)	212	203	210	204	216	209	213

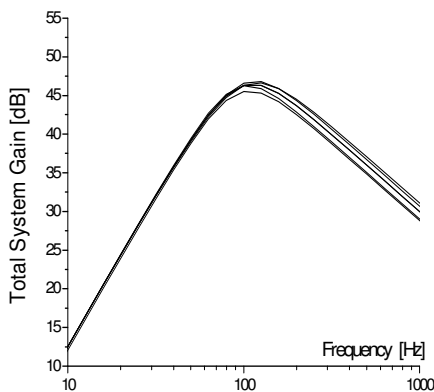


Fig. 15. AC simulation varying several parameters.

Figure 16 presents the transient analysis of the  $GmC$ . Only the positive signal is presented in order to distinguish more easily the differences between the graphs.

Figure 17 shows the peak response of Fig. 15 by varying the global reference current. The result is a monotonic gain increase. Thus to make the filter compliant with the standards it is necessary to adjust a single parameter, the bias current.

In Fig. 18 the transient response of the rectifier is presented. The reference voltage was set to 0.8V.

The transient response of the comparator is shown in Fig. 19. The reference voltage was also set to 0.8V.

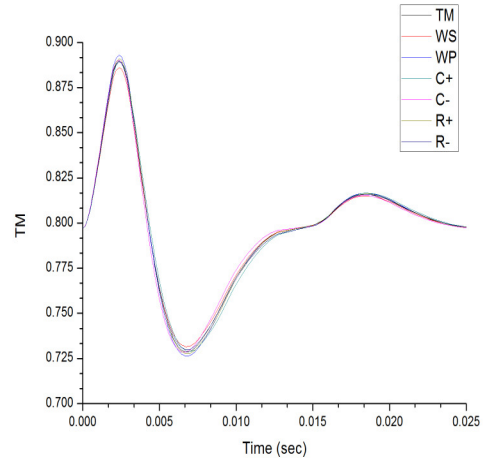


Fig. 16. Transient simulation varying different parameters. Input's amplitude: 1mV.

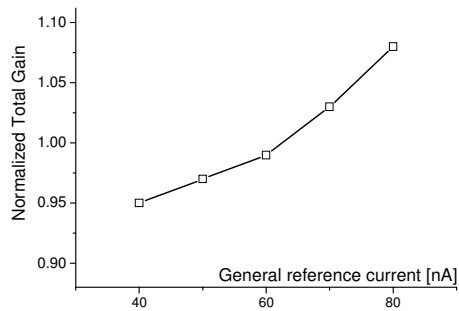


Fig. 17. Peak response to current variation

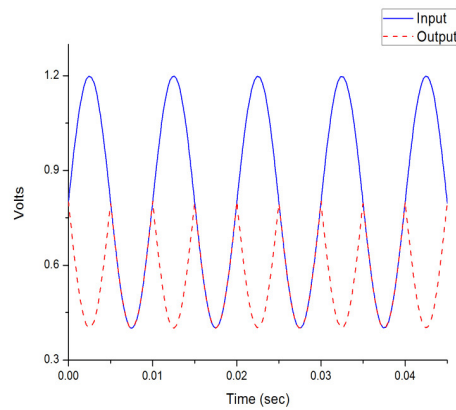


Fig. 18. Output of the rectifier for a sine input

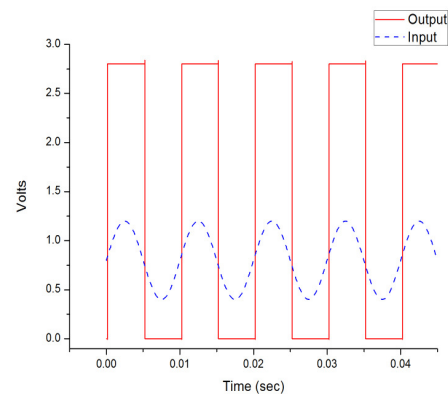


Fig. 19. Output of the comparator for a Sine input.

## VI. CONCLUSION

In this work the design of a fully integrated sensing channel for cardiac pacemakers has been presented, including a few innovative circuit techniques. A study to determine the accuracy of the transfer function has been presented, to determine the strategy to include this fully integrated but untrimmed circuit in a real medical device. The circuit has been designed in XC06, a 0.6 $\mu$ m CMOS technology with HV [1], and the samples have just arrived. Measurements will be realized in the next few months. This research was possible because the found granted by Fondo María Viñas, “PR\_FMV\_2009\_1\_3224 - Integrated circuit for cardiac sensing”.

Table V presents the overall results.

TABLE V  
OVERALL RESULTS

Specification	
Supply Voltage ( $V_{dd}$ )	2.8-8.4V
C. Consumption	740nA
Cut off Frequency (1)	67Hz
Cut off Frequency (2)	212Hz
Gain	47dB
Area	2.0mm <sup>2</sup>

Apart from the accuracy study in the transfer function of the filter, the main original contributions of this work are: the use of a novel nano power rectifier topology, and the development of a preamplifier that exploits HV transistors to avoid the use of safety capacitors obtaining a complete sensing channel without external components. Finally it should be mentioned that most of the design (most transistors operate in deep weak inversion) was carried with LT-Spice [13], a free CAD tool. BSIM foundry models were adapted without major problems.

## REFERENCES

- [1] <http://www.xfab.com/en/technology/cmos/06-um-xc06.html>
- [2] J. G. Webster (Eds.), *Design of Cardiac Pacemakers*, IEEE Press: New York, 1995. ISBN0-7803-1134-5.
- [3] F. Silveira, D. Flandre, *Low power analog CMOS for cardiac pacemakers—design and optimization in bulk and SOI technologies*, Kluwer Academic Publishers, 2004. ISBN 140207719X.
- [4] D. Prutchi, “Cardiac Pacing and Defibrillation” in *Design & Development of Medical Electronic Instrumentation*, Wiley-Interscience, 2004. ISBN 0471676233
- [5] L. Lentola, A. Mozzi, A. Neviani, and A. Baschiroto, “A 1  $\mu$ A front end for pacemaker atrial sensing channels with early sensing capability” *IEEE Transactions on Circuits and Systems -II*, vol.50, no. 8, pp. 397–403, 2003.
- [6] A. Arnaud and C. Galup-Montoro, “Consistent noise models for analysis and design of CMOS circuits”, *IEEE Transactions on Circuits and Systems -II*, vol. 51, no. 10, pp. 1909–1915, 2004.
- [7] Wong, L. S. Y., et al. (2004). “A very low power CMOS mixed signal IC for implantable pacemaker applications”, *IEEE Journal of Solid State Circuits*, vol. 39, issue 12, pp. 2446–2456.
- [8] Sacristan, J., & Oses, M. T. (2004). “Low noise amplifier for recording ENG signals in implantable systems”, *IEEE International Symposium on Circuits and Systems (ISCAS'04)*, vol. IV, pp. 33–36.
- [9] A. Arnaud, M. Miguez, J. Gak, M. Bremermann, “On the Reduction of Thermal and Flicker Noise in ENG Signal Recording Amplifiers”, *Journal Analog Integrated Circuits and Signal Processing (AICSP)*, vol. 57, no. 1-2 , pp.39-48, nov.2008.

- [10] F. Silveira, P. Jespers, *Low Power Analog CMOS for Cardiac Pacemaker: Design and Optimization in Bulk and SOI Technologies*, Springer 2010, ISBN 14419554198.
- [11] CENELEC Standard EN45502 2-1
- [12] J. Silva-Martinez and J. Salcedo-Suner, “IC voltage to current - transducers with very small transconductance”, *Journal of Analog Integrated Circuits and Signal Processing*, vol. 13, pp. 285–293, 1997.
- [13] <http://www.linear.com/designtools/software/>



**Jose Lasa** received his MSc and Graduate degree in Electronics Engineering from the Universidad Católica in 2009 and 2011 respectively. In 2009, he joined the Electrical Engineer Department, Universidad Católica, Montevideo-Uruguay. Since 2009, he has been involved in research projects in the field of CMOS analog and mixed mode and HV CMOS.



**Matías R. Miguez** received his MSc and Graduate degree in Electronics Engineerings from the Universidad Católica, Montevideo Uruguay in 2008 and 2005 respectively. He has also received a Graduate degree in Physics from the Universidad de la República, also in Montevideo, Uruguay in 2007. In 2005, he joined the Electrical Engineering Department, Universidad Católica, Montevideo-Uruguay. Since 2005 he has been involved in research projects in the field of CMOS analog design and vehicular traffic modeling. In 2010 he became a Doctoral Candidate at the Universidad Nacional del Sur, Bahía Blanca, Argentina.



**Alfredo Arnaud** received the M.S., and Ph.D. degree in electronics from the Universidad de la República, Montevideo-Uruguay, in 2000, and 2004. Since 1997, he was involved in several research and industrial projects, in the field of CMOS analog design, and optoelectronics. In 2004, he joined the Electrical Engineering Department, Universidad Católica, Montevideo-Uruguay.