A 12 nA Low Frequency Oscillator

Pablo O. Cayuela, *Member, IEEE,* Alfredo Arnaud, *Senior Member, IEEE*

***Abstract*— In this work, a 12 nA current consumption, 27 Hz (nominal) square wave oscillator is presented. The circuit includes self-bias current and voltage references, and can be powered with a wide range supply voltage from 1.6 to 5.0 V. The circuit is designed in a standard 0.6 µm MOS technology, with most of the transistors operating in weak inversion. The oscillator is intended as part of the next generation of portable or autonomous devices, powered by microbatteries or energy harvesting systems.**

***Index Terms*—Ultra Low Power Circuits, Oscillator, Weak Inversion, MOS transistor, Analog Circuit Design**

I. Introduction

IN RECENT YEARS, there has been a considerable research effort in the development of micro power integrated circuits and systems, including simple but powerful CPUs as well as sensors and even wireless data transceivers, due mainly to their application in sensor networks, autonomous data-loggers, and implantable medical devices among others. For example a 1000 mAh battery can power a pacemaker, or a small 110 mAh coin cell can power a low cost active RFID tag and they could do it in both examples for many years. The strategy to achieve such a low power consumption is the same in a wide range of embedded systems: the CPU and most digital and analog circuitry is idle and periodically turned on with an extremely low duty cycle (or turned on only by certain events). However, most systems preserve at least a current and voltage reference always turned on to bias critical analog circuits, and a low frequency digital clock or a Real Time Clock (RTC) to track time and wake up the CPU if necessary. While efficient current sources can be implemented with extremely low power consumption [1], [2], state of the art real time clocks [4], [5], [10] as well as bandgap references [6], [7], [8] consume hundreds nA from the power supply. Nevertheless, hundreds of nW may result in a too much high power consumption for the next generation of devices, powered by microbatteries or energy harvesting sub-systems. RTCs are accurate crystal oscillators and bandgaps are accurate temperature compensated voltage references, thus a power consumption reduction can be achieved with a careful design and relaxed precision constraints. In this work, an autonomous clock circuit is presented, including a voltage and current source references. The overall circuit current consumption is only 12 nA from a power supply ranging from 1.6 to 5.0 V. The proposed circuits use most of the MOS transistors working in the weak inversion (WI) operation region, and design space exploration was done using the ACM transistor model [3].

In Section II, a 500 pA current and a 365 mV voltage references are presented. The circuit is based on the current source proposed in [1] with only 500 pA bias current on each branch. A relatively stable 365 mV voltage reference is derived from an internal node in the current source. In Section III, a Nanopower Oscillator is presented. The oscillator combines the previously developed references, with two nested comparators to periodically charge-discharge an integrated capacitor. Simulation results are presented in Section II, and Section III, the circuit is currently being fabricated in a 0.6 µm CMOS technology. The proposed current, voltage, and time references, can be employed to further reduce power consumption in modern, autonomous systems on a chip.

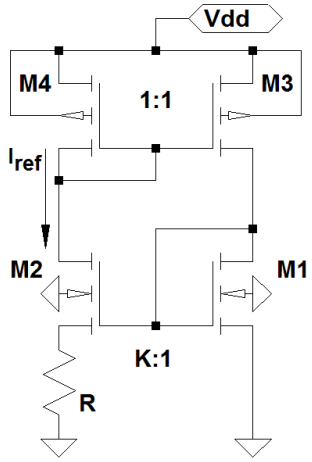

Fig. 1. Classic Self-Bias Current Source (SBCS).

II. Current & Voltage Reference

The circuit in Fig. 1 is a classic Self-Bias Current Source (SBCS) [6], with an output current:

$$I_{REF} = \phi_t \frac{\ln(K)}{R} \tag{1}$$

In a practical design K >> 1 and the voltage drop V_R across the resistor is in tens of mV [1], [2]. For a target current

This work was supported in part by Agencia Nacional de Promoción Científica y Tecnológica, Argentina; Universidad Católica de Córdoba and Universidad Católica del Uruguay.

P. O. Cayuela is with the Universidad Católica de Córdoba, Argentina (corresponding author; e-mail: cayuela@ieee.org).

A. Arnaud, is with the Electrical Engineering Department (DIE), Universidad Católica del Uruguay, Montevideo, Uruguay (e-mail: aarnaud@ucu.edu.uy).

reference set at 500 pA, a 120 MΩ resistor is required for the thermal voltage ϕ_t = 26 mV and K=10, which cannot be integrated in a reasonable circuit area.

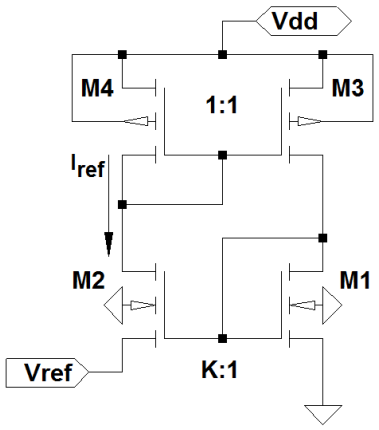

Fig. 2. SBCS with a Voltage Reference instead of a large resistor.

A possible solution to avoid the use of a large resistor is shown in Fig. 2. This current reference uses a voltage reference $V_{ref} = f(I_{ref})$ to substitute R in the source of M_2. To complete the circuit it is necessary to generate an adequate and efficient circuit block to generate V_{ref}. I_{ref} can be replicated as many times as necessary just adding extra output transistors to M_3-M_4 mirror.

A. SCM Voltage Reference

A Self-Cascode MOSFET (SCM) is proposed in [1], [2] for V_{ref}, also called elementary PTAT voltage source [7]; the circuit is shown in Fig. 3.

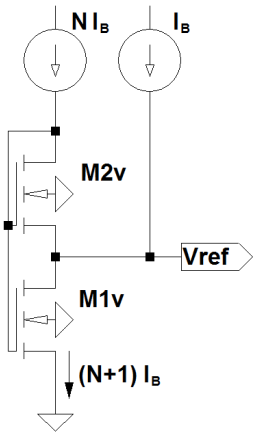

Fig. 3. SCM (Self-Cascode MOSFET) Voltage Reference completes the circuit in Fig. 2.

In this work, a 500 pA current reference was designed following the guidelines in [1]. A nominal V_{ref} = 65 mV at the nominal I_{ref} = 500 pA was selected. The analysis of the circuit of Fig. 3 in [1] and [7] leads to the following estimation for the voltage reference:

$$V_{ref} = \phi_t \left[P - Q + \ln\left(\frac{P-1}{Q-1} \right) \right] \tag{2a}$$

where:

$$P = \sqrt{1 + M\ N\ I_B / I_{S2v}} \tag{2b}$$

$$Q = \sqrt{1 + N\ I_B / I_{S2v}} \tag{2c}$$

$$M = 1 + \left(S_{2v} / S_{1v} \right) / \left[(N+1)/N \right] \tag{2d}$$

$$I_{S2v} = \mu_n C'_{ox}\, n \phi_t^{\,2} S_{2v} / 2 \tag{2e}$$

and $S_{1v,\,2v}$=(W/L) $_{1v,\,2v}$ respectively.

The oscillator in the next section requires a voltage reference as stable as possible, but V_{ref} = 65 mV results too low.

To derive a larger voltage V_{ref2} without introducing extra power consumption in the circuit, M_{2v} is split into two parts: M_{2vs} and M_{2vi}. The complete resulting circuit is shown in Fig. 4, already combining SBCS with modified SCM. A second voltage reference V_{ref2} = 365 mV (nominal) is generated.

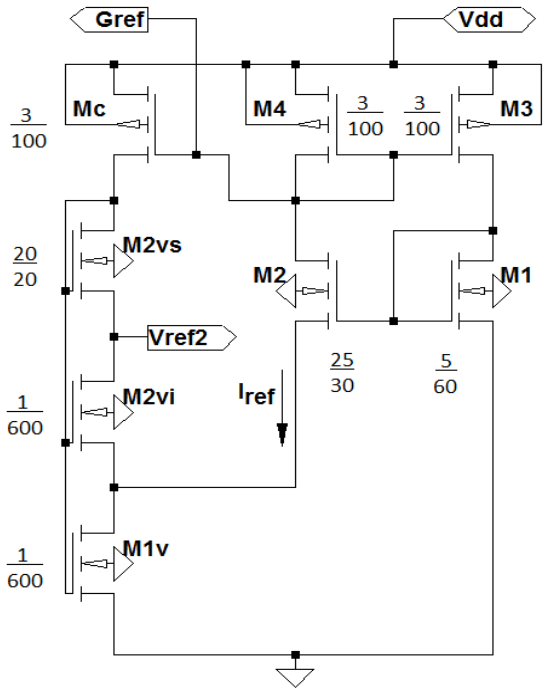

Fig. 4. Current-Voltage Reference (CVR) as an SBCS-SCM combination with the second voltage reference output V_{ref2}. Transistor sizes are shown as (W/L). Output G_{ref} is for the gate of current-replicating extra transistors.

Also the series association of transistors (Fig. 5) must be taken into account for the analysis of M_{1v}-M_{2vi} as an M_S-M_D associated transistor operating only in triode region (3a,b) and M_{2vi}-M_{2vs} as an M_S-M_D associated transistor operating in triode and saturation region (4a,b) as suggested by [9].

$$\left(\frac{W}{L} \right)_{eq} = \frac{\left(\frac{W}{L} \right)_D \left(\frac{W}{L} \right)_S}{\left(\frac{W}{L} \right)_D + \left(\frac{W}{L} \right)_S} \tag{3a}$$

$$I_D = \left(\frac{W}{L} \right)_{eq} \left[g(V_{GB}, V_{SB}) - g(V_{GB}, V_{DB}) \right] \tag{3b}$$

$$m = \frac{(W/L)_D}{(W/L)_S} \tag{4a}$$

$$I_{Dsat} = \frac{m}{m+1}\left(\frac{W}{L}\right)_S g(V_{GB}, V_{SB}) \tag{4b}$$

where: $g(V_{GB}, V_{XB})$ with X:{S, D}, is the MOS dc behavior function; W and L are channel width and length respectively.

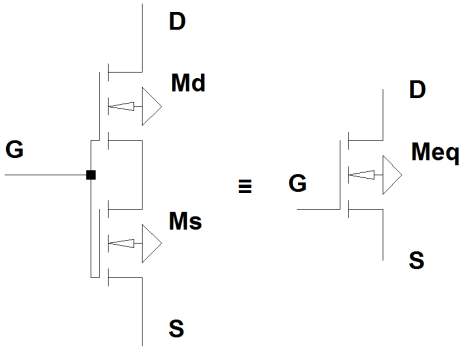

Fig. 5. Series association of MOS transistors being equivalent to one M_{eq} according to (3a,b) for only-triode operation pair, and (4a,b) for triode-saturation operation pair.

Fig. 6 shows simulated current-voltage reference (CVR) output I_{ref} against supply voltage for Worst Case Power (WP), Typical Mean (TM) and Worst Case Speed (WS) transistor models.

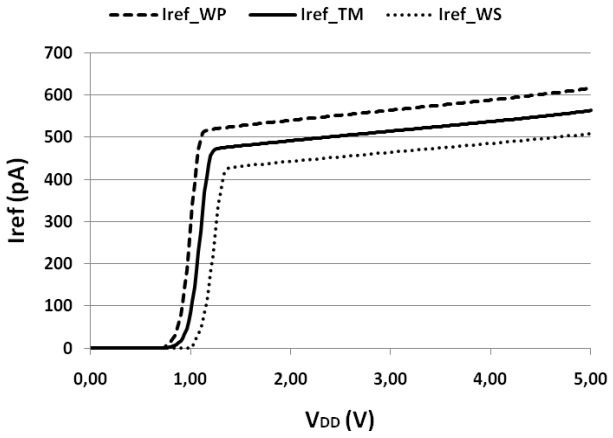

Fig. 6. CVR Current Reference I_{ref} versus Supply Voltage at WP, TM, WS transistor models.

It should be noted that while the model in [3] was used for design equations, simulations use BSIM3v3 models provided by the foundry. It shows also that I_{ref} has an approximately 26 pA/V slope for $V_{DD} > 1.5$ V for all the cases.

Fig. 7 shows simulated CVR current reference output I_{ref} against temperature for TM transistor model, where I_{ref} has an approximately 0.6 pA/ºC slope.

Fig. 8 shows simulated CVR second voltage reference output against supply voltage for WP, TM and WS transistor models, where V_{ref2} has an approximately 2.3 mV/V slope for $V_{DD} > 1.5$ V.

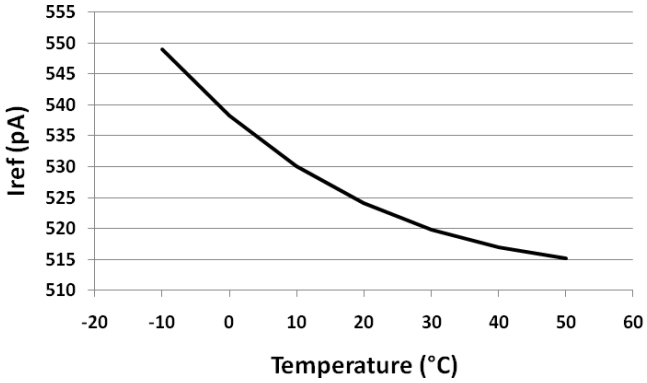

Fig. 7. CVR Current Reference versus Temperature for Typical Mean transistor model at $V_{DD} = 3.3$ V.

Fig. 9 shows simulated CVR second voltage reference output V_{ref2} against temperature for TM transistor model, where V_{ref2} has an approximately 0.65 mV/ºC slope.

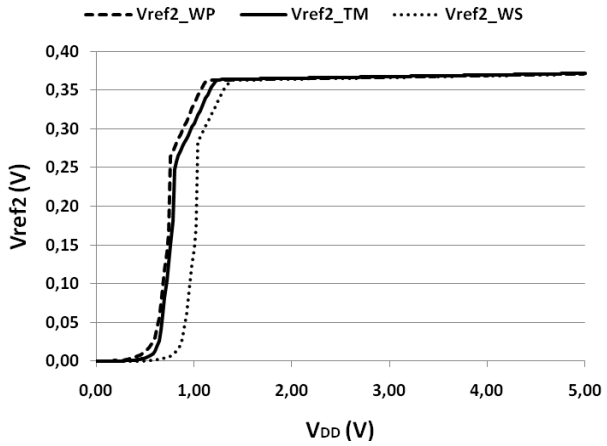

Fig. 8. CVR Voltage Reference V_{ref2} versus Supply Voltage at WP, TM, WS transistor models.

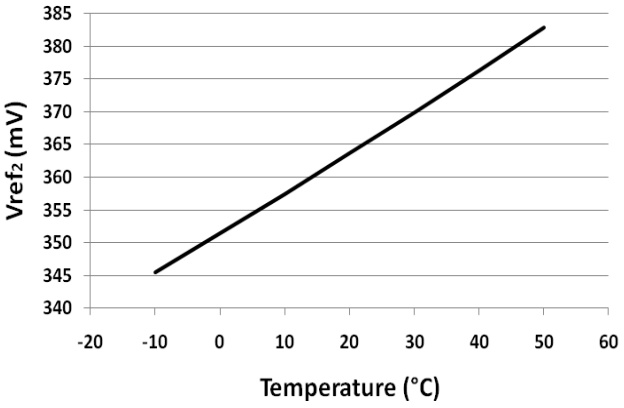

Fig. 9. CVR Voltage Reference V_{ref2} versus Temperature for Typical Mean transistor model at $V_{DD} = 3.3$ V.

III. NANOPOWER OSCILLATOR

A. Nanopower Oscillator circuit

The proposed oscillator in Fig. 10 is based on two nested charge-discharge capacitor stages. Both 20 pF and 5 pF capacitors are charged with a constant 500 pA current. Both current and voltage reference values determine the charge-discharge time in the circuit.

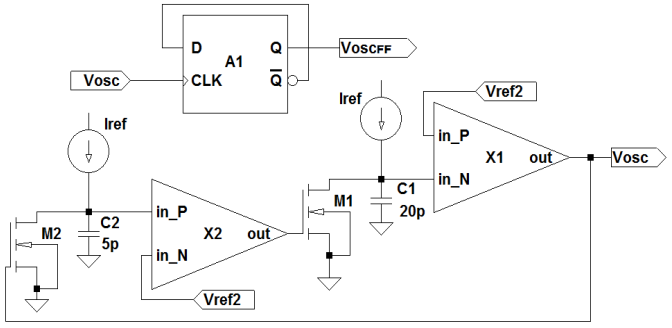

Fig. 10. Nested charge-discharge capacitor stages oscillator and frequency divider.

For experimental purposes the frequency was set around 27 Hz according to (5):

$$\frac{T}{2} = \sum_{i=1;2} C_i \frac{V_{ref\,2}}{I_{ref}} \tag{5}$$

Fig. 11 shows how the oscillator operates. When M_1 is off, V_{osc} is on, C_1 is linearly charged by I_{ref} until it surpasses V_{ref2}. This turns X_1 output off (V_{osc} off), then M_2 turns off, and starts charging C_2 also until it surpasses V_{ref2} that turns the X_2 output and M_1 on, discharging C1, turning X_1 output on (V_{osc} on), starting the cycle again.

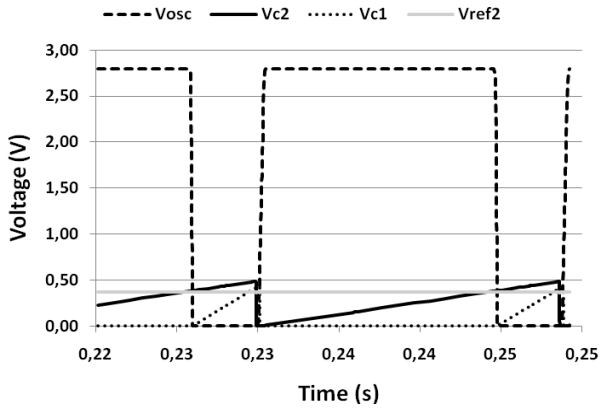

Fig. 11. Charge-discharge cycle of capacitors and oscillator output, where dot line is V_{C1}, C_1 charge voltage level; solid line is V_{C2}, C_2 charge voltage level; gray line is V_{ref2}; and dash line is V_{osc}, output of comparator X_1.

Both comparators are PMOS-inputs uncompensated Miller stages, (Fig. 12).

B. Signal Conditioning circuit

The oscillator output is squared using an output flip-flop (Fig. 10) in order to avoid large transition time between logic 1 and 0 levels and it is used as a frequency divider. Limiting resistors were included in series with the supply voltage that powers the flip-flop to reduce power consumption due to large current spikes in digital transitions.

The complete circuit layout is shown in Fig. 16 including CVR, oscillator, and the flip-flop on the right. It covers an approximate area of 280 µm by 250 µm.

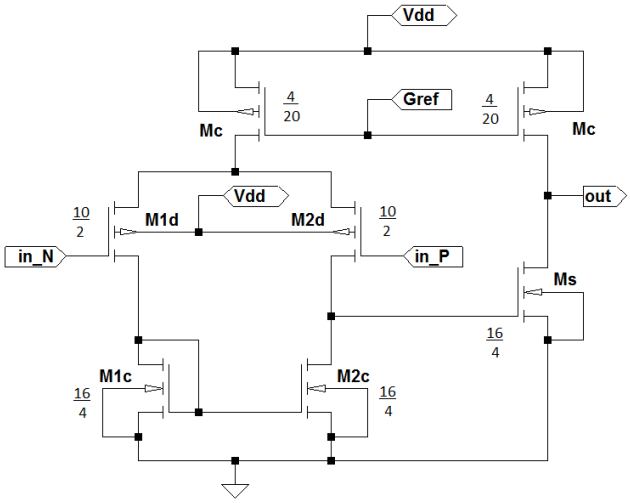

Fig. 12. PMOS-inputs uncompensated Miller stages comparator.

C. Simulation Results

In Fig. 13, Fig. 14, and Fig. 15, simulation results of the complete oscillator circuit are presented.

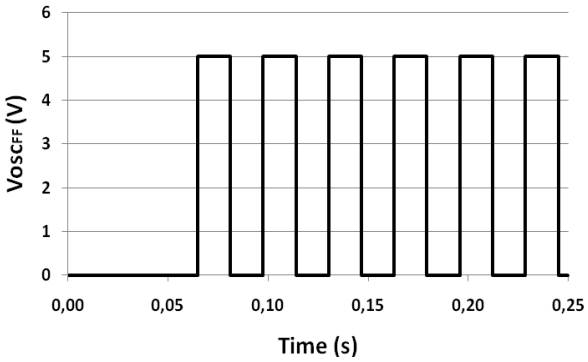

Fig. 13. Oscillator output after signal conditioning by a flip-flop for Typical Mean transistor model at V_{DD} = 5 V.

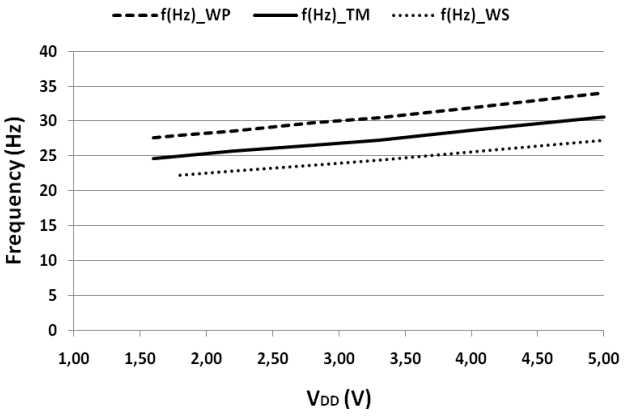

Fig. 14. Frequency versus Supply Voltage at WP, TM, WS transistor models.

Fig. 14 shows that frequency has a dependence on supply voltage of around 1.7 Hz/V.

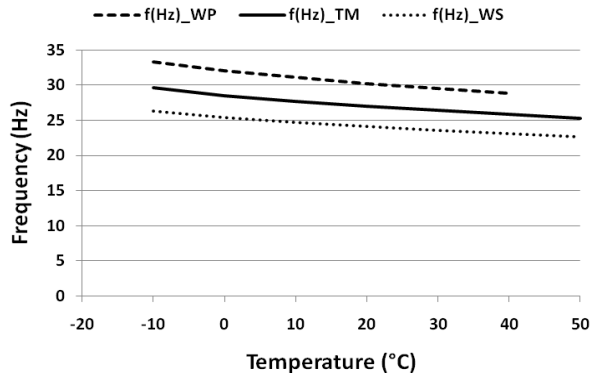

Fig. 15. Frequency versus Temperature at WP, TM, WS transistor models.

Fig. 15 shows the variations of the oscillator frequency with temperature, with an approximately 0.7 Hz/ºC slope.

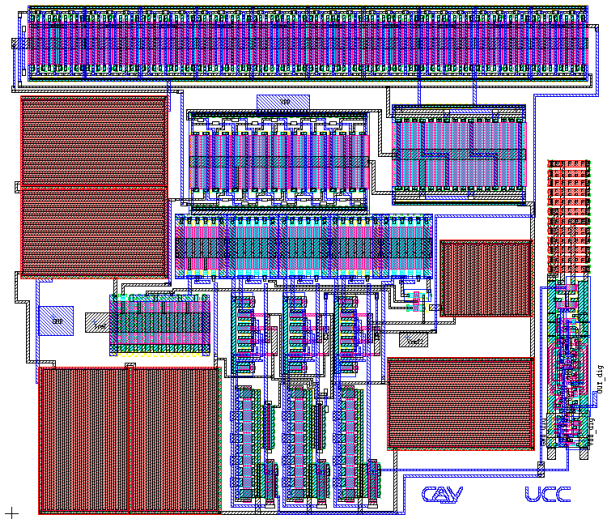

Fig. 16. Layout of the Nanopower Oscillator.

IV. Conclusion

An ultra-low power circuit including a current and a voltage reference, and 27 Hz square wave oscillator was presented. The total current consumption is only 12 nA. The circuit shows a stable and adequate performance for a supply voltage V_{DD} ranging from 1.6 to 5 V.

The current reference is based in the topology of reference [1] and simulated results are similar to those of previously reported circuits using the same topology. The circuit was slightly modified to derive a 365 mV voltage reference that resulted very stable with transistor parameters variations, supply voltage variations, and temperature.

A robust bistable oscillator was developed using two comparator and the designed references, to control the charge/discharge of two integrating capacitors. Nominal oscillator frequency is 27 Hz.

While the presented oscillator frequency depends on temperature, V_{DD}, and transistor parameters, it can be utilized as a time reference for different embedded systems that are not precision-constrained. Furthermore, future work on this circuit includes to compensate specially temperature dependence of the oscillator frequency.

The proposed current-voltage-time reference set, may result a valuable circuit block for the next generation of ultra low-power, autonomous systems on a chip powered either by microbatteries or energy harvesting sub-systems.

Acknowledgment

The authors are grateful for the helpful advice of Matías Míguez and Joel Gak from the Universidad Católica del Uruguay.

References

[1] E. M. Camacho-Galeano, C. Galup-Montoro, M. C. Schneider, "A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology", *IEEE Transactions on Circuits and Systems - II: Express Briefs* , vol. 52, no. 2, pp. 61-65, February 2005.

[2] E. M. Camacho-Galeano, J. Q. Moreira, M. D. Pereira, A. J. Cardoso, M. C. Schneider and C. Galup-Montoro, "Temperature Performance of Sub-1V Ultra-Low Power Current Sources", *International Symposium on Circuits and Systems (ISCAS 2008)*, Seattle, WA, USA, May 2008, pp. 2230-2233.

[3] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design", *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510-1519, Oct. 1998.

[4] D. Ruffieux, F. Krummenacher, A. Pezous, and G. Spinola-Durante, "Silicon Resonator Based 3.2uW Real Time Clock With 10 ppm Frequency Accuracy", *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 224-234, Jan. 2010.

[5] RX-8581 – RTC module datasheet. Available at http://www.eea.epson.com/portal/pls/portal/docs/1/1413527.PDF

[6] E. Vittoz and J. Fellrath, "CMOS analog circuits based on weak inversion operation", *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 224-231, June 1977.

[7] E. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference", *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 573-577, June 1979.

[8] L. Toledo, W. Lancioni, P. Petrashin, C. Dualibe, and C. Vazquez, "A new CMOS voltage reference scheme based on Vth difference principle", *International Symposium on Circuits and Systems (ISCAS 2007)*, New Orleans, LA, USA, May 2007, pp. 3840-3843.

[9] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications", *IEEE J. Solid-State Circuits*, vol. 29, pp. 1094-1101, Sep. 1994.

[10] PCF8523 CMOS Real Time Clock - calendar datasheet. Available at http://www.nxp.com/documents/data_sheet/PCF8523.pdf

Pablo O. Cayuela (S'97–M'02) is a doctoral student at the Universidad Católica de Córdoba. He received a degree in Information Systems Engineering in 2002 and another degree in Electrical Engineering in 2009, both from the Universidad Tecnológica Nacional, Facultad Regional Córdoba, Argentina. His main interests are on Analog Microelectronics, Programmable Logic and Computer Engineering.

Alfredo Arnaud is a Full time professor G.4, at the Universidad Católica del Uruguay, Researcher Level 1 of the SNI. He received the M.S. and Ph.D. degrees in electronics from the Universidad de la República, Montevideo, Uruguay, in 2000, and 2004, respectively. Since 1997, he has been involved in several research and industrial projects, in the field of CMOS analog design, and optoelectronics. In 2004, he joined the Electrical Engineering Department, Universidad Católica del Uruguay, Montevideo, Uruguay.