Integrated filter-amplifier for ENG signals

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***Abstract*— Due to the extremely low amplitude of the input signals, the design of electro-neurgo-graph (ENG) amplifiers normally involves special care for flicker and thermal noise reduction. The task becomes really challenging in the case of implantable devices, because power consumption is restricted to few tens μW. In this paper a ultra-low-noise, low-power amplifier is presented. Thermal noise is reduced by using an energy-efficient DC-DC downconverter and low voltage design techniques. Measured input referred noise in this case was 5,5 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at only 380μW power consumption. The circuit was fabricated in a 1,5 micron technology.**

***Index Terms*— Analog design, low-power, ultra-low-noise.**

I. Introduction

Most implantable neuroprostheses are stimulators of the nervous system. The main improvement that, in both the industry and research laboratories is nowadays being investigated, is to enable neural signals (electro-neuro-graph or ENG) to be used as inputs in the control feedback of neuroprosthetic systems [1]. ENG signals are registered from electrodes placed around nerves and may be used instead of a wide variety of artificial sensors in implants. Microelectronics technology is steadily contributing to develop this group of medical devices, and in recent years there has been a considerable research effort in the development of integrated amplifiers for ENG [1-4]. The main challenges are: the extremely low noise required for amplifying μV range signals, and the ultra-low power consumption specified for implantable electronics since they are normally battery powered. Power consumption is the main restriction for the development of such amplifiers. On the other hand, circuits must be extremely reliable because they may be life supporting devices for the patient. ENG signals range from a few Hz to a few kHz; an amplifier requires an input referred noise of a few $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, a high gain, and CMRR [1,4]. The main sources of electrical noise in the frequency span of biological signals –apart from coupling noise- are thermal and flicker noise of the circuit elements at the input stage. In this paper the focus will be in the former. For a MOS transistor, thermal noise current model is in general not questioned, its PSD being (the PSD of the noise current in parallel with the transistor) [5]:

$$S_{i\_th}(f) = n\gamma k_B T g_m \qquad (1)$$

where k_B is the Boltzmann's constant, T the absolute temperature, g_m is the transistor's transconductance, $n \approx 1$ is the slope factor, γ = 2, 8/3 in strong and weak inversion respectively [5]. Integrating (1), in the frequency band of interest in a continuous time amplifier, input referred thermal noise voltage shows a relation with power consumption [5]:

$$v_{nrms} \approx \frac{\mathrm{A}}{g_m} = \frac{\mathrm{A}}{g_m/I_D}\cdot I_D \qquad (2)$$

In (2), v_{nrms} is the input referred rms noise voltage, g_m is the transconductance of the input pair. A, ia a constant depending on frequency band, technology parameters, and the number of transistors introducing noise at the input branch. As pointed in [4,5] low input thermal noise requires a large bias current for a large g_m . Equation (2) shows that to minimize thermal noise with a fixed current budget, input transistors should be biased in weak inversion (WI) to maximize the ratio g_m/I_D . At WI $g_m/I_D \approx 25$; further noise reduction necessarily require for the designer an increase of the bias current and thus power consumption.

II. A Figure of merit

Regarding thermal noise, it appears useful to define a figure of merit that allows the comparison of different amplifiers. It should be noted that if all the transistors in two low noise circuits of similar topology, are assumed to operate in the same inversion level (ideally WI), and the circuits have the same supply voltage, the input referred noise voltage is related to power consumption in both circuits (1),(2):

$$\frac{v_{n1}(f)}{v_{n2}(f)} = \sqrt{\frac{P_2}{P_1}} \qquad (3)$$

Where $v_{nx}(f) = \sqrt{PSD}$ [$\mathrm{nV}/\sqrt{\mathrm{Hz}}$] is the noise voltage ($v_n(f) = v_n$ in the case of thermal noise) and P_x is the power consumption of each circuit. Equation (3) shows that to reduce the noise voltage by 5, power consumption has to be increased

by 25, and so on. Observing (3), it is possible to define the following figure of merit:

$$\zeta = v_n \cdot \sqrt{P} \tag{4}$$

A lower ζ indicates a more efficient low-noise circuit for the task of amplifying signals at the minimum power consumption.

III. The Amplifier

The amplifier in this work consists of three blocks as shown in Fig.1(a). The DC-DC down converter of Fig1(b), is used to reduce power supply form 5V to 1,8V (efficiency close to 100%). In this way it is possible to keep the same bias current of an amplifier (and thus thermal noise according to (2)) but reducing three times the power consumption of the battery. A preamplifier (Fig 1(c)) powered by the DC-DC converter amplifies the signal that is then band-pass filtered. The preamplifier's topology is similar to the one in [4] but transistors sizes are optimized to work with low supply voltage. The band-pass is a G_m-C filter, as shown in Fig.1(d).

The specifications of the circuit are: low-noise $5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (input referred), high gain 1000 or more, high CMRR 90db, and cut off frequencies at 100 and 5KHz.

IV. Preamplifier

$M_{pp1(2),np1(2)}$ in Fig.1(c) are bias current sources, while transconductance gain is provided by the differential pair $M_{pd1,pd2}$. *R* makes current to voltage conversion, and *C* provides a high pass characteristic. V_{ref} fixes the common mode output. The resulting transfer function is:

$$H(f) = \frac{Rg_{mpd} \cdot j2\pi f}{j2\pi f + \frac{ng_{mpd}}{2C}} \tag{5}$$

where g_{mpd}=2,2x10^{-3}S is the differential pair M_{pd} transconductance, *R*=50kΩ and *C*=2,2μF. Theoretical pass-band gain is G_{DC}=110 with low-pass cut-off frequency at f_c=100Hz.

As described in [6], transistor sizing is optimized by examining the noise contribution at the input, of each pair of transistors in Fig.1(c). The result is summarized in table I.

According to an existing current budget I_{Bias} (Fig.1(c)) is 1μA so the bias current of each transistor is 100μA. In Fig.2 the simulated and measured transfer function of the preamplifier is shown. The measured DC gain is much less than expected in (5) because the channel resistance r_{ds} of the NMOS current source is close to *R* value. Some of the signal current flows through the NMOS instead of *R*, lowering the gain form 100 to 60 approximately. A list of measured and simulated characteristics is presented in table II. The results show a input noise similar to the amplifier in [4], but the use of the DC-DC substantially reduce power consumption. It is still necessary to investigate the origin of the still poor measured CMRR. Using ζ as defined in (4), the amplifier here presented has an figure of merit $\zeta = 2.1\ \mathrm{nV}\cdot\sqrt{\mathrm{mW}}/\sqrt{\mathrm{Hz}}$ (preamplifier is connected to the DC-DC converter).

V. Band Pass Filter

A G_m-C band-pass filter (BPF) shown in Fig1.(d), is used to eliminate noise out of the frequency spectrum of the ENG signals. This BPF has a gain G_{BP} = 33 and cut-off frequencies at 100 and 5KHz.The transfer function of the filter is :

$$H(j\omega) = \frac{Q\omega_o}{k}\frac{j\omega\omega_o/Q}{\omega_o^2 + j\omega\omega_o/Q - \omega^2} \tag{6}$$

where, $\omega_o^2 = A_o k\omega_L = \frac{G_{m1}G_{m3}}{C_1C_2}$, $Q = \sqrt{\frac{A_o k}{\omega_L}} = \sqrt{\frac{G_{m1}G_{m3}C_2}{G_{m2}^2 C_1}}$, and $A_o = G_{BP} = \frac{G_{m1}}{G_{m2}}$ .Solving (6),

$$f_{p1} = -j2\pi\omega_o\left[\frac{1}{2Q} - \sqrt{\frac{1}{4Q^2}-1}\right],\ f_{p2} = -j2\pi\omega_o\left[\frac{1}{2Q} + \sqrt{\frac{1}{4Q^2}-1}\right] \tag{7}$$

where ω_{p1} is the low frequency pole, and ω_{p2} is the high frequency pole. For f_{p1}=100Hz, f_{p2}=4960Hz, G_{BP}=33, we selected Gm_1=20μS, Gm_2=682,8nS, Gm_3=2,2nS, C_1=78pF and C_2=22pF. C_1 and C_2 are ploy1-poly2 capacitors. $G_{m1,2,3}$ were implemented as a standard symmetrical OTAs using series-parallel association technique [7]. For G_{m1} the current copy factor from the differential pair to the output is 1:1, while for G_{m2} is 16:1, and for G_{m3} 100:1. $G_{m1,2}$ input transistors are biased in SI, and in Gm_3 in WI. In table III, a summary of transistors size and bias current is presented for the designed G_m's .

To calculate noise, only G_{m1} will be considered, because it is the input transconductor. Using (1) to estimate each transistor's noise in the OTA, the equivalent input noise of G_{m1} is $v_{nG_m} = 33\mu V_{rms}$ .The design criterion is that the preamplifier's output noise must be greater or equal to the G_m-C filter's input noise. In effect both are very similar, thus the total input noise of the circuit is:

$$v_{n\_Tot} = \sqrt{v_{nG_m}^2 + v_{n\_out\_pream}^2} = 46{,}25\mu V_{rms} \tag{8}$$

In Fig 3, the simulated transfer function is shown from which f_{p1}=120Hz, f_{p2}=5160Hz, G_{BP}=33.

VI. DC-DC down converter

The DC-DC down converter used to power up the preamplifier is shown in Fig1(b) (see also section IV). The use of the DC-DC converter, enables to keep the same noise condition as [4], but consuming 1/3 of the power from the battery.

When CLK is at low level (0V) transistors M_1 to M_3, charge C_{fly1} to C_{fly3} at $\frac{V_{Bat}}{3}$. When CLK is at high level (V_{Bat}) transistors M_4 to M_8 put C_{fly1} to C_{fly3} in parallel with C_{sto} . Charge is transferred and C_{sto} voltage is kept approximately at $\frac{V_{Bat}}{3}$. C_{sto} is a tank capacitor to eliminate ripple at the output, providing a constant voltage to the load.

To determinate transistor sizes and capacitor values, we

must consider the DC-DC converter in two stages: charge and discharge (Fig4(a,b)). Using a 10% criteria,

$$e^{\frac{-T/2}{RC_{fly}}} < 10\% \qquad (9)$$

Where R is the total transistor on-state channel resistance and $T=1/f_{clk}$, choosing C_{fly}=100nF, f_{clk}=30KHz (outside Gm-C filter band) and solving (9), $R < 72\Omega$.

C_{sto} and C_{fly} are external, their values were chosen because their physical sizes are small enough to be used in implantable devices and they present very low leakage currents.

In table II simulated and measured results of Vcc and efficiency are shown, for nominal load of 200µA and f_{clk}=30KHz. In Fig.5 to Fig.6 different simulated and measured results are shown

VII. FIGURES AND TABLES

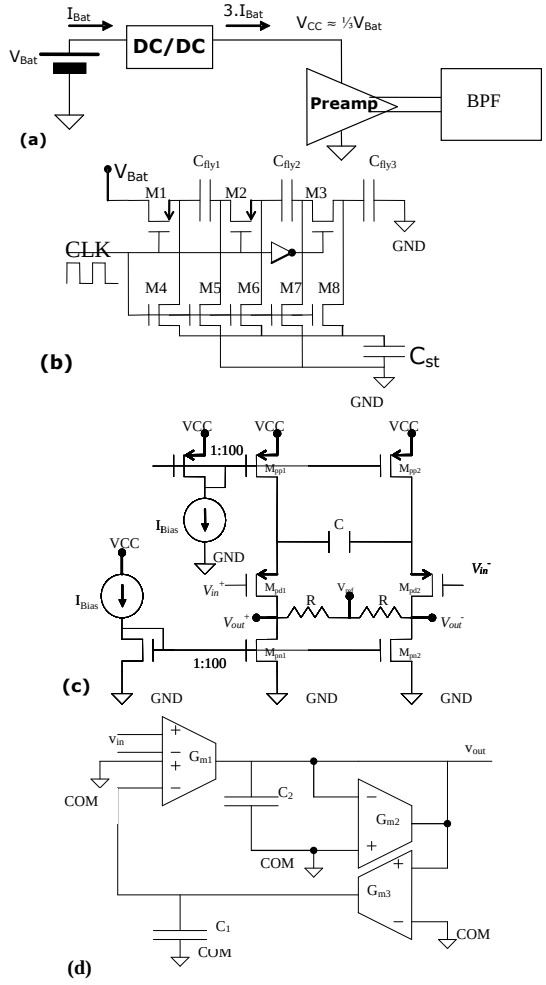

Figure 1. a) Block diagram of the amplifier. b) DC-DC converter , V_{Bat}=5,4V, V_{CC}=1,8V, C_{fly*}=100nF, C_{sto}=10µF and f_{CLK}=30kHz. c) Preamplifier, I_{Bias}=1µA, C=2,2µF and R=50kΩ. d) G_m-C band pass filter , G_{BP}=33, Gm_1=20µS, Gm_1=682,8nS, Gm_1=2,2nS, C_1=78pF and C_2=22pF.

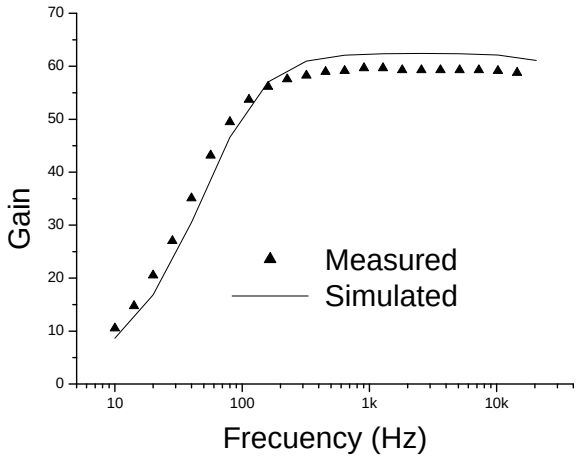

Figure 2. Preamplifier transfer function, simulated (line) and measured (triangles).

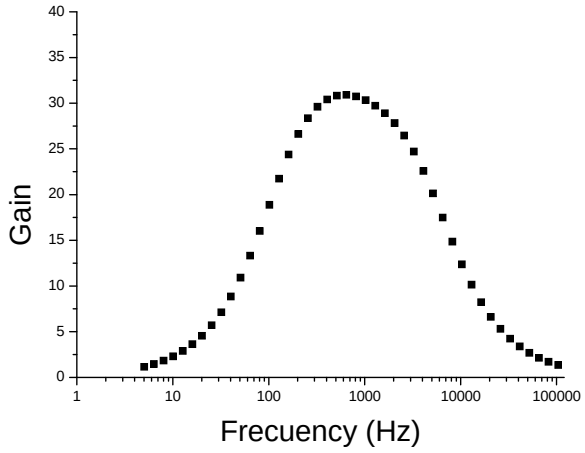

Figure3. Band pass filter transfer function, simulated.

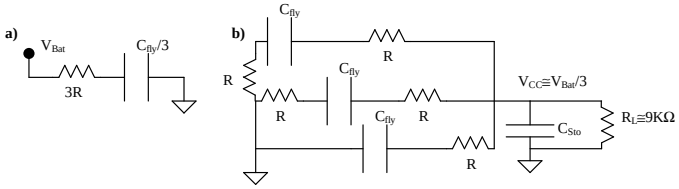

Figure 4. DC-DC down converter equivalent circuits, a) charge, b) discharge.

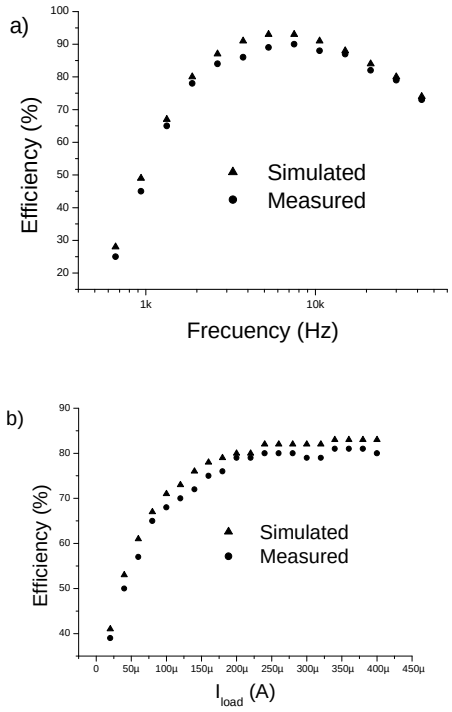

Figure 5. a) Efficiency vs f_{clk} for nominal load 200uA and V_{Bat}=5,4V, simulated (triangle), measured (circle). b) Efficiency vs load for f_{clk}=30kHz and V_{Bat}=5,4V, , simulated (triangle), measured (circle)

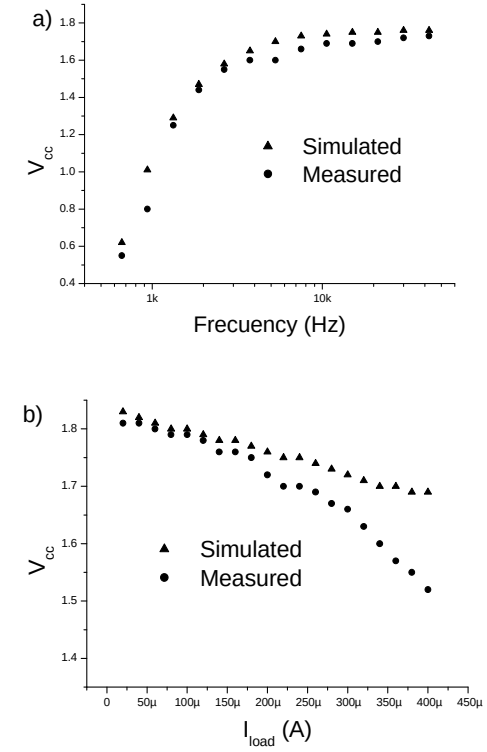

Figure 6. a) V_{cc} vs f_{clk} for nominal load 200uA and V_{Bat}=5,4V, simulated (triangle), measured (circle). b) V_{cc} vs load for f_{clk}=30kHz and V_{Bat}=5,4V, , simulated (triangle), measured (circle)

NMOS (µm)	PMOS (µm)	Pair (µm)
W=14826 L=4,5	W=3760 L=4,5	W=14826 L=4,5

Table I. Preamplifier transistor sizes

	Simulated	Measured
Cut-off frequency	82 Hz	60 Hz
Preamplifier Gain	62	60
CMRR	-----	58 dB
Input noise (100-5kHz)	0.5µ V_{rms}	0.54µ V_{rms}
Power consumption (*)	-----	380µW
DC-DC output	1.76 V	1.72 V
Efficiency DC-DC	85 %	80 %

Table II: Simulated and measured results.
(*) DC-DC converter included

GM	I_{Bias}	W/L
1	4µA	96µm/4,5µm
2	13µA	22µm/20µm
3	22nA	9µm/82,5µm

Table III. Gm's polarization and differential pairs sizes.

VIII. CONCLUSIONS

A preamplifier was design and implemented with the following measured characteristics: Supply voltage 1,8V, power consumption 380µW, gain 60, pole 60Hz, input referred noise 5,5 nV/√Hz and CMRR 58 dB.

A DC-DC down converter was design and implemented with the following measured characteristics: Input voltage 5,4V, output voltage 1,72V, load 200µA, f_{clk} 30kHz and efficiency 80%.

A G_m-C band pass filter, was design and implemented with the following simulated characteristics: Supply voltage 5V, gain 33, lower pole 120Hz and higher pole 5160Hz.

The three blocks together form a Integrated filter-amplifier for ENG signals, that improves in the sense of thermal noise vs. energy trade-off the results of previous works.

The preamplifier has a figure of merit $\zeta = 2.1\ \mathrm{nV}\cdot\sqrt{\mathrm{mW}}/\sqrt{\mathrm{Hz}}$, which is 2 ½ times more efficient than [4]. It should be pointed that the improvement is achieved just by designing for low voltage and adding a DC-DC converter, all in a rather large 1,5µm technology.

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