DIGITAL TRIMMING FOR LOW OFFSET COMPARATOR

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Abstract –In this work a digital trimming technique to achieve a low offset (below 100µV) low power consumption (0.33µW@3.3V) with an area of 1mm^2 integrated comparator is presented.

I. Introduction

This project aims to design, simulate, fabricate and measure an integrated comparator with digital trimming based control to minimize offset. Its purpose is to be used in a channel for sensing cardiac activity, as part of a larger implantable medical device.

II. Digital trimming based control.

Offset in integrated comparators is caused mainly due to transistor mismatch. This occurs because components that are exactly equal during layout creation and simulation are in fact physically different because of fabrication constraints. Regarding implantable devices, offset is one of the main design challenges due to the low amplitude of biological signals [1]

The digital trimming technique aims to reduce offset through the following method: if the comparator's differential pair is designed in such a way that one of the transistors is broken into several interconnected small transistors, each with its own gate drain and source, then each of those transistors is accessible to be turned on or off.

The control block is designed to turn each piece of transistor on or off. It accomplishes this goal by offering several outputs that are either connected to ground or to a selectable node in the circuit. The selectable node can be, for example, the drain of the transistors. In this case each transistor can be interpreted as ON if the drain connected to other drains or OFF if the drain is connected to ground. (See Fig. 1)

Normal operation is as follows: when first turning on the circuit, all of the accessible transistor pieces are turned off and the differential input is short-circuited. Then one transistor is turned on for each rising flank in the clock of the circuit. A feedback loop ensures that the clock is disabled for the control circuit as soon as the objective offset is reached (mismatch is minimized, see Fig 5). This is determined by the output of the comparator; as soon as there is a change in its output, the control circuit is disabled and its state is memorized. Fig. 4 shows simulation results for 50 control outputs.

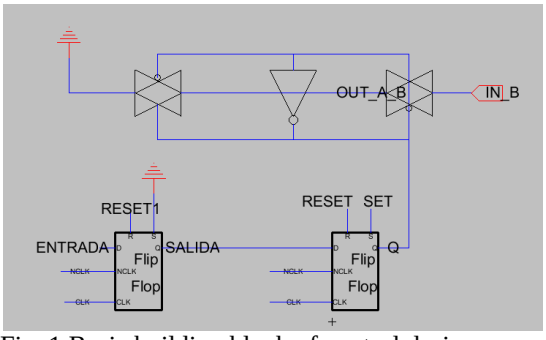

Fig. 1 Basic building block of control design

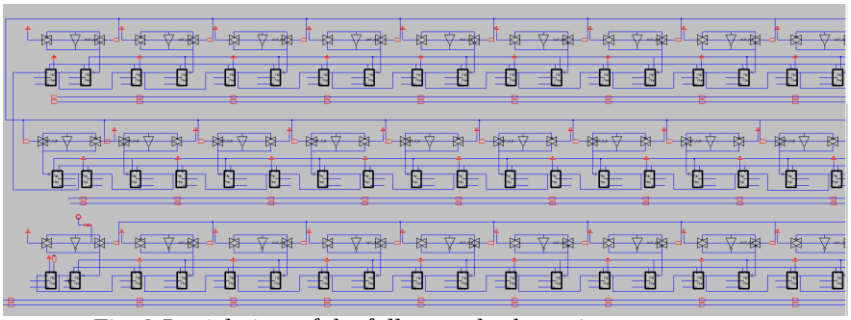

Fig. 2 Partial view of the full control schematic

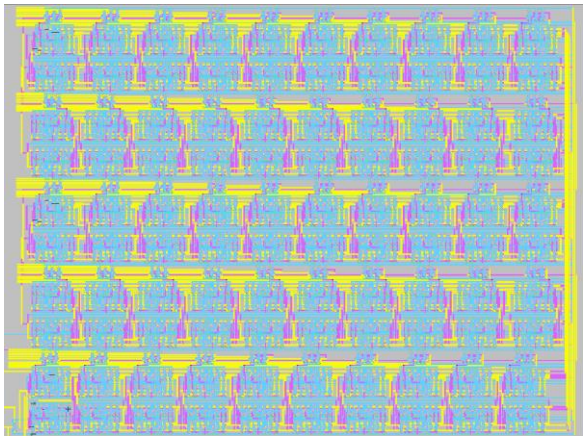

Fig. 3 Layout of the control system

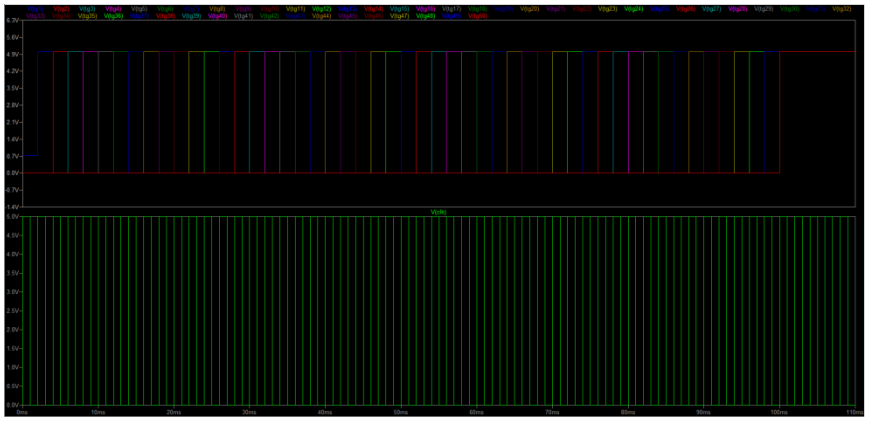

Fig. 4 Simulation results for 50 control outputs.

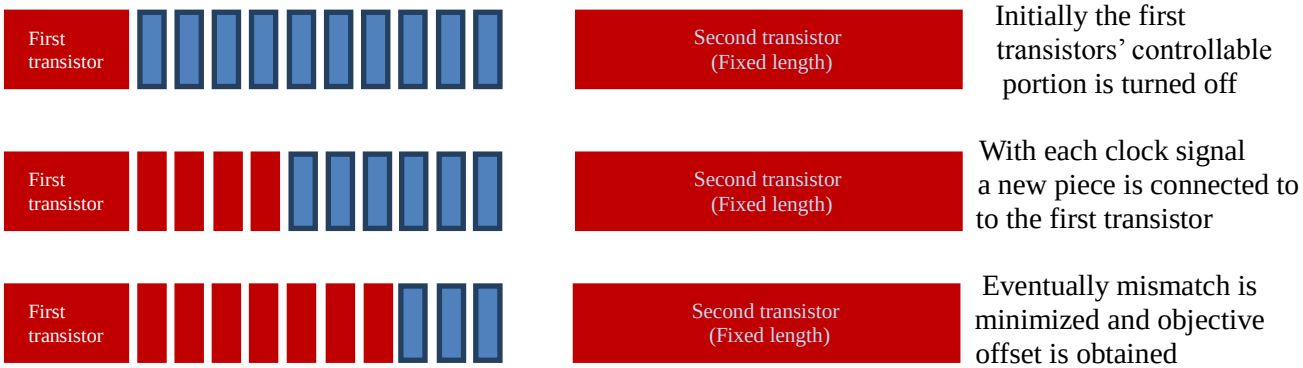

Fig.5 Description of control system

III. Comparator.

The comparator is currently being designed. Design goals are:

- Voltage supply between 2V and 4.2V
- Current consumption below 100nA
- Die area below 1mm^2

IV. Conclusion

In this paper a novel method using digital trimming to reduce offset voltage in comparators is presented. The control part of the circuit performs as expected and the comparator is currently being designed. In the following months a full circuit simulation is expected with fabrication and testing coming after that.

V. References

[1] - "Amplificador integrado para Señales Nerviosas" Joel Gak, Martín Bremermann, Ing.Thesis, Universidad Católica del Uruguay, May 2007, Seccion 4.