Full ISO11784/11785 compliant RFID reader in a programmable analog-digital, integrated circuit.

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Abstract—**Nowadays, powerful off-the-shelve System on Chip (SOC) ICs are available to implement complex communication or signal processing modules. In this work a programmable-analog, programmable-digital IC, is utilized to implement a fully compliant ISO11784/11785 RFID reader module, working at 134.2kHz. Several continuous time programmable gain amplifiers, switched capacitor filters, comparators, programmable timers, clock generators, and a risc CPU core, all them inside the SOC, are used for the signal decoding. The proposed RFID core is part of a handheld reader device, aimed at being used in cattle industry traceability.**

I. INTRODUCTION

The traceability of food becomes a very important issue for the agribusiness industry, not only to improve productivity but also to comply with the increasing number of regulations like the EC 178/2002 among others [1][2]. Particularly in Uruguay a wide national, modern, traceability system has been established for livestock [3], and every beef cattle animal in the country shall be part of it at the end of 2010, including a mandatory electronic ear tag (RFID) each. Radio Frequency IDentification (RFID) is a widely used method to track pieces, lots, animals, in diverse production systems. It is normally based in an integrated circuit, an antenna, and minimum extra components, hermetically sealed in diverse forms (tokens, paper tag, ear tag, etc.), capable to store information ranging from an unique number or EAN.UCC code, to several kbytes, and to transmit it later, contactless, to a reader unit. This ID unit is named Tag, and there exist several frequency bands and standards for the communication protocol. Low cost tags are passive ones that obtain the supply energy from the reader unit by means of a coupling coil.

A. ISO 11784/11785 standard

The main RFID standards operate either around 125-135kHz (LF), 13.56MHz (HF), 900MHz (UHF), and 2.45 or 5.8GHz (microwave) bands [4][5]. Cattle identification tags however work at 134.2 kHz frequency, and the communication protocol is well defined in ISO11784/11785 standard [6] adopted also by ICAR [1]. As far as we know, all the national regulations about RFID for animal traceability

within the cattle industry adopted this standard. At such a low frequency instead of RF waves, the communication link should be better described as an inductive coupling phenomenon between the antennas, that are normally just coils (from tens to hundreds turns of copper wire, in either an air or ferrite core). In Fig.1 several plastic RFID ear tags are shown. ISO11784/11785 define two types of communication protocol for two different types of passive tags, known as half duplex (HDX), and full duplex (FDX). The reading procedure for an HDX tag starts when the reader creates a relatively large alternating electromagnetic (EM) field close to 134.2 kHz, then the tag stores energy in a small capacitor from the induced current in it's antenna coil, and later use the stored energy to transmit data back to the reader (immediately after the AC EM field from the reader decays). The data is FSK modulated at 124.2kHz for the digital '1', and 134.2kHz for the digital '0' symbols, at approximately 8kbits/s. A typical HDX message starts with a '01111110' header, and contains a minimum of 80bits including the country code, unique ID number, and CRC check, among other information. On the other hand, a FDX tag transmits all the time while being powered through the EM field; the datagram starts immediately after the reader provides enough energy. For data transmission, the tag circuit modifies its antenna coil load thus the EM field is modulated. From the reader's perspective, the data is ASK modulated, a modified differential bi-phase encoding (DBP) is used to encode digital '1's and '0's [6]. The ID message structure starts with ten '0's and a single '1' header, and apart from an interleaved '1' every ninth bit for synchronization purposes, the remaining information is similar to that in an HDX message at an approximated rate of 4194bits/s. The tag continuously repeats the message while being powered. A reader unit shall alternate FDX, HDX scan time slots: it shall establish the 134.2kHz EM field for 50-100ms to power tags and search for a FDX reply, then for 3-20ms the AC EM field stops and the reader just scans for an HDX message (ISO11784/11785 precisely defines timing).

B. The developed system

This paper presents a portable RFID reader for both FDX, HDX, tags. In Fig.2, a scheme of the developed embedded

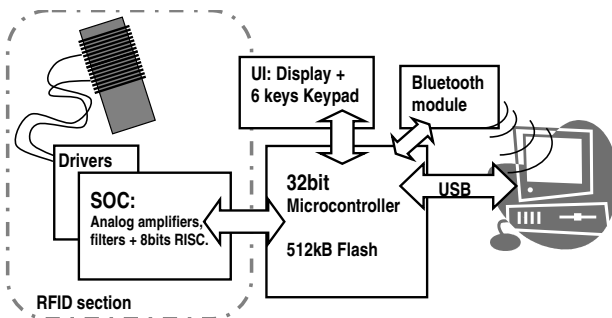Figure 1. Sample cattle RFID eartags.

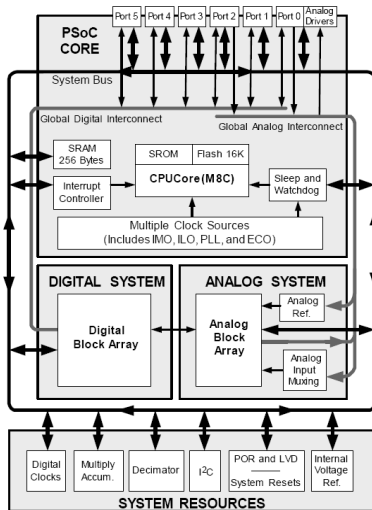

Figure 2. Handheld embedded system scheme.

Figure 3. PSOC internal architecture, reproduced from [7].

system is shown. The RFID core of the handheld unit is implemented on a programmable system on a chip (PSOC) CY27443[7] that contains a simple 8bits risc microprocessor core, and several programmable analog and digital blocks. A scheme of the PSOC from [7] is shown in Fig.3. Analog blocks include continuous time opamps with programmable feedback networks, comparators, as well as several switched capacitor programmable filters [9]. By programming several registers in the PSOC, the analog blocks can be turned into differential PGA's, either low pass or band pass filters, AD's, among others, while digital blocks can be turned into timers, PWM's, SPI communication registers, etc.. Inside the SOC, signals can be routed between inner blocks, to the CPU, or the I/O system. The antenna coil in Fig.2 is composed of several copper wire turns in a special ferrite rod, with an approximated total inductance L_{Ant} = 600µHy. Antenna driving circuitry include several HV Mosfets to switch an AC current to the coil (in a resonant, tuned, LC circuit configuration) to generate the AC EM field, and several resistors, diodes, capacitors, for input signal decoupling. A photograph of the RFID block and antenna is shown in Fig.4. The PSOC transmits the demodulated RFID digital data and clock, to a more powerful 32 bits microcontroller (uC32) that controls the user interface (OLED display, keypad, buzzer, rumble), connectivity (to PC or mobile phone via USB, or Bluetooth), and stores the read information in its flash memory for later use. All the system is powered with a 2200mAh lithium rechargeable battery. The uC32 turns on-off the PSOC, but also handles higher level operations over the RFID datagram like CRC calculation during a read operation. Because the microcontroller system is a standard one, in this work the focus will be on the PSOC to implement the RFID communication protocol.

II. RFID READER BLOCK

Few years ago, RFID decoders were ICs developed for the specific task. However, modern powerful microcontrollers, DSPs, and SOCs, allow the fast development of RFID readers in cheaper programmable platforms. In the case of low frequency RFID, even downconversion is not strictly necessary, and the signal from the antenna can be directly connected to an AD converter and/or a signal processing module. While the reader can be implemented with an analog front-end circuit and a DSP unit, the proposed PSOC device offer an attractive option to implement both analog signal conditioning circuitry, and detection algorithms, in a single chip under CPU supervision. Overall cost, and development time, can be greatly reduced. In effect, PSOCs were successfully employed in 125kHz RFID readers [8] (several similar projects are reported in the Web), but in this work a much more complex reader working close to 134.2kHz will be presented. Apart from cost, the main advantage of PSOCs is ability to fit both protocols (FDX, HDX) in the same platform, so timing and other requirements can be easily adjusted just at firmware level.

A. HDX reading circuit and procedure

The analog section of the HDX read circuitry programmed in the PSOC is shown in Fig.5. The signal is decoupled directly from the antenna coil when AC current is turned off,
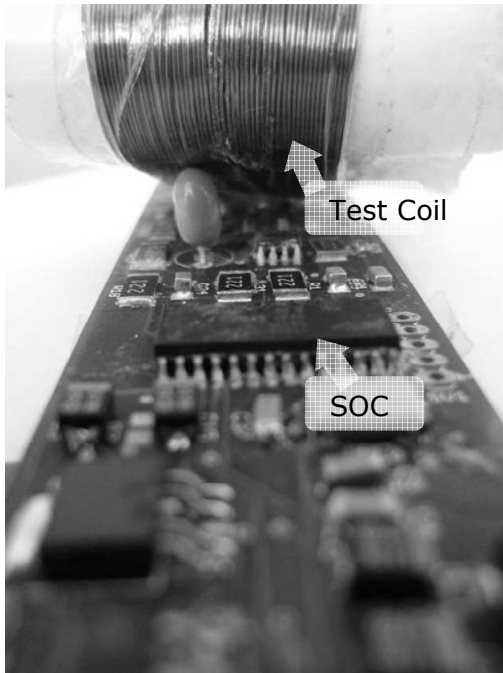
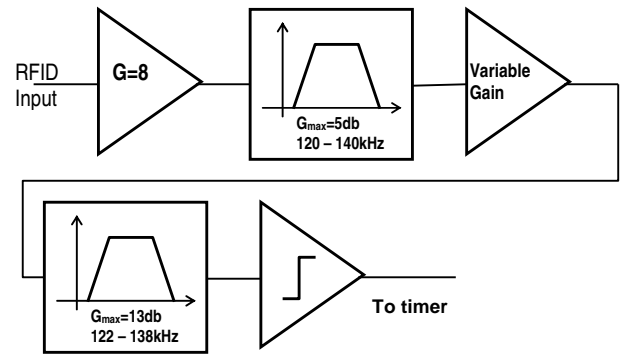Figure 4. A photo of the RFID section of the reader.

Figure 5. HDX section scheme. RFID input is decoded from HDX antenna, note the first gain stage acts also as a low pass.

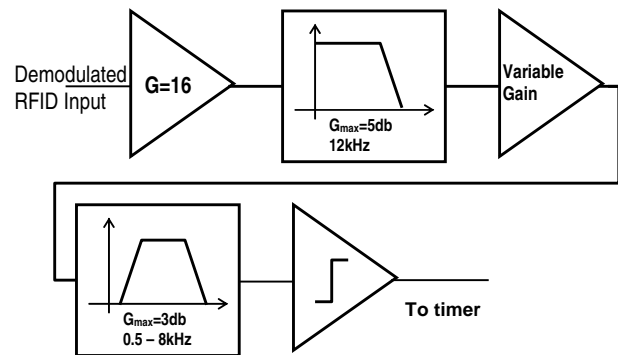Figure 6. FDX detection scheme. RFID input is previously demodulated with a diode after the FDX antenna.

and firstly amplified by a factor 8 with a differential continuous time (CT) amplifier. It should be pointed that because of the finite bandwidth of the amplifiers in the PSOC, the stage is also a low pass filter, the 3db decay is very close to the 134.2kHz frequency. Then a switched capacitor (SC) band pass filter (120-140kHz, elliptic) removes undesired noise, and a second CT-PGA amplifier increases signal level up to an optimum. The gain of this amplifier is adjusted by the PSOC's CPU. Finally a second SC band pass further cleans the signal that is connected to a comparator. The comparator triggers a timer to measure the received signal frequency by means of zero-cross time detection. At a higher level, the PSOC's CPU monitors this timer and counts periods, to estimate whether the received signal is a logical '0' or '1', and identifies the message header for timing purposes. The PSOC provides a recovered clock, and data output to the uC32 regardless of the amplitude of the RFID signal being received. Later the uC32 shall determine through CRC check, if a valid datagram has been received. When no tag is present within the RFID read range, the uC32 will see just digital noise, and a meaningless clock for data timing.

B. FDX reading circuit and procedure

The FDX read circuitry programmed in the PSOC is shown in Fig.6. Before the PSOC, the signal is decoupled/demodulated from the FDX antenna by means of a circuit similar to that presented in [4] for the same task, including a rectifier diode, and a low pass then high pass passive filter. As pointed in [6], most of the signal power of the DBP ASK signal lies between 129kHz and 139kHz (approximately ±5kHz baseband bandwidth after demodulation). First a CT amplifier, with a fixed gain boosts

the signal and acts a first low pass to remove the ripple from the rectified RFID input (thus this stage is the antialiasing filter for the successive SC stage). This first amplifier's bandwidth is limited to 75kHz (3db decay) by setting the low-power mode for the amplifier according to the PSOC datasheet [8]. It shall be highlighted that in a regular FDX read, the ASK signal is a few mV in amplitude but immerse in several Volts AC from the sinusoidal EM field. Thus a very large 134.2 kHz and harmonics components, still persist after demodulation and shall be removed. A second SC low pass filter at 12kHz, 750kHz clock frequency, 40db/dec, further removes undesired spectral components, and a second CT-PGA amplifier increases signal level to an optimum. Finally a second SC band pass process the signal to a zero cross detection comparator that triggers a timer to measure each period's time. At a higher level, the PSOC's CPU monitors the timer, to estimate whether the signal currently being received is a logical '0' or '1'. Because of DBP coding, a large period of the received signal corresponds to a logical '1', while short periods correspond to logical '0's, PSOCs CPU implements simple state machine to track the message, header check, clock recovery, and undesired data removal. The PSOC provides an output to the uC32 regardless of the amplitude of the RFID signal being received, later the uC32 shall determine with the CRC if a valid datagram has been received.

C. RFID mode switching and timing

A very useful feature of PSOCs is their ability to change the configuration context in a single function call. In hundreds μseconds, the PSOC can switch between the HDX and FDX detection schemes of Fig.5, Fig.6, just by changing several registers values. Digital and analog blocks are programmed like different PWMs, timers, amplifiers or filters to fit each signal processing chain thus PSOC resources are shared, as shown in Table I. A typical read cycle starts in FDX mode generating the reader EM field for 50ms. If a FDX header (FDX tag is present) is detected the field is extended up to a maximum of 100ms to allow a complete tag read. If no FDX tag is detected the pulsating EM field is turned off, and the reader scans for a HDX message for the next 3ms. If a HDX message header is detected during scan, then the off time is extended to a maximum of 20ms, to allow the full HDX datagram to be read. If no valid tag is read, including CRC check at the end, the procedure starts again at FDX. On each tenth cycle, a fixed 50ms FDX, 20ms HDX, pattern is interleaved for synchronization purposes. In the PSOC, several timer-programmed digital blocks are used to trigger HDX-FDX mode exchange, to fulfill ISO11784/11785 timing requirements. The frequency basis necessary for the coil ~134.2kHz AC EM field generation, detection algorithms, and FDX-HDX timing, is also synthesized inside the PSOC from a single external standard crystal.

For a better understanding, in Fig.9, the measured magnetic field (using a probe coil) from the reader and tag is shown, for a typical HDX tag in a noisy environment (bit errors are present). For a complete description of different other cases, the documents in [6] can be examined.

III. MEASUREMENT RESULTS

In Fig.7 the measurement results are shown for an HDX tag reading (a small photo of the final reader external aspect can be also seen in the centre of the picture). The experiment consists in moving a probe tag in a plane that contains the main axis of the reader antenna (it will be denoted as reader plane), and registering the reading distance under certain circumstances. Because of the magnetic coupling, the reading distance depends not only on the position, but also on the plane that contains the tag coil (it will be denoted as tag plane). In the continuous line, the absolute maximum reading distance is plot, obtained by rotating the tag plane, orthogonal with the reader plane, up to an optimum coupling. In the dotted line, the minimum reading distance is plot, obtained by moving the probe tag parallel to the reader (tag plane and reader plane are the same). Finally, a more realistic worst case is shown in the dashed line that was obtained by rotating the tag up to a minimum coupling in certain direction radial to the reader tip, but keeping always the tag plane orthogonal with the reader plane. The probe tag is a standard HDX one, and a maximum 33cm read distance was obtained in de direction of the reader (this is the distance normally measured in compliance tests). The reader covers a good reading zone around it. It should be pointed that, from the experience with the developed device, without any special tag alignment the maximum reading distance exceeds the medium zone (dashed line in Fig.7). A very comfortable RFID eartag reading in
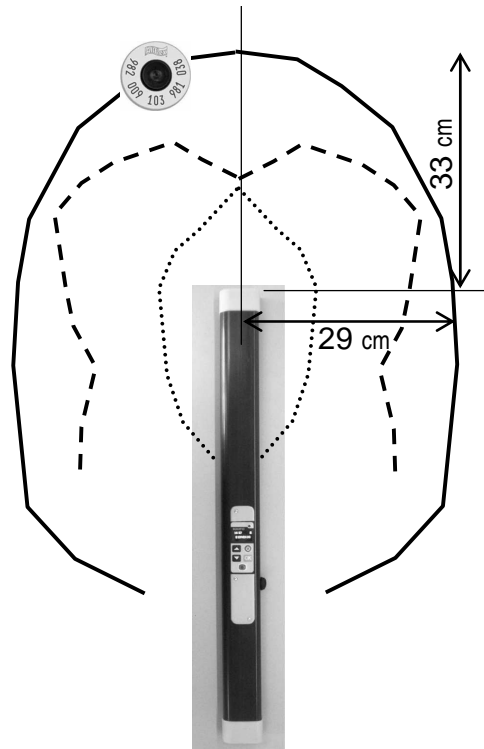

Figure 7. Measured reading distance for a standard commercial HDX tag: maximum distance (continuous line), absolute (doted) and realistic (dashed) minimum distance. Probe tag and reader photos can be observed.
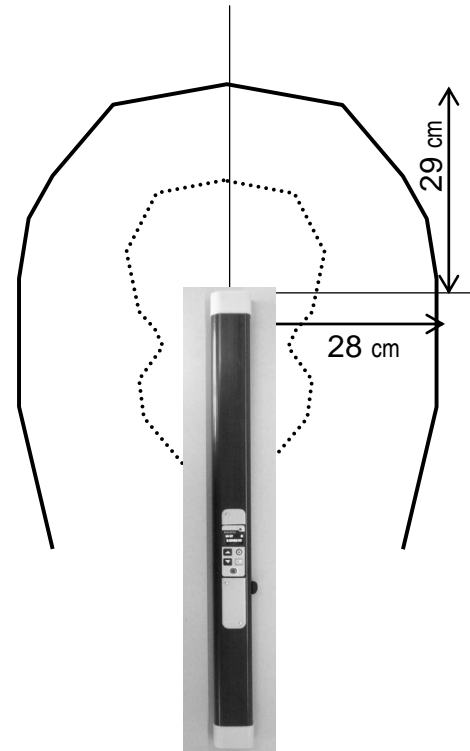

Figure 8. FDX reading distance for a commercial tag: Maximum distance (continuous line), absolute minimum distance (doted line).
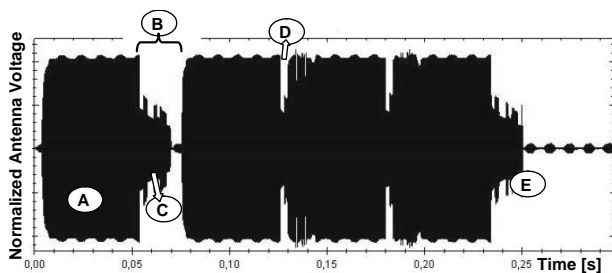
Figure 9. Measured magnetic field using a probe coil behind a far HDX tag (bit errors are highly probable, because of the long reading distance) . The reader creates the alternating EM field for 50ms (A), then stops 20ms for message decoding (B), the HDX-tag message can be observed (C). Because the CRC check was not valid the reader starts the cycle again; 3ms scan slots where not even a valid header is detected are observed (D). Finally a valid message was decoded (E). Note the reader scans for FDX tags in (A) and successive EM excitation time slots, all of them 50ms long because no FDX tag header is detected.

livestock was verified in the field. In Fig.8 the measurement results are shown for a FDX tag reading. The experiment is the previously described one, in the continuous line the absolute maximum reading distance is plot, while in the dotted line the minimum reading distance is plot (the later obtained by moving the tag when the tag plane and reader plane are the same). The third experiment of Fig.7 was not registered for FDX, but the reading distance with no special tag alignment seems only a bit smaller than that for the HDX tag. The probe tag is a standard FDX one, and a maximum 29cm read distance was obtained in the direction of the reader. However while in between different HDX tag samples from different manufacturers only small variations were observed, different FDX tag samples shown sometimes a large difference in reading distances. From the later observation, nothing can be concluded because the problem probably is the quality of the tag, not the data transmission method. Another observation, is that for a moving HDX probe tag, reading is much robust in comparison to FDX ones.

IV. CONCLUSIONS

The architecture of a complete ISO11784/11785 handheld reader unit has been presented, as well as a detailed view of the RFID circuit block implemented in an off-the-shelve programmable analog, programmable digital, SOC integrated circuit. Several features inside the SOC like amplifiers, switched capacitor filters, timers, clock synthesis circuitry, and a complex interrupt handling system were combined with the embedded risc CPU core for the task. The final system fully complies with ISO11784/11785 standard, particularly the accurate timing for FDX and HDX reading was verified. The maximum measured reading distance was 33cm for an HDX tag, and 29cm for a FDX one. The obtained reading distance, as well as reading time response, is similar to that of high-end commercial RFID portable readers. PSOCs seem to be an

excellent trade-off solution for signal processing in the range of frequencies of LF RFID, and at a low cost. On the other hand, the relatively large power consumption of the PSOC, can be a constrain in the case of an application different to a RFID reader were power consumption is certainly not a problem.

The development platform proved to be a powerful, flexible, and easy to use tool for the application example, allowing the fast prototyping off different detection strategies. For the presented application in fact, the PSOC implemented a low cost software-radio in the frequency range of LF RFID.

TABLE I
TOTAL RESOURCES USED FROM THE PSOC.

Resources	HDX	FDX
Digital Programmable Blocks	6/8	5/8
Continuous time Amplifiers	3/4	3/4
Switched Capacitor Blocks	6/8	8/8
Analog Comparators	1/4	1/4
Output Buffers	-	1/4
Interrupts	3	2
Program Flash	40%	

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