A Safe Circuit for the Measurement of Stimuli Pulse Amplitude in Biomedical Devices

Diego Costa, Matías Miguez, *Member, IEEE* and Alfredo Arnaud, *Senior Member, IEEE*

***Abstract*— In this paper an integrating amplifier aimed at estimating pulse amplitude in implantable stimuli delivery devices is presented. The proposed circuit can integrate during each stimulus the effective voltage being applied to tissue, to later use this measure in a self-calibration procedure or in a closed loop stimulator scheme. The circuit was designed and simulated using a 0.6μm HV CMOS technology, it consumes only 8μA current from the battery when it is turned on, and shows an error below 3% for pulses ranging from 100μs to 5ms, and from 350mV to 15V if the time-voltage product does not saturate the integrating capacitor. The circuit is safe in the sense it is not harmful for the patient in the case of a single (independent) circuit failure. The focus of this work is in a pacemaker application, but the developed circuit block can be incorporated in a wide set of biomedical devices.**

***Index Terms*—Biomedical circuits, amplifier, analog design**

I. Introduction

PACEMAKERS sense the natural electric activity both of the atrium and the ventricle of the heart, and stimulate if it is necessary [1]. A stimulus consist in a voltage pulse applied to the cardiac tissue trough properly implanted electrodes, and modern pacemakers allow to program both the amplitude V_S and duration T_S of the pulse. On the other hand, all circuits connected to a patient shall be reliable and safe [9]. Regarding to the safety of an implantable device it shall be compliant the following rule: any single failure (may be a punctured gate in a MOS transistor, software bug, among others) must not cause a catastrophic event. In the case of a circuit in contact with the heart, a catastrophic event may be a significant (for example larger than few μA) DC current flow to tissue [2],[3], or a too high artificial pace rate. In this work the focus will be on the former that is closely related to the design of analog circuits directly connected to the electrodes. The traditional solution to attain safety in a cardiac stimuli circuit or sensing amplifiers is to include capacitors in series with the electrodes [1], [4], [5], [6]. If any transistor fails, the series capacitor blocks DC current. In Fig. 1 there is a simplified scheme of a stimuli delivery circuit following the scheme in [1],[3], where the positive electrode E+ is connected to the positive battery terminal V_{DD}. M_1, M_2 are two very wide high voltage (HV) transistors (HV transistors are required because pacemaker pulses can achieve up to 10V in some cases). During the stimulus M_2 connects E+ to V_{DD} and M_1 connects E- to a negative stimuli voltage V_{Stim}; C_S in the order of few to tens μ-Farads is the safety series capacitor, and in a first approach the cardiac tissue is simulated with a R_T = 500Ω resistor [1][7]. But the effective amplitude of the pulse is lower than V_{Stim}, because M_1 and M_2 have an effective on-resistance, because both C_S and the electrode interface are charged during a stimulus pulse [1], and because normally V_{Stim} is also derived from a charged capacitor C_{Stim} [8]. As C_{Stim}, C_S and the electrode interface get charged/discharged, the differential output voltage defined as usual $V_E = (V_{E-} - V_{E+})$ [5] resembles an exponential curve [1], [4]-[6]. In Fig.2, a measured pulse delivered with a previously developed integrated circuit in the same 0.6μm HV CMOS technology is shown, in this case the starting V_{Stim} = 14.5V but the effective stimulus voltage is defined as:

$$V_{S\_Eff} = \frac{1}{T_S} \cdot \int_0^{T_s} \left| V_{E-} - V_{E+} \right| \cdot dt \qquad (1)$$

T_S is the pulse duration from 100μs to 1.5ms in commercial pacemakers, V_{E-} and V_{E+} are the negative and positive electrode respectively. The effective pulse amplitude V_{S_Eff} of (1) corresponding to the shaded pulse area of Fig. 2 divided by T_S, is the magnitude that must be programmed to a pacemaker with a tolerance within 5% according to usual regulations [7]. But the tolerance of capacitor values, the uncertainty in the M_1 and M_2 on-resistance, and in the value of the voltage reference used to generate V_{Stim}, make it difficult to comply with a 5% maximum error. The uncertainty in the pulse effective amplitude is not only a problem in pacemakers but also in a wide set of modern implantable devices. Finally note in Fig.2 also the so called charge balance stage [1],[5] necessary to discharge the electrode's interface [2],[3]; during charge balance the circuit of Fig. 1 is closed to V_{DD} with a small PMOS switch (not shown). But charge balance stage has no interest in the present work. In this paper an integrating-amplifier is proposed, to measure V_{S_Eff} effectively integrating (1). The circuit will be triggered on each stimulus when needed, and provide at the end of the pulse a value proportional to V_{S_Eff} to an AD converter. This output can be used in a close-loop stimuli configuration or in a self-calibration procedure for the stimuli amplitude. The proposed circuit will be connected like the voltmeter of Fig. 1. In this paper the focus will be on pacemakers, but the same circuit

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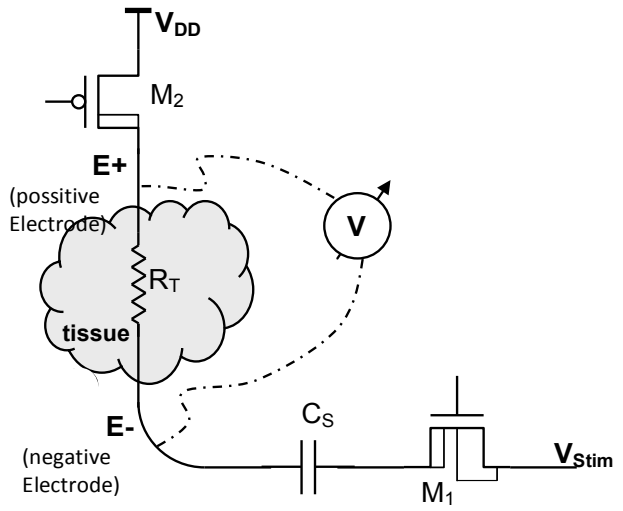

Fig. 1. A simple circuit to deliver a stimulus to cardiac tissue. M_1, M_2 are very wide transistors, and C_S is a series safety capacitor. The voltmeter shows where the pulse amplitude is measured.

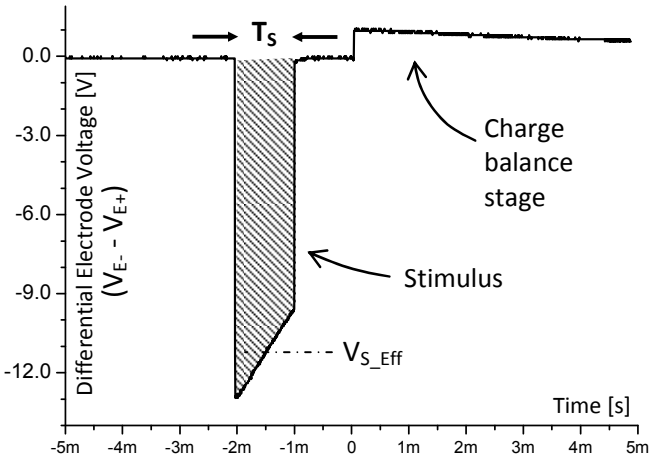

Fig. 2. A measured stimulus pulse. The objective of the proposed circuit is to measure the shaded area.

can be applied to different devices like a wide range of neurostimulators, chronic pain therapy, bones stimulators, among others.

A. Specifications

The circuit is triggered by a digital signal named ON, and shall provide a voltage sample proportional to V_{S_Eff} of (1). The time ON is high, determines the integration time T_S. A chip select CS signal shall be activated before the trigger to turn on amplifiers, and the integrating capacitor is discharged (reset) when CS is low. The complete circuit shall consume less than 10µA from the supply battery when CS is active, and less than 100nA when CS is not active. It should be noted the pulse integrator will be most of the time turned off thus its average power consumption is negligible, but the previous 10µA limit was specified to avoid a significant voltage drop in the case of a battery with a too large series impedance. The pulses to measure may range from 500mV to 10V and from 100µs to 1.5ms in time (these are pacemaker specifications, but a wider range is desirable to cover other devices). Once the system is calibrated, the error of the sampled V_{S_Eff} shall be less than 3% to comfortably comply with the 5% error specified in [7]. The supply voltage V_{DD} will be at least between 2V to 4.5V to cover from the end-of-life (eof) of a regular pacemaker lithium-iodyne battery, to a fully charged lithium medical grade rechargeable one as being employed in some modern implantable devices. The circuit must be completely integrated, without external components.

II. Circuit Description

A scheme of the proposed integrator is shown in Fig. 3. A differential amplifier first converts the differential V_E input signal into a common mode one referred to V_{DD}. This first stage is composed by OA1, $R_{ina} = R_{inb} = 2M\Omega$, $R_{1a} = R_{1b} = 1M\Omega$, $R_{3a} = R_{3b} = 100k\Omega$, $R_{2a} = R_{2b} = \{25k\Omega, 125k\Omega, 725k\Omega$ and $3125k\Omega\}$ (R_2 is a 4-tap digitally programmable resistor). All the resistors are made of high resistivity Poly. The switches M_{Sa} and M_{Sb}, connect/disconnect the input signal to the amplifier. Both switches are HV PMOS controlled by V_{Ctrl}, when $V_{Ctrl} = V_{DD}$ (logical '1') the input signal is not connected, and when V_{Ctrl} = GND (0V – logical '0') the signal is connected to the amplifier. Implementing the two input switches with HV technology is essential to avoid transistor damage in the case of 15V pulses for example; the HV PMOS utilized can withstand voltages up to 50V. The HV switches prevent a current if the tissue voltage is different than V_{DD} (for example if a pulse is applied with a different electrode to tissue). Nevertheless if the switches fail to block the current (a gate oxide rupture in one of the switch transistors for example), the 2MΩ input resistors are big enough to limit the current to a safe value [2],[3]. The large input resistor R_{in} has two more effects: first of all they elevate the input circuit impedance, but also because R_{in} is much greater than R_3 it elevates the differential amplifier input common mode voltage closer to V_{DD}.

The input amplifier can be analyzed as a standard differential one, just by taking the Thevenin equivalent for $R_{ina(b)}$- $R_{3a(b)}$-V_E:

$$V_{O1} = V_E \cdot \frac{R_3}{R_{in} + R_3} \cdot \frac{R_2}{\left(R_{in} \| R_3\right) + R_1} \qquad (2)$$

Since pulses with areas between 35µVs and 40000µVs are to be expected, a variable gain is of great value to achieve the required precision on the measure. To overcome this problem, R_2 is implemented as a programmable resistor as depicted in Fig. 3. A second stage composed by OA2 connected to M_3 gate, R_4 – C_1 integrates V_{O1} in time. The drain of M_3 is connected to the positive OA2 input to form a stable feedback loop that results in a current source charging C_1. Because V_{O1} is a signal referred to V_{DD}, the current through R_4 - M_3 is proportional to the overall circuit input V_E, $I_{R4} = (V_{DD}$-$V_{O1})/R_4$. Both R_4 and C_1 are chosen big enough to lower the power consumption during integration and to maintain the linear behavior of the circuit in all cases. M_3 is a PMOS transistor sized to work in weak inversion to allow the circuit

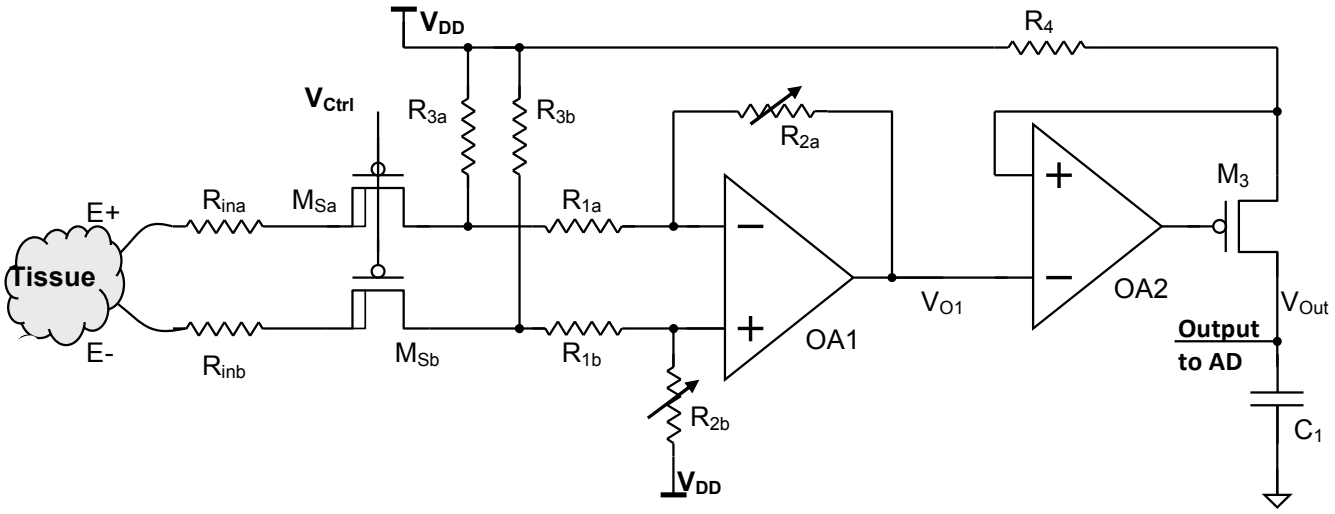

Fig. 3. A scheme of the proposed integrator. M_{Sa}, M_{Sb}, M_3 bulks are connected to V_{DD}.

to operate for a reduced V_{DD}. Equation (2) is used to calculate the output voltage to the AD. Assuming a null charge of the capacitor at the beginning and a total integration time T_S:

$$V_{Out} \approx \frac{R_2 R_3}{R_{in}(R_3 + R_1)R_4 C_1} \cdot \int_0^{T_S} V_E \cdot dt \qquad (3)$$

Thus the circuit output is proportional to the effective pulse amplitude of eq.(1). Precise matched resistors can be employed to determine the relation between V_{Out} and V_{S_Eff}, nevertheless note the result in eq.(3) depends on the absolute value of R_4C_1 and this represents a problem to calculate the effective stimulus. The expected output may vary from one integrated circuit to another thus a calibration procedure on a single parameter at least is necessary.

A. Miller Operational Amplifiers

Both OA1 and OA2 are two identical Miller operational amplifiers (opamps) with NMOS input like in Fig. 4, except for the bias current I_{Bias1} = 0.5µA, and I_{Bias2} = 0.25µA. The opamps were designed using wide input transistors (W_1/L_1 = 50µm/4µm) to push them towards weak inversion in order to minimize the input referred offset and noise [10]. Large 200µm^2 M_3 transistors were also selected to preserve a reduced offset. The estimated offset of the opamps using the foundry mismatch model for the transistors is 1.5mV. The opamps were designed so they have a non-dominant pole greater than ten times the gain bandwidth GB. Although the biomedical signals are relatively slow, in this case the opamps were designed with GB_1 = 2.3MHz, GB_2 = 1.3MHz, to precisely measure the rectangular pulses. The opamps must have a large slew rate to track rectangular pulses with a small integrated error. The worst-case scenario would be a short pulse with a large amplitude and V_{DD} = 4.5V, so to contemplate this case a SR_1 of 1.4V/µs (OA1) , and SR_1 of 0.7V/µs (OA2) were finally selected.

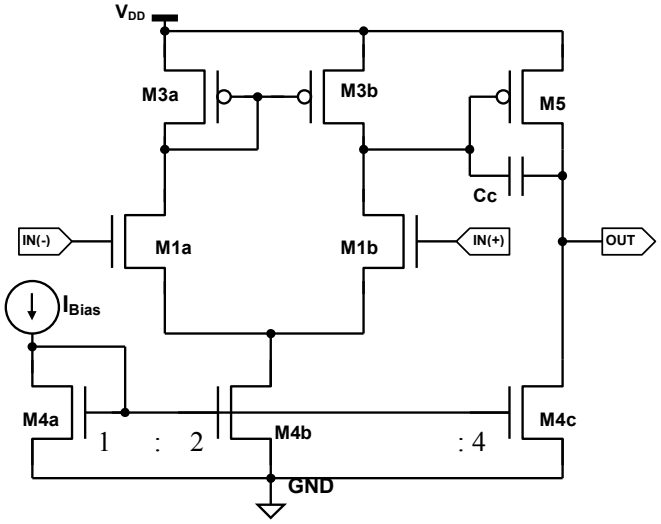

Fig. 4. OA1 and OA2 are standard Miller Opamps.

B. Digital Commands Signals

The integrator was designed to be controlled by an external microprocessor trough an internal asynchronous state machine. The microprocessor will have access to the ON, CS, signals, and two bits b_1-b_0 to control R_2 resistor bank of Fig. 3 to select the best possible configuration depending on the amplitude·T_S product. R_2 can be programmed at any time according to Table I.

For the sake of simplicity, a few switches and logic gates were removed from Fig. 3. During the time CS is low (GND)

TABLE I
R_2 RESISTANCE DEPENDING ON B_1 AND B_0 BITS

b_1	b_0	R_2 Nominal Resistance
GND	GND	25kΩ
GND	V_{DD}	125kΩ
V_{DD}	GND	725kΩ
V_{DD}	V_{DD}	3125kΩ

the output capacitor will be short-circuited and disconnected from the rest of the circuit, the input HV switches will be open and the opamp bias currents will be powered down (the total power consumption of the circuit is only 50nA in this state). When CS is set to V_{DD} the two opamps will be turned on and the circuit is ready to start a new pulse measure (it is recommended for minimizing the error to power-on the integrator at least 10µs before the input pulse begins). The ON signal must be synchronized with the stimulus pulse. When a rising edge on ON signal is detected, the HV switches will be closed and the output capacitor will be connected to the rest of the circuit, to allow the integration begin. On the falling edge of ON signal the integrator will assume the pulse has been stopped, it will disconnect the circuit from the tissue opening the HV switches, and will disconnect the output capacitor avoiding any offset to modify the obtained measure sample. Finally, a new signal READ (circuit output) is set to V_{DD} to indicate the microcontroller if necessary that the process is completed and V_{Out} is ready to be converted. At the present a buffer is connected to the output capacitor for test purposes, but a different output scheme may be selected. It is important to guarantee in any case, an infinite input impedance of the readout circuitry for the integrated C_1 capacitor no to be discharged.

When CS is set to GND again, the signal READ will be set to GND too and the capacitor short-circuited erasing the measure and leaving the circuit in its initial state, ready to start the cycle again. To avoid any misinterpretation, note the V_{Ctrl} signal in Fig. 3 is almost ON signal inverted.

C. Layout Techniques

To achieve the specified 3% precision, a careful layout that improves the matching between circuit elements in mandatory. First of all, a particular care was adopted in the layout of the differential pair and the M_3 transistors of Fig.4 to preserve the offset of the opamps below 2mV at the input. But also most of the resistors in Fig. 3 are matched to minimize any uncertainty in their ratios.

The layout of the NMOS differential pair of Fig.4 amplifiers is shown in Fig. 5. Each $M_{1a(b)}$ transistor sized W/L = 50µm/L=4µm was split in an array of 10 unitary ones (W_u/L_u=5µm/4µm) and connected in parallel. Unitary transistors were placed in rows, interleaved, and connected using a common centroid strategy, following the guidelines in [11],[12]. Fig. 5(b) and Fig. 5(c) highlight each of M_{1a} and M_{1b} of the differential pair in dark grey. Regular dummy transistors were placed on both row ends, as well as a guard ring surrounding the transistors to provide a uniform bulk potential and isolate the cell.

According to (3), to achieve a good precision in the amplification of the signal, the ratio of R_x/R_2 has to be precise. Also symmetric resistors $R_{1a(b)}$, $R_{2a(b)}$ etc. has to be matched between them to improve CMRR. This is a challenging problem because R_2 is a programmable resistor, and because there are 14 different resistors to be matched with nominal values varying form 25kΩ to 2MΩ, all of them utilizing high resistivity Poly. To match the resistors a structure inspired by

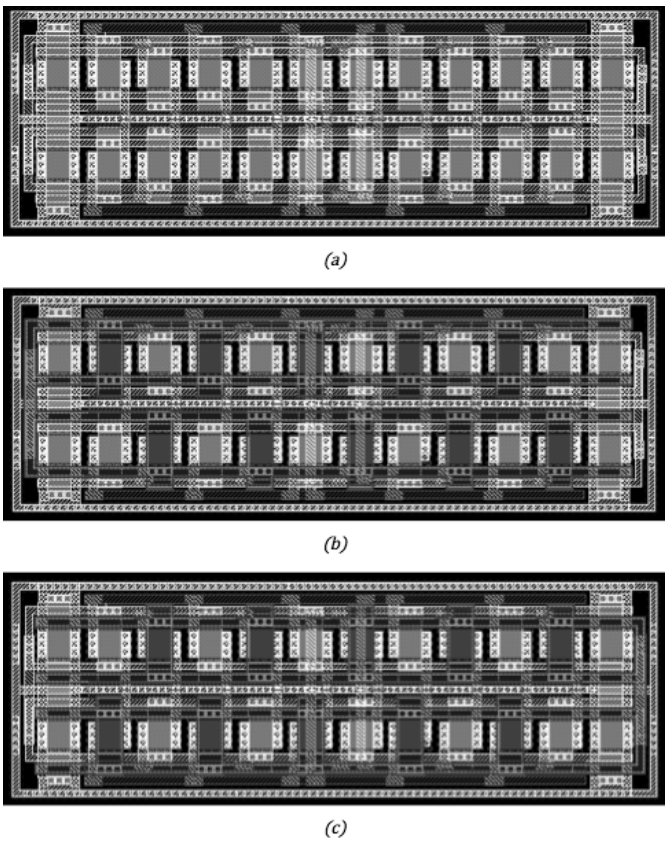

Fig. 5: Layout of the Miller differential Pair. In (b),(c), in dark grey the transistors of each M_{1a}, M_{1b} of Fig. 4.

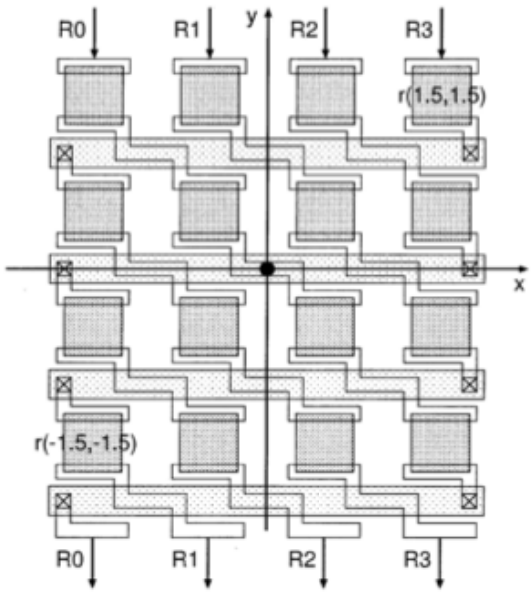

Fig. 6: Layout scheme for the resistors array.

those presented in [11],[12] was also used, connecting like in the case of the transistors several rows with 25kΩ unitary resistors; a small section's scheme of the resistor array is shown in Fig. 6. To form each resistor of Fig. 3, different interleaved unitary resistors of the array are series-parallel connected. According to [11] a minimum of 16 unitary resistors were employed for each resistor including those of low value. For example a 4x4 array of unitary 25kΩ resistors

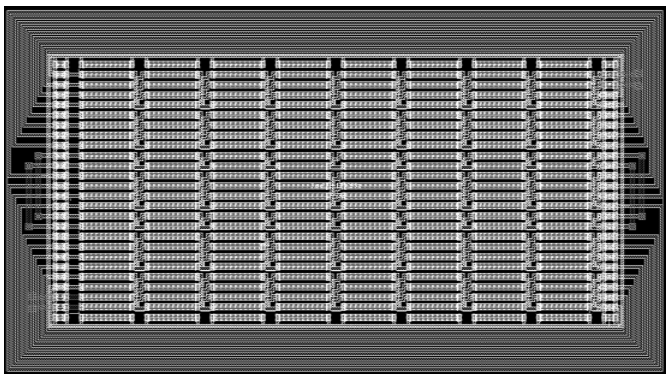

Fig. 7. Layout of the resistor array.

was used to implement the 25kΩ resistor of Table I. In Fig.7, a large 192-unitary resistor array is shown containing R_{ina}, R_{inb}, R_{3a}, R_{3b} of Fig.3 each one implemented combining different interleaved unitary resistors of the array. Usual layout practices can be observed in Fig. 6 and Fig. 7, like (small) dummy resistors at the row/column ends, same current flow direction for each unitary resistor, and even a metal structure as symmetric as possible connecting the unitary resistors. The array of Fig. 7 is also surrounded by a guard ring.

III. Simulation Results

Simulation results shows that the capacitor charge is highly linear with a slope proportional to the input voltage V_E. The final capacitor voltage is effectively proportional to the stimulus area of Fig. 2 up to a given maximum of $T_S \cdot V_{S\_Eff}$ value. But since according to (3) the final voltage depends on the absolute value of C_1 and at least one resistor, the proportionality constant may fluctuate from one chip to another. Thus the proposed system shall be calibrated at least one time at the beginning of the device life-cycle. Calibration procedure can be done for a single R_2 value because the resistor options of Table I are all matched together. In Fig. 8, four curves are presented to show the linearity of the circuit. Each symbol corresponds to the final capacitor charge when a pulse of different duration/amplitude is applied. The straight line corresponds to the result of a least square regression (LSR) on each data set. Each of the four data groups were obtained simulating with the four possible values of R_2 in Table I. The input pulses of the simulation were almost rectangular ones (similar to the ones used for calibration in the target application), with a raise and fall time of 100ns.

Since the circuit will be calibrated, it is possible to assume the slope of each line in Fig. 8 to be known and then to calculate the error for any input pulse, as the difference between each symbol in Fig. 8 and the linear fit. Almost two hundred and fifty pulses were analyzed with amplitudes varying form 350mV to 8V, pulse duration T_S varying from 100µs to 5000µs, and considering resistor mismatch fluctuations and opamp offset effect. The simulations show that the circuit is very independent of the battery voltage. A percentile error histogram is presented in Fig. 9, showing that

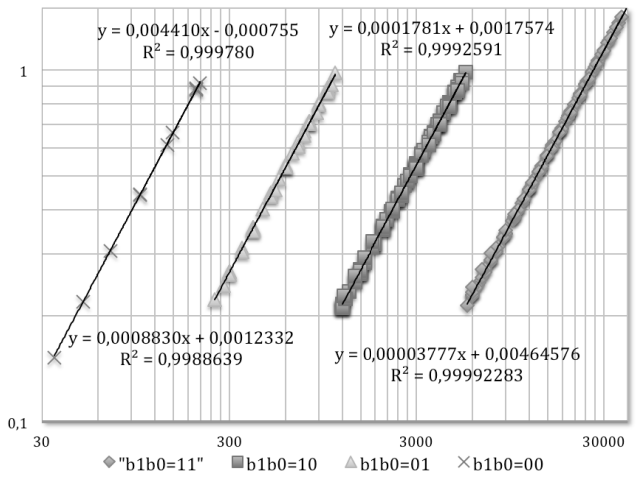

Fig. 8. Simulation results for the output capacitor voltage for 250 different pulses, while varying also R_2 between its 4 possible values.

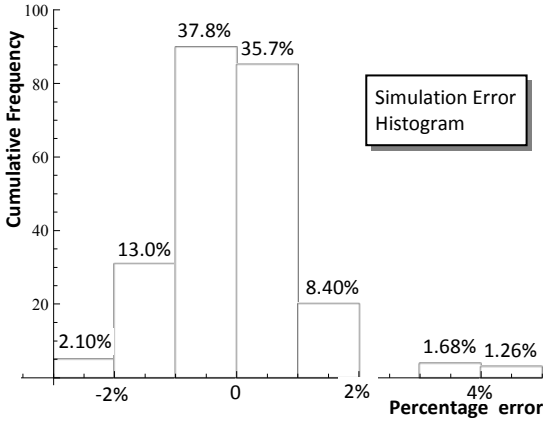

Fig. 9. Simulation error histogram for 250 different pulses, varying also R_2 between its 4 possible values.

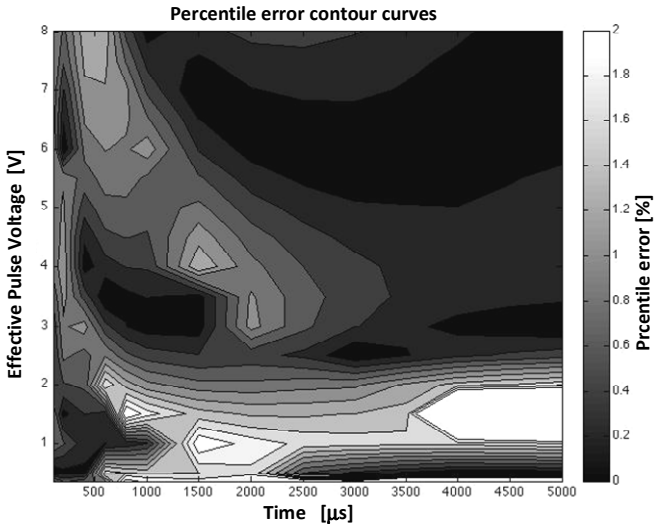

Fig. 10. Simulation error contour plot in the T_S-V_{S_Eff} plane.

in the 73% of the cases the percentile error is below 1%, and there are only 5% percentile measures above the 2% error mark. Finally, in Fig. 10 a contour plot of the percentile error

in the pulse duration-amplitude plane is shown. It should be noted that as expected, small pulses would be affected by a larger relative error due to the more significative effect of amplifiers' offset and resistor mismatch. But Fig. 10 also shows a slight increase in the percentile error for pulses short in time but with a large amplitude. Finally it should be pointed that all the plots in Fig. 8, Fig. 9, Fig. 10 (it is clear in Fig. 8), were obtained for the best suitable R_2 value from Table I (that is, for a given pulse the largest possible circuit gain that cause no saturation is selected).

A safe circuit for the measurement of stimuli pulse amplitude in pacemakers and other biomedical devices was presented. The circuit was designed and simulated in a 0.6µm HV CMOS technology and is currently being fabricated. Some known circuit techniques were combined to develop an inherently safe circuit, able to be in contact with biological tissue. A summary of circuit characteristics is shown in Table II. The high linearity, and reduced overall percentile error, all in a wide supply voltage range, should be highlighted.

IV. Conclusion

A safe circuit for the measurement of stimuli pulse amplitude in pacemakers and other biomedical devices was presented. The circuit was designed and simulated in a 0.6µm HV CMOS technology and is currently being fabricated. Some known circuit techniques were combined to develop an inherently safe circuit, able to be in contact with biological tissue. A summary of circuit characteristics is shown in Table II. The high linearity, and reduced overall percentile error, all in a wide supply voltage range, should be highlighted.

TABLE II
SIMULATED CIRCUIT PERFORMANCE

Circuit Characteristic	Simulated Value
Supply Voltage	$1.7V < V_{DD} < 5.5V$
Current Consumption	8µA
Percentile Error	~ 2%
Input Referred Noise (opamp)	$0.2\mu V/Hz^{1/2}$
Circuit Area	$0.35mm^2$

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