# A Cardiac Sense Channel in a Programmable Analog Device.

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***Abstract*—A cardiac sense channel implemented in a programmable system on a chip including analog and digital blocks is presented. This architecture relies on switching capacitors and switch matrix to create analog circuits with different, programmable transfer functions, such as filters. Then, an ASIC using the same concept and specifically designed to use in low power, medical implantable devices is simulated. Simulations were carried out using 0.6um technology parameters.**

***Index Terms*—low power, switched capacitor filter, analog system on chip, implantable medical applications.**

## I. Introduction

Nowadays, powerful off-the-shelf System on Chip (SOC) ICs are available for implementing complex communication or signal processing modules. Particularly in recent years programmable mixed signal ICs finally are stable in the market (see [4], [13] for example). These systems are especially attractive for the development of medical applications because of the reduced number of the fabricated units of each product. A programmable framework allows fast prototyping for engineering purposes, but also allows producing few hundreds or thousands units without the time and cost inherent to an ASIC. Both aspects result in a significant time to market reduction. In this work firstly a programmable IC is utilized to implement a full cardiac sense channel, including a programmable gain instrumentation amplifier, a Switched Capacitor (SC) band-pass filter and a positive/negative programmable trigger comparator. The target platform is a programmable system on a chip (PSoC) CY8C27443 [12] that contains a single 8bits M8C CPU core and several programmable analog and digital blocks. Biological signals range from sub-Hz to a few thousands Hertz and the PSOC is well suited to for the application. However, a major limitation is the power consumption, which rises up to several mA. This renders the PSOC approach unacceptable in the case of a battery powered implantable medical device, where average current consumptions in the μA range are necessary. The second part of this paper explores how to extend the programmable topology to a low power ASIC device. A micro-power SC programmable filter will be presented, which combines the structure of a PSOC with low power design techniques. The goal is to develop in the future a programmable mixed-signal IC equivalent to the PSOC. This would allow fast prototyping for engineering purposes, or the production of a few hundred units of a medical device that consumes as little as few μA current from a given supply battery.

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### A. Cardiac activity sense channel.

Modern medical devices are complex electronic circuits that perform several sensing, control, and stimulation functions. Although very efficient and sometimes powerful microcontrollers are regularly employed to control these devices [10], because of power consumption constraints there is still room for analog signal processing [9]. Switched capacitors have been for a long time the preferred technique for biological signal processing (see [1], [2] for a cardiac sensing channel), because of its accurate transfer function based in the ratio between capacitors and a reference clock. Although biological signals to be registered in medical devices show a high variability, there are some standards that regulate initial filter accuracy (for example [5]). A cardiac sense channel to detect natural electrical activity consists in a band-pass amplifier and a programmable level detector using a low offset comparator with a DAC-controlled threshold to trigger detection. Fig. 1 shows a block diagram of a typical cardiac sense channel. The comparator is usually a dual detector for positive and negative (normally symmetrical) signal level. The scheme can be also combined with a programmable gain amplifier at the input. This preamplifier can be shared, for example in the case of intracavital ECG recording. The standard in [5] uses the so called CENELEC waveform as the normalized test at the input, the amplitudes to detect range from 100uV to 15mV. In an implantable device the circuit shall consume below 1μA current. Putting aside the power consumption constraint, a programmable analog device is well suited to build a cardiac sense channel, due to its inherent flexibility. Parameters such as sensitivity and bandwidth among others, can be modified on the go either to adjust the sense channel or to perform different tasks like ECG recording or cardiac evoked response detection.

It should be noted that a sense channel like in Fig.1 is not a

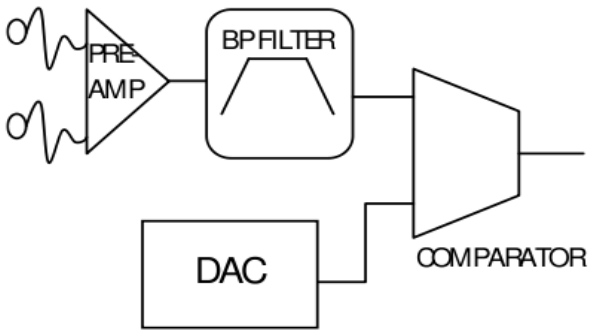


Fig. 1. Block diagram of a typical cardiac sense channel.

complex task for a modern programmable SoC, the case study is taken in this work as a first step and example to integrate a successful programmable analog architecture in a micropower environment.

### *B. The Programmable System on Chip.*

The environment used to develop this PSoC application is the Cypress PSoC Designer©. There are two distinctive blocks, Analog and Digital blocks. Analog blocks include continuous time op-amps with programmable feedback networks and comparators as well as several switched capacitor programmable filters. By programming several registers in the PSoC, the analog blocks can be turned into differential PGA's, either low pass or band pass filters, AD's, among others. It can operate in two modes: continuous and discrete time. In discrete time mode, besides the switch matrix and components, devices need a clock signal (often, two clock signals with distinctive phases) which connects or disconnects different parts of the circuit. This adds yet another degree of freedom to the design, given that swapping phases or different clock frequencies can cause the same circuit to behave differently. The analog section of the used PSoC is divided in rows and columns, each column has one continuous-time (ACT, analog continuous-time) block and two discrete-time (AS, Analog switched) blocks. In a very similar way to an

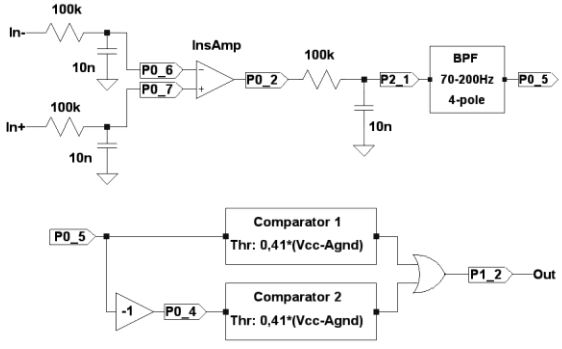


Fig. 2. Simplified schematic of the Cardiac sensing channel implemented in the PSoC, showing on-chip and off-chip signal paths.

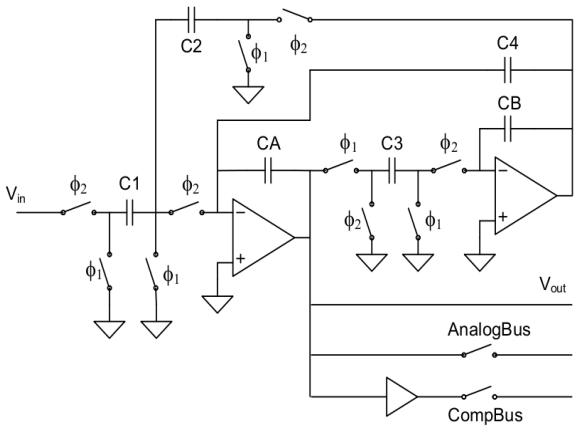


Fig.3. Schematic figure of the filter block implemented in the PSoC, depicting programmable capacitors and clock phases.

FPGA, there are inner interconnection buses, a Global Input Analog Bus and a Global Output Analog Bus. While some technical limitations exist in the PSoC to arbitrary connections between blocks, the switch matrix is flexible enough to create very useful circuits connected to any Input/Output. Each of the blocks in a column shares an independent common clock. There are two configurable analog global clock sources, and each of the digital blocks (e.g. a Timer or a PWM block) can be a potential clock generator. Digital blocks can be turned into Timers, PWM's, SPI communication engines, etc. Inside the PSoC, signals can be routed between inner blocks, to the CPU, or the I/O system

## II. A CARDIAC SENSE CHANNEL IN A PSOC.

The cardiac sensing channel consists of a front end stage, a filtering stage and a comparator stage. A simplified schematic of the sense channel shown in Fig.1 appears in Fig. 2. The layout of the blocks was done in such a way that important signals could be routed outside the system, for test purposes.

There is an RC network at the input for signal decoupling (safety capacitors not shown) and to avoid aliasing because SC filters are employed forward in the signal path. The front-end stage is an instrumentation amplifier comprising two ACT blocks, namely "differential amplifiers", and a SC block, the "conversion amplifier", which converts the differential signal from the electrodes to a common mode one. The amplifiers' gain is programmable in the range from -6 dB to 39 dB. The filter stage is a 4-pole Bessel SC band-pass amplifier with 24dB gain, formed by two bi-quad stages. A schematic diagram of half the filter can be seen in Fig 3. Two two-pole filters can be interconnected using the switch matrix, to form a 4-pole filter. Capacitor value ratios determine the frequency response and gain of the filter. Each capacitor can be programmed using 0 to 31 unitary capacitors in parallel (approximately 70fF each). The cut-off frequencies are located at 70Hz and 200Hz.

The final stage is a programmable window comparator. To implement the comparator pair of Fig. 1, a unity gain inverter amplifier is used to mirror the input signal. Then the input and the mirrored signal are routed into two separate comparators with the same reference level. There is a single output through an OR gate, which indicates to the microcontroller a sense condition is detected.

The sampling frequency of the SC was set to 2400Hz in order to have a minimum oversampling ratio of 12 at the highest frequency of interest. The sampling frequency complies with reported circuits in the micropower range [1].

### *A. Circuit measurements*

The circuit was implemented in a properly shielded custom PCB, Fig. 4. The whole test was conducted inside a metallic box connected to ground and with the circuit supplied from a 9-volt battery, to minimize external noise. The input signal was obtained with an arbitrary waveform signal generator and a resistance divider through 100kΩ and a 500Ω resistor with a resulting attenuation ratio of 201, as recommended in [5]. The measured system frequency response before the comparator is shown in Fig. 5.

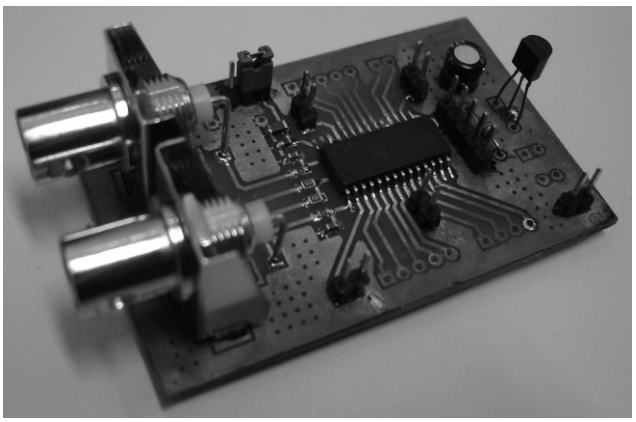

Fig. 4. Custom PCB used to implement the cardiac sense channel.

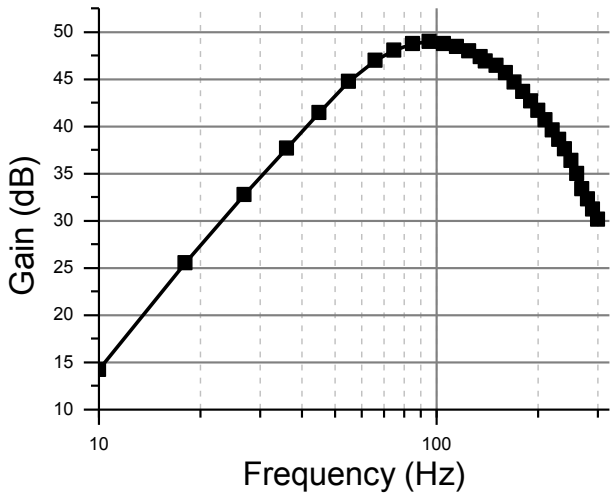


Fig. 5. System frequency response programmed at 54dB gain.

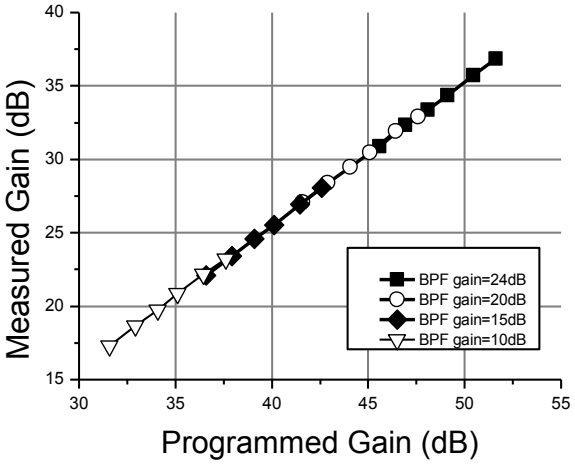


Fig. 6. Linearity Gain test with a CENELEC signal under different BPF and INSAMP programmed gains.

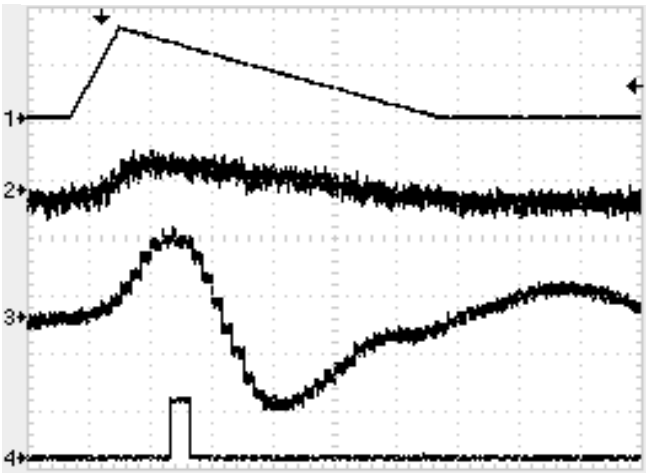


Fig. 7. Oscilloscope capture of the system response to the standard test signal Trace 1, CENELEC signal, in a 200mV/div scale. Trace 2, Insamp out after RC and divisor, 50mV/div. Filter output shown in the middle lower trace (100mV/div), and comparator output in the bottom (5V/div). Time scale is 2.5ms/div.

The detection threshold measurements were conducted using the standard signal CENELEC signal. For the test, a set of different gains was selected in order to measure the relation between programmed and measured gain, Fig. 6.

The overall system response can be seen in Fig. 7. This particular capture was taken with the circuit at high gain (Insamp 27,6dB, BPF 24 dB) and minimum detectable signal.

## III. A MICROPOWER PROGRAMMABLE SWITCHED CAPACITOR FILTER FOR IMPLANTABLE MEDICAL DEVICES.

A fully integrated switched capacitor filter was designed based on the previously described architecture, with the main objective of reducing overall power consumption. The circuit was designed using a 0.6μm CMOS technology with double poly and high resistivity poly capabilities. The basic SC block is similar to the one in Fig.3, using CMOS transmission gates for the switch matrix, capacitor selection bank switches and

phase switches. Many strategies to minimize stray capacitance and leakage effects were used, including the resize of the unitary capacitor to 500fF. The op-amp used was a simple OTA-Miller, designed to have a zero systematic offset, and a total current consumption of less than 250nA. A schematic of the Miller opamp used is shown in Fig. 8 with a 40nA current

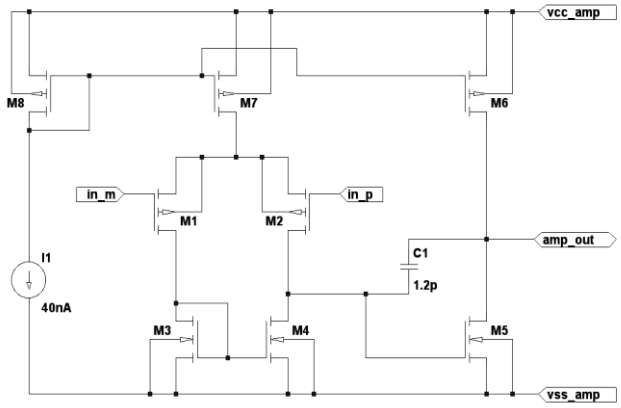


Fig. 8. Schematic of the Miller OpAmp employed in the SC filter.

| | |
|---|---|
| M1,M2 | 180u/2u |
| M3,M4 | 50u/10u |
| M5 | 80u/4u |
| M6 | 80u/4u |
| M7 | 40u/4u |
| M8 | 80u/4u |

Table I. Transistors W/L ratio, in micrometers.

source. The sampling frequency was kept in 2400Hz.

### *A. Circuit simulations.*

Several simulations were conducted to explore the design space, using BSIM3v3 typical transistor (TM) model as well as worst power (WP) and worst speed (WS) corners. The power supply was varied from 1.9V to 2.8V. The frequency response can be seen in Fig. 9. The current consumption of the simulated filter is 700nA.

After that, filter response was evaluated with the standard test signal to measure gain linearity. A plot of measured gain versus programmed gain is shown in Fig 10.

## IV. Conclusion

In the first part of this work, a fully programmable cardiac sensing channel implemented with a commercial PSoC was designed and implemented with satisfactory results. In the second part an ultra-low power, switched capacitor filter with a PSoC structure was simulated, showing technical feasibility. Most of the used transistors operate in deep weak inversion. This design has been sent to XFab to be fabricated, and is

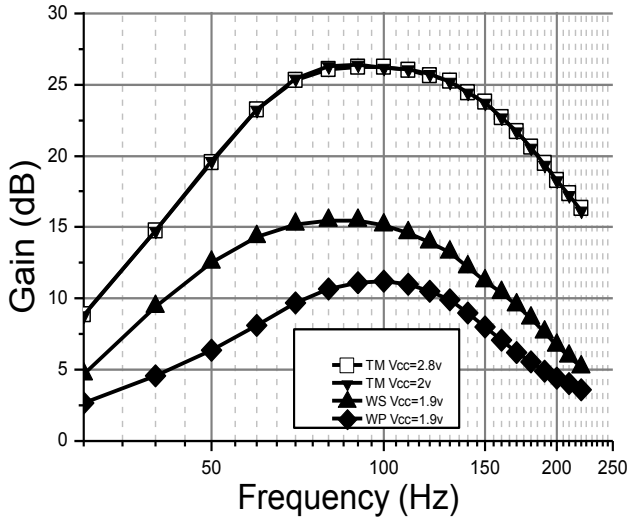


Fig. 9. Frequency response plot of the SC filter. Typical, worst speed and worst power transistors were used, as well as operation under different supply voltages.

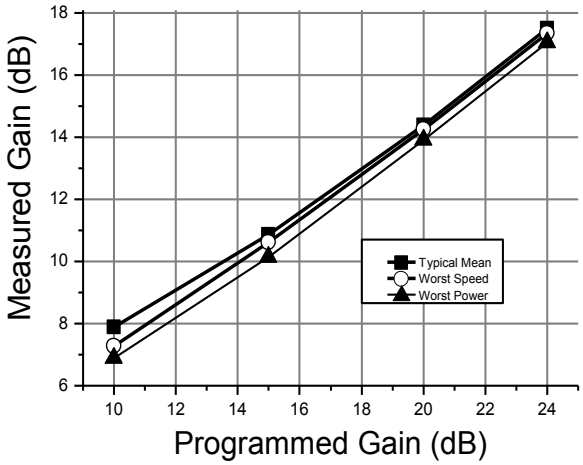


Fig. 10. Measured Gain with the test signal versus Programmed Gain. The upper trace corresponds to the circuit with Typical Mean Transistors. The middle corresponds to the circuit with Worst Speed Transistors. The lower corresponds to the circuit with Worst Power Transistors. Vcc is nominal.

expected to be available soon for testing and measurements purposes. Finally it should be noted that most of the design and simulation was carried on with LT-Spice [11], a free CAD tool. BSIM foundry models were adapted without major problems, and the results were validated along with other available tools.


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