Integrated programmable current source for implantable medical devices.

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***Abstract*— In this paper an integrated current source is presented. The source is digitally programmable and can be used on implantable medical devices. It was designed in AMI C5 (0.5µm) technology, and it is currently under fabrication.**

I. INTRODUCTION

Most modern implants are active stimulators that provide electrical pulses in voltage or current to nerves or muscles [1]. There is an intelligence that controls the precise time, form and duration of the pulses, and amplifiers and sensors that record the signals needed to determine the stimulus. Due to the significant restrictions and challenges in reliability and power consumption, design for medical applications is of academic interest as well as technological relevance.

In this case we will design a current source, which can be controlled by an external microprocessor using a certain communication protocol, as shown in Figure 1. The protocol was designed to allow the integration of more than one source connected to a single data bus.

The first part of this document shows the specifications requiered, followed by the design considerations. Finally, the simulated results and conclusions are presented.

II. SPECIFICATIONS

An 8-bits programmable current source is required, which can provide currents from 150 µA to 37 mA, with a step of 150 µA. The source must work with stimulation voltages (V_{stim}) from close to zero and up to 16 V. The aim is to develop an ASIC with multiple independent stimulation electrodes, each of them able to drain a programmable current to ground from a biological tissue.

On the other hand, the supply voltage can be between 2 and 4,5 V, typical values in this class of applications, considering, from EOL (end of life) of lithium-iodine batteries as those used in pacemakers, to the full charge of a rechargeable battery of medical grade [2].

To integrate several current sources in a single ASIC the area of each one should be minimal.

III. DESIGN CONSIDERATIONS

A. *Current source operation*

A programmable current source usually consists of a current sensing resistor, and an operational amplifier that controls a pass transistor. The feedback loop cancels the voltage difference between the resistor and the reference. Thus, there is a fixed current through the resistor. Configuring the reference voltage by a DA converter produces a programmable current source.

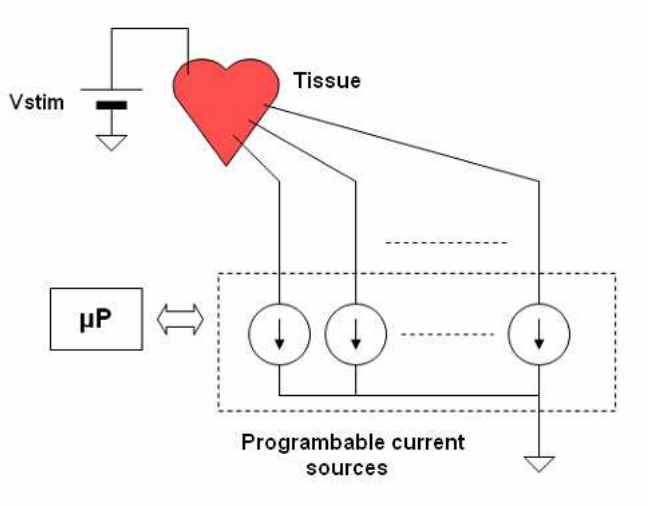

Figure 1. Intended application for current sources.

In this design a slightly different topology was used. As it is easy to integrate several elements in a single ASIC, the DA converter will be avoided, because it is expensive in terms of chip area and electric consumption. Instead, using switches and a bank of integrated resistors the value of the sensing resistor will be changed, keeping fixed the reference voltage. This ensures a small constant voltage drop in the resistance, and therefore a simple and efficient circuit from an energy consumption point of view. This approach cannot be used in circuits using discrete elements as the number of resistors makes it impractical.

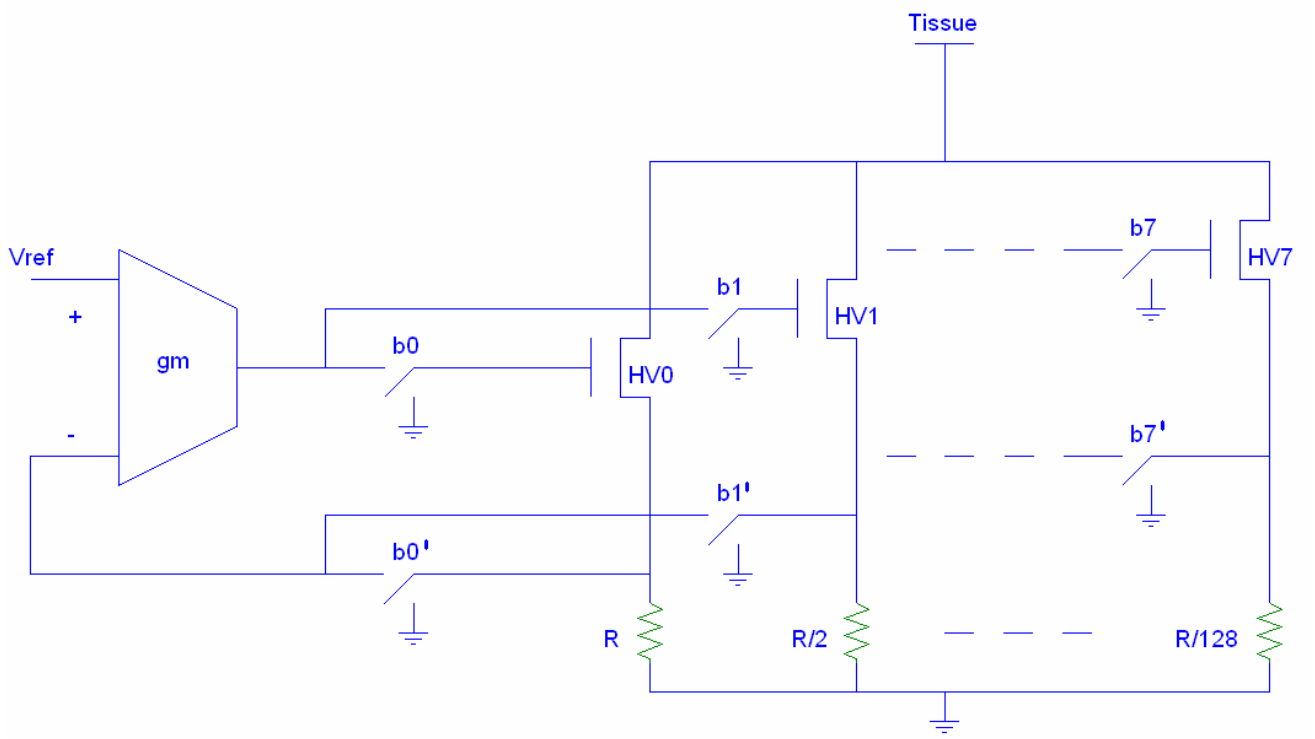

Figure 2. Symplified esquemathic. Switches bX and bX' connect and disconnect each branch.

Figure 2 shows the schematic circuit design. The source consists of 8 branches, each commanded by a bit, resulting in 256 discrete steps. The current is established imposing a fix voltage (Vref) onto a known resistance (R, R/2,…, R/128). This tension is maintained by the feedback loop of the g_M, which injects current into the gates of de HV switches until it conducts the selected value.

These transistors are implemented with high voltage transistors to support stimulus tensions of up to 16 V. The selected technology allows an HV transistors which withstands 20V between drain and source but only 5 V between gate and source.

B. *HV transistor design*

Table 1 shows the current through each branch when it is enabled, the corresponding resistance and the width (*W*) of the HV switch. Taking into account the manufacturer recommendations, all HV transistors were designed with a length (*L)* of 6 µm. Values for the width are also restricted, so the HV transistors were drawn using a unitary cell of W=23 µm and L=6 µm connected in parallel.

TABLE I. BRANCH'S PARAMETERS

Branch	0	1	2	3	4	5	6	7
I (mA)	0.15	0.30	0.60	1.20	2.40	4.80	9.60	19.2
R (Ω)	1830.4	915.2	457.6	228.8	114.4	57.2	28.6	14.3
W (µm) of HV	23	46	92	184	345	690	1311	2622

This unitary cell was implemented with two transistors of 6 µm of length and 11.5 µm of width, as shows the Figure 3.

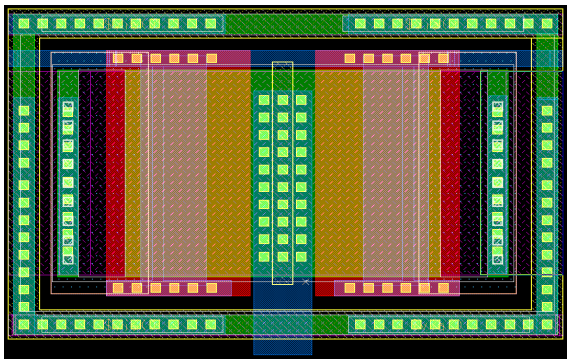

Figure 3. Layout of HV unitary cell with W=23 µm and L=6 µm.

C. *Resistors Bank*

To implement the resistors bank in the smallest possible area, but keeping the accuracy, the series-parallel association was used.

In integrated circuits, due to the large variation of the parameters in the manufacturing process, is not possible to obtain resistors of a determined absolute value. However, with layout matching techniques, relations between resistors can be accurately obtained. This allows the implementation of discrete steps for the current selection.

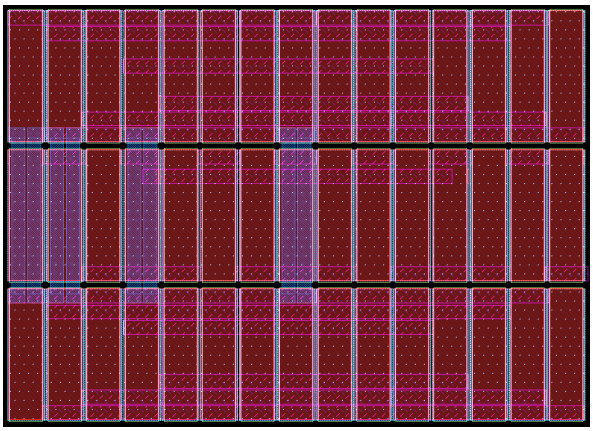

Figure 4. Resistor's layout.

Using a unitary cell, an array of 45 resistors was designed of equal size and shape. In particular *R*, the resistance with the highest value, was implemented connecting in series 8 resistors of unit value *r*. To obtain *R/2*, 4 resistors were connected, and so on until *R/128*, which was implemented with 16 resistors *r* connected in parallel. The resistors bank layout, with its interconnections appears in Figure 4.

A *Vref* of 275 mV was selected, resulting in an *r* of 228 Ω. The reference voltage level selection was constrained by two conditions. The first condition requires that the input offset voltage on the transconductor, estimated around a few mV, should not exceed the 1% of the input voltage. For this reason, *Vref* must be greater than a few hundred of mV. The second condition refers to the stimulus voltage excursion. As *Vref* increases, the operating range of the source decreases, limiting the source performance. Thus the 275 mV value was selected.

Vref is an external reference allowing, if necessary, to calibrate the current source. This may be necessary as the absolute value of *r* varies between different fabrications runs.

For the smallest resistors, the resistance of the metal wires was considered, because they can be greater than the selected resistance if they are not carefully designed. To prevent this, wide and short metal strips were used, especially for branches 6 and 7. HV6 y HV7 were placed next to the bank of resistors, ensuring a negligible voltage drop.

D. Transconductor

The transconductor (g_M) circuit was implemented using a symmetrical OTA [3], as shown in Figure 5. The value of the transconductance was designed considering the total gate capacity of all HV transistors (maximum output current), and allowing a maximum settling time of 3.5 µs. This resulted in a transconductance of approximately 400 µS.

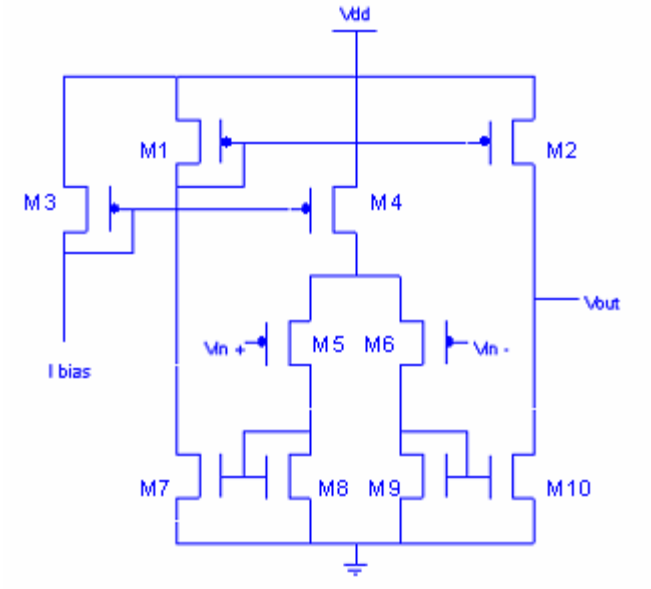

Figure 5. Schematic circuit of the g_M (symmetric OTA). Transistor sizes (W/L): M1, M2 = 8; M3, M4 =18; M5, M6 = 1040; M7, M8, M9, M10 = 3.

The input pair M5 and M6 were designed to operate in weak inversion to reduce offset by mismatch and current consumption [4], with an W/L of 1040. On the other hand, the polarization and current mirror transistors have a W/L of the order of 10, since they were designed to work in strong inversion. To select the sizes of each element, the ACM model was used [5].

Complementing the design, a capacitor C_{out}=8pF was added at the transconductor output (as seen in Figure 6) to reduce the overshoot when the demanded electric current is small, in other words, when only the smallest HV are switched on (branches 0 and 1). This did not significantly affect the response time mentioned before, considering the size of the capacitor is approximately 10% of the total gate capacity of all eight HV transistors.

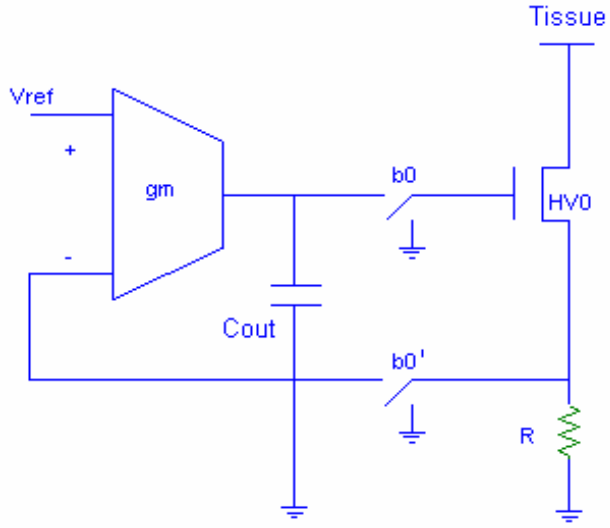

Figure 6. Simplified circuit showing the added capacitor.

The current consumption of the designed transconductor is 100 µA. The possibility to turn off this circuit, reducing consumption when the current source is off, was also added. This feature was implemented by connecting the power supply of the transconductor through an inverter.

In order to reduce mismatch, the input transistors were designed by connecting intercalated smaller transistors in parallel. Similar considerations were taken for all the current mirror transistors and dummies were used in all analog transistors. To avoid parasit signals guards were added. In Figure 7 the layout is presented. The transconductor occupies less than 7% of the total area of the circuit.

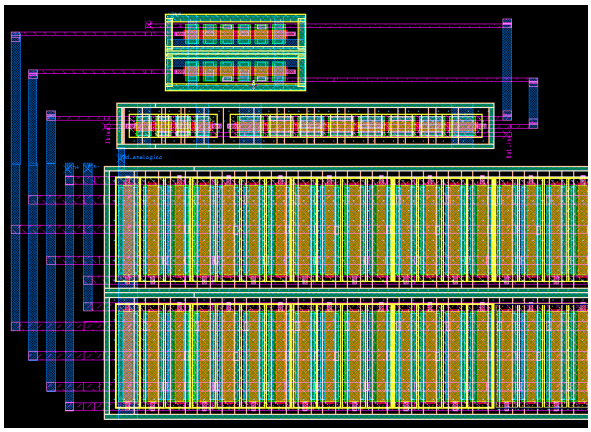

Figure 7. *Gm* layout.

E. Control Logic

The current is selected using a control logic circuit, as shown in Figure 8. Each branch is commanded by its corresponding bit and a common trigger signal.

When the two signals are in a logical '1', both transmission gates will be enabled, closing the feedback loop and allowing the required current to circulate through the HV switch and the resistance.

Otherwise, both transmission gates will be open leaving the feedback loop open and, by precaution and redundancy, the HV switch gate is connected to ground. This ensures that no current is conducted through the branch.

F. Safety

In implantables medical devices it is important to guarantee that no DC current circulates through the tissue, even if a single fault, as can be the puncture of the insulator in the gate of one of the HV switch, occurs. In this design, this precaution requires that no current between the power supply voltage and the tissue can exists, even when there is a single failure. For that reason the switches bX were implemented with high voltage transistors.

Another precaution was not to cross the different metal layers connected to the tissue and the power supply in the layout. This ensures that in case of a failure in the insulator between metal layers, DC current is not conducted through the tissue.

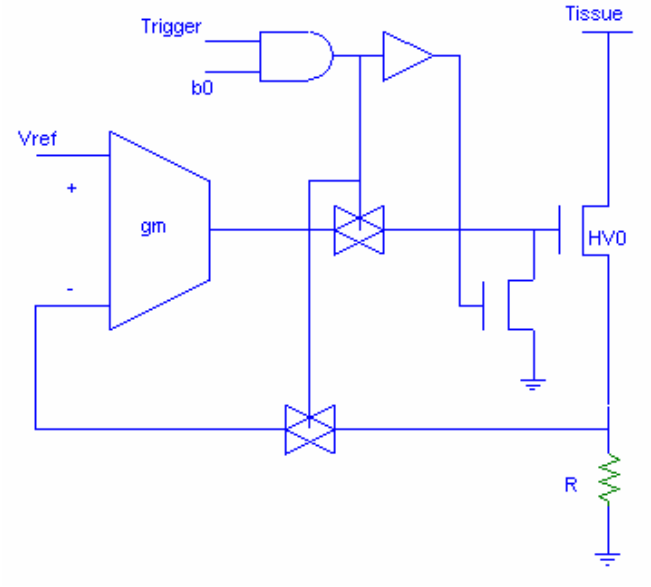

Figure 8. Control logic circuit.

G. Communitacion with the microproccesor

The current source programming is done by an external microprocessor. The communication between the ASIC and the microprocessor was implemented with four digital signals: clock, transmission, reception and enable.

The designed protocol is hereby explained: To establish a communication the microprocessor first turns on the enable signal, and in each rising edge of the clock it transmits one bit of the 16 bits package. This package contains the following information: the required action (erase, write, read or reset), the 8 bit current selection, the source address (since more than one can be included in the same communication bus) and a parity check. After receiving the package, if parity check is correct the specific order is executed.

IV. SIMULATIONS AND RESULTS

Table 2 presents the simulated settling times (90% of the nominal value of the current) for the maximum, minimum and an intermediate value of the current. Also, the simulations were realized with two different values of V_{DD}, both typical values of batteries in implantables devices, 2,8 V and 3,6 V.

These settling times remain valid for stimulus voltages from 1 to 16 V. For tensions under 1 V, settling times increase, but the source continues to function correctly up to 0,7 V.

Figure 9 shows the simulated response for the maximum current with a 2,8 V power supply and a pulse width of 15 µs.

It is important to note that for all the current range, the turning off time is less than 0,5 µs. When the trigger is not enabled, no current circulate through any branch.

TABLE II. SETTLING TIMES FOR DIFFERENT CURRENTS AND SUPPLY VOLTAGES.

V_{DD} (V)	Itheoretical (mA)	Isimulated (mA)	t (µs)
2.8	0.1500	0.1496	0.79
	4.80	4.79	1.27
	37.00	37.13	4.82
3.6	0.1500	0.1506	0.50
	4.80	4.82	0.80
	37.00	37.39	2.90

Finally, Figure 10 shows the complete layout of the circuit, that occupies 0,6 mm^2. To the left the transconductor, in the center the resistor bank, surrounded by the HV switches along with each control logic and on the bottom a register where the current digital value is stored.

V. CONCLUSIONS

An integrated digitally programmable current source, apt for implantable medical devices applications was designed, simulated and its currently under fabrication in AMI C5 (0.5µm) technology.

This current source works with different supply voltages and even when this values approach EOL values, the programmed current is accurately provided, even though settling times are slightly higher. Stimulus voltages may range from 1 to 16 V with no loss of performance.

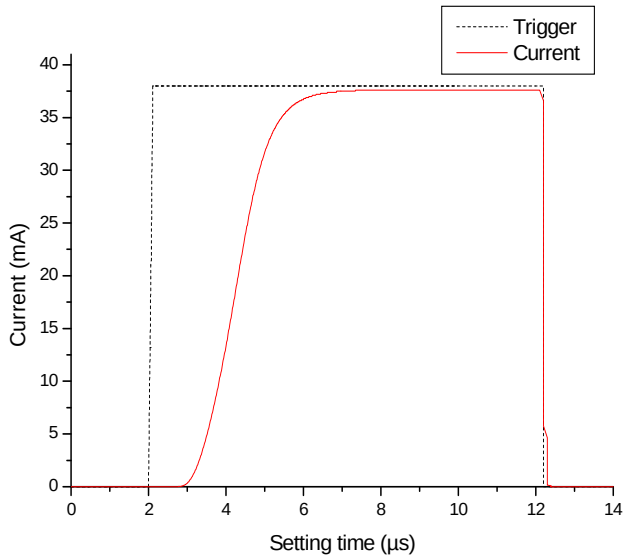

Figure 9. Response for a pulse of 15 µs with V_{DD}=2.8 and

VI. AKNOWLEDGEMENTS

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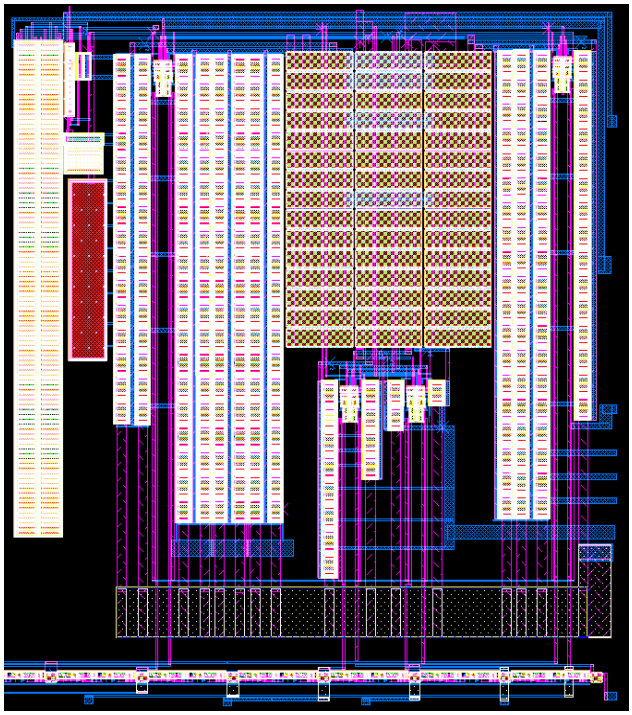

Figure 10. Complete circuit layout.

VII. REFERENCES

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