G_m-C Chopper Amplifiers for Implantable Medical Devices.

Matías Miguez and Alfredo Arnaud
Departamento de Ingeniería Eléctrica.
Universidad Católica del Uruguay
Montevideo, Uruguay
meiyas@ieee.org

Abstract—**In this paper two different G_m-C chopper amplifiers, aimed for signal amplification in implantable devices are presented. The first one is a pre-amplifier for ENG signals that was fabricated in a 1.5 µm technology. Measurements of this amplifier showed input noise of 1.2 nVHz$^{-1/2}$ and 2.5 µV offset with a power consumption of 28 mW. The second is a complete amplifier for EEG signals designed in a 0.35 µm technology. This amplifier, currently being fabricated, has 1 µV$_{rms}$ input noise in the 0.5 to 100 Hz band, at only 1.2 µW of power consumption.**

I. INTRODUCTION

In recent years there has been a considerable research effort in the development of integrated amplifiers, with low noise and low power consumption, for different biological signals. These signals normally range form a few hertz to a few kilohertz and require input noise voltage of a few microvolt.

The main sources of electrical noise in the frequency span of biological signals -apart from coupling noise- are thermal and flicker noise of the circuit elements at the input stage. For a MOS transistor, thermal noise current model is in general not questioned its PSD being (the PSD of the noise current in parallel with the transistor) [1]:

$$S_{i\_th}(f) = \gamma n k_B T g_m \tag{1}$$

where k_B is the Boltzmann's constant, T the absolute temperature, g_m is the transistor's transconductance, $n \approx 1$ is the slope factor, γ = 2, 8/3 in strong and weak inversion respectively [1]. Integrating (1) in the frequency band of interest in a continuous time amplifier, input referred noise result in [1]:

$$v_{nrms} \approx \frac{A}{g_m} = \frac{A}{g_m / I_D} \cdot I_D \tag{2}$$

Where v_{nrms} is the input rms noise voltage in the band of interest, g_m is the input transistors transconductance, I_D is the drain current and A is a constant depending on frequency range, and technology parameters. It can be seen that to reduce thermal noise, the input transistors should work in WI, maximizing g_m/I_D for a given I_D.

To reduce flicker noise, several circuits use the chopper amplifier technique [2,3]. In 1984, Oswald et al. [4] proposed a simple CMOS chopper circuit, just by switching input branches of a Miller-like amplifier. But CMOS choppers have evolved since then to improve usual chopper benchmarks: reduce offset, but also noise and power consumption. A popular topology is the use of a band-pass amplifier in between chopper modulators to reduce high-frequency spikes that introduce residual offset [5,6]. But extra circuitry increases power consumption and circuit complexity and so occupied area. In the case of biological signal amplifiers, extreme low offset is not required thus a better option is to return to a simpler chopper, able to remove flicker noise but consuming less power. In this paper, a chopped G_m-C filter is proposed, and two circuits aimed to be used in implantable medical devices are presented. The first one, is a pre-amplifier for ENG (electroneurograph) signals, it was designed, fabricated in a 1.5 um technology and tested. The second one is a complete amplifier for EEG (electroencephalogram) signals, which was designed, simulated, and is currently being fabricated in a 0.35 µm technology.

A. Figure of merit

If the chopper amplifier is carefully designed, it is possible to push most flicker noise energy out of the band of interest. Regarding thermal noise, it appears useful to define a figure of merit that allows comparing two different low noise amplifiers. If all the transistors in two low noise circuits of similar topology are assumed to operate in the same inversion level (ideally WI), and the circuits have the same supply voltage, the input referred noise voltage is related to power consumption in both circuits:

$$\frac{v_{n1}(f)}{v_{n2}(f)} = \sqrt{\frac{P_2}{P_1}} \tag{3}$$

Where $v_{nx}(f) = \sqrt{PSD}$ [nV/$\sqrt{\text{Hz}}$] is the noise voltage ($v_n(f) = v_n$ in the case of thermal noise) and P_x is the power consumption of each circuit. Observing (3), it is possible to define the following figure of merit:

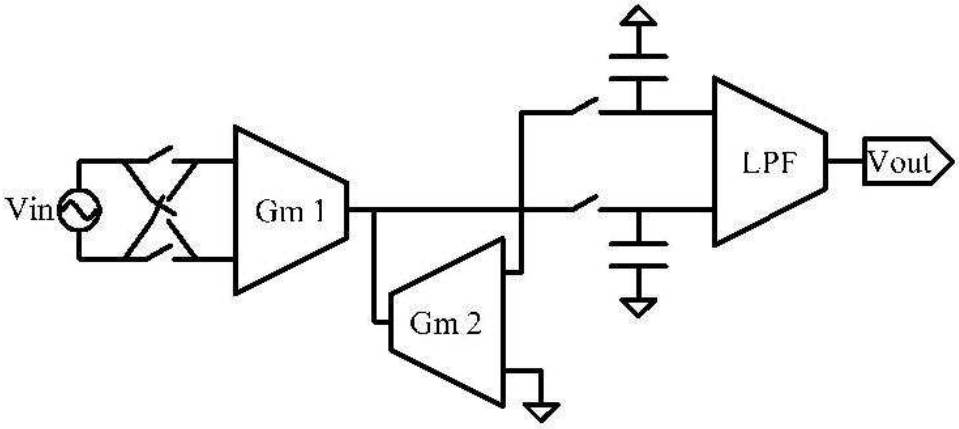

Figure 1. Pre-Amplifier for ENG signals

$$\zeta = v_n \cdot \sqrt{P} \tag{4}$$

A lower ζ indicates a more efficient low-noise circuit for the task of amplifying signals at the minimum power consumption.

II. PRE-AMPLIFIER FOR ENG SIGNALS.

This circuit is intended to amplify ENG signals with amplitudes greater than 1 μVp in the band from 100 to 5 KHz. Low noise is critical, and initially specified as less than 5 $nV/\sqrt{Hz}$ Additionally gain of this first stage must be at least 50, while further amplification is obtained in successive stages. A high CMRR (~ 90dB) is expected.

Figure 1 shows the proposed Gm-C amplifier. The input signal V_{in} is chopped and then amplified on each phase through two independent G_m-C low pass filters. The intermediate signals are further amplified by means of a low-pass filter (LPF) to remove residual frequency components above the band of interest. In this case all the circuit was integrated except for the LPF, which is only needed to provide a cleaner signal and increase gain. Both G_{m1} and G_{m2} were implemented as symmetrical OTA as shown in Figure 3.

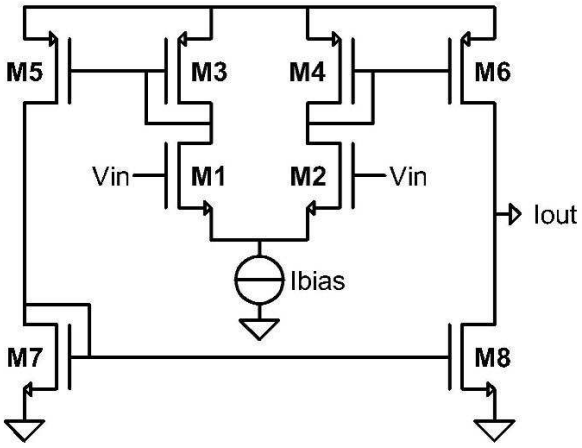

Figure 3. Symmetrical OTA

The transfer function of the pre-amplifier is:

$$H(\omega) = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{[1 + j\omega 2C/G_{m2}]} \tag{5}$$

In Table 1, a summary of measured and simulated results is presented, while in Figure 4 a frequency vs. gain graphic is shown.

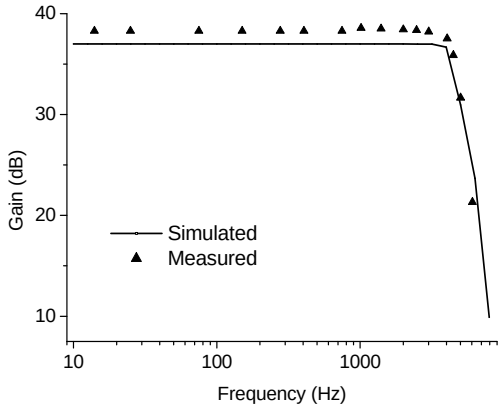

Figure 4. Pre-Amplifier Gain vs. Frequency

TABLE I. MEASUREMENT RESULTS

Measured Results		
	Simulated	*Measured*
Gain	70	80
Bandwidth	5 KHz	5 KHz
CMRR	---	88 dB
Power Consumption	---	28 mW
Input rms reffered noise (.5 to 100Hz)	4 $nV/Hz^{1/2}$	1,2 $nV/Hz^{1/2}$
Supply	5 V	5 V
Active area	0.04 mm^2	
Offset	---	2.5 μV
Area	1 mm^2	

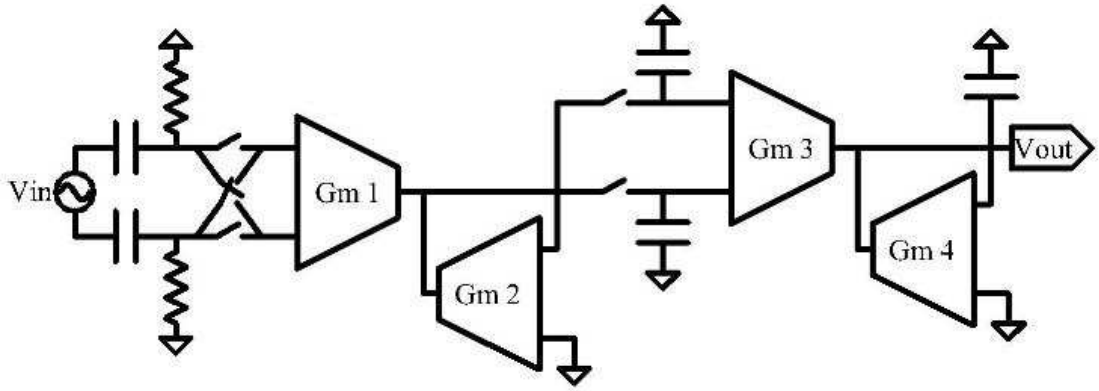

Figure 2. Amplifier for ENG signal

A relatively low offset was obtained, despite the simple topology used. Also most of the area was used to integrate the capacitors, indicating that the performance of the amplifier can be improved by enlarging input transistors, with little impact in the occupied area.

In this first circuit consumption is still large but using the figure of merit in (4), for this amplifier, $\zeta = 5.82 nVHz^{-1/2} mW^{1/2}$, close to the reported values [7]. The consumed power is high, and should be reduced in further work.

III. AMPLIFIER FOR EEG SIGNALS.

This application was designed for a different biomedical application. In this case the same chopped G_m-C topology will be applied for the amplification of EEG (electroencephalogram) signals. These signals range from 1 Hz to 100 Hz approximately. This time the full amplifier was designed, not just the pre-amplifier as in the previous section. Specifications for EEG include power consumption of less than 3uW, 1.5μV of input referred noise, and a gain of at least 40 dB.

The amplifier was designed with two stages, the first one implemented with a chopped G_m-C similar to the Figure 1, and the second stage is a non-chopped G_m-C amplifier. Figure 2 shows the full circuit.

All the circuit was integrated with the exception of the input RC filter which provides the low frequency cut-off.

G_{m-2} and G_{m-4} can be replaced by a resistor connected to ground, with a value equal to the inverse of the G_m transconductance. This required value(30 MΩ and 55 MΩ respectively), is so huge that it cannot be integrated. The three integrated capacitors were designed of a 30 pF value, large enough to be connected to a FET input buffer at the output for measurement purposes. All four G_ms are standard symmetrical OTA as shown in figure 3. G_{m4} linear range was further increased using linearization techniques shown in Figure 5[8].

To reduce power consumption, without reducing the bias current, G_m 1 and G_m 2 were designed to function at only 1.3 V [9]. This allows reducing noise by increasing I_D maintaining the same power consumption.

All the transistors in the G_m's as well as the current copiers were implemented using unitary transistors and series-parallel association, to reduce mismatch [10].

The circuit is currently under fabrication in a 0.35 um technology.

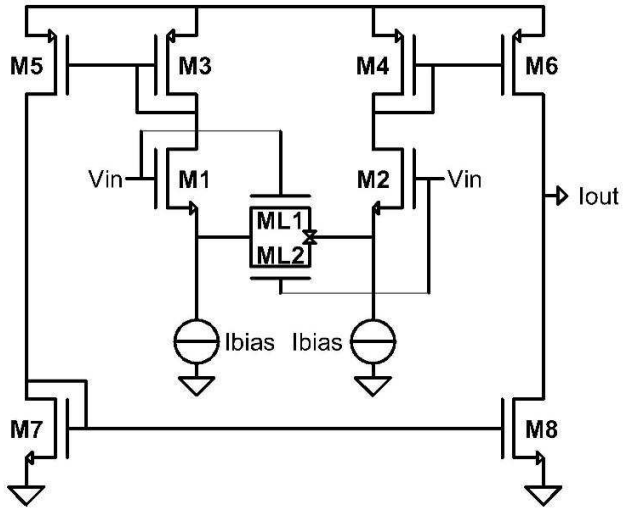

Figure 5. OTA with extended linear range

Figure 6 shows the layout of the circuit; Figure 7 shows the gain vs. frequency graph and Table 2 shows simulated results.

The circuit is now being fabricated; predicted results show a figure of merit $\zeta = 3.5 nVHz^{-1/2} mW^{1/2}$, that slightly improves previous published results like [11].

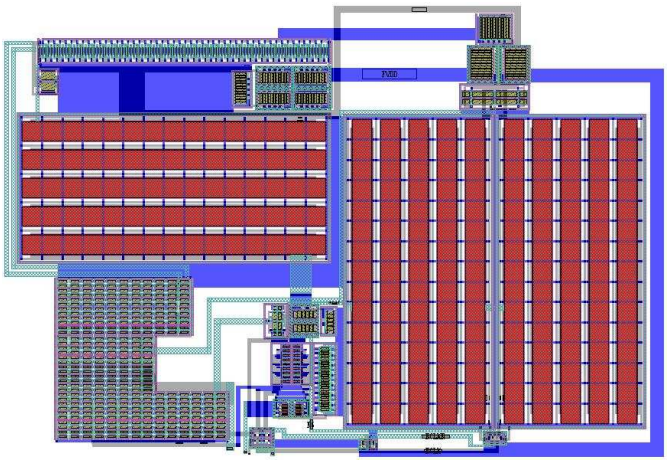

Figure 6. Circuit Layout.

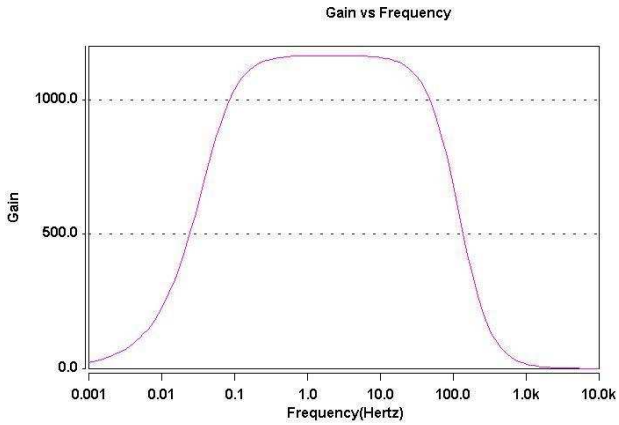

Figure 7. Amplifier Gain vs. Frequency

TABLE II. SIMULATED AMPLIFIER RESULTS.

Simulated Results		
	Implantable requirements	*This work*
Gain @10Hz	> 40 dB	61 dB
High pass frequency	150 Hz	75 Hz
Low pass frequency	0.5 Hz	0.05 Hz
Power Consumption	< 3 uW	1.2 uW
Input reffered noise	1.5 uV	~ 1 uV
Area	-	0.69 mm^2

IV. CONCLUSIONS

In this paper we show that simple G_m-C choppers can be used for the amplification of biological signals in medical implantable devices, obtaining a good trade-off between power consumption and input noise. In a first circuit we show some measured results supporting the simple chopper approach in the case of ENG signals. In a second design, a complete amplifier for EEG signals in implantable devices is shown.

ACKNOWLEDGMENT

The authors are grateful to the MOSIS MEP program for fabricating the circuits.

REFERENCES

[1] Arnaud, A., Galup Montoro, C., Consistent noise models for analysis and design of CMOS circuits, *IEEE Trans.Circuits & Systems I*, Vol. 51, No. 10, pp.1909-1915, Oct.2004.

[2] B.Gosselin, V.Simard, "Low-power implantable microsystem intended to multichannel cortical recording", *IEEE ISCAS'2004*, Vol. IV, pp.5-8, May-2004.

[3] A.Uranga, N.Lago, X.Navarro, N.Barniol, "A low noise CMOS amplifier for ENG signals", *IEEE ISCAS'2004*, Vol. IV, pp.21-24, May-2004.

[4] W. Oswald and J. Mulder , "Dual Tone and Modem Frequency Generator with On-Chip Filters and Voltage Reference", *IEEE J. Solid-State Circuits*, Vol. SC-19, pp. 379-388, June 1984.

[5] Enz, C.C., Temes, G.C., "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization", *Proceedings of the IEEE* , Vol. 84, No. 11, pp.1584 – 1614, Nov.1996.

[6] Menolfi, C., Qiuting Huang, "A fully integrated, untrimmed CMOS instrumentation amplifier with submicrovolt offset", *IEEE J. Solid-State Circuits*, Vol. 34, No. 3, pp.415-420, March 1999.

[7] M. Miguez, A. Arnaud, "A Low Noise GM-C Chopper for ENG Signal Amplification", XIII Iberchip Lima, Peru, march 2007, http://www.iberchip.org/iberchip2007/articulos/7/b/paper/2--meiyas-AlownoisegmcchopperforENGsignalamplification.pdf

[8] Krummenacher, F.; Joehl, N., "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning ," *Solid-State Circuits, IEEE Journal of* , Vol. 23, No. 3, pp.750-758, Jun 1988

[9] Joel Gak, Martin Bremermann, "Amplificador integrado para Señales Nerviosas" Graduate thesis Universidad Católica del Uruguay.

[10] Alfredo Arnaud, Rafaella Fiorelli, Carlos Galup-Montoro "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors", IEEE Journal of Solid State Circuits, Vol. 41, No. 9, pp.2009 – 2018, Sept. 2006.

[11] Timothy Denison, Kelly Consoer, Andy Kelly, April Hachenburg, Wes Santa, "A 2.2µW 94nV/√Hz, Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants" ISSCC 2007.