Bulk Linearization Techniques

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***Abstract*— The use of the bulk terminal to enhance the linear properties of the MOS transistor is examined. Firstly, bulk-linearization of a MOS differential pair is presented, including harmonic distortion measurements. Then bulk-degeneration technique is extended to the triode region to implement large MOS pseudo-resistors. A new asymmetric bulk-modified composite MOS with an equivalent saturation voltage of several hundred mV is introduced, and a 150MΩ pseudo-resistor by stacking a few of these stages is presented. Finally, bulk-linearization of the MOS differential pair and the MOS resistor are combined to implement a 6.4nS transconductor with above 1V linear range, consuming only 6nA, improving the compromise between linear range and power consumption of previously reported small transconductance OTAs.**

Keywords—linearization, bulk-degeneration, CMOS transistor.

I. Introduction

Bulk degeneration completes the three basic techniques of linearizing the MOS transistor, the two others are source and gate degeneration [1,2,3]. Source degeneration is the widest employed technique to enhance a differential pair's linearity, used a lot in RF, audio, and instrumentation amplifiers among others; gate degeneration is less used but known for a long time. But bulk linearization of a MOS differential pair was only introduced in 2007 [4] where an increasing compensating voltage is applied to the bulks of a differential pair, thus decreasing the transconductance and increasing the linear range. The technique is further discussed in [5, 6, 7] where some contributions to the theoretical development and measured circuits are presented. A few circuits were reported previously using bulk degeneration like in [8, 9] but in these works the technique is not identified as such, but specific circuits are presented (note in the case of [9] the patent was issued in 2011 but priority goes back to 2004). Bulk degeneration of a differential pair is introduced in [4] including a theoretical development for the input transistors in strong inversion (SI), simulations, and an OTA example; later in [5] a measured transconductor and a nano-power G_m-C filter are presented, while a high frequency OTA is presented in [6] including for the first time measurements of the HD_3 distortion optimum previously simulated in [4, 5]. Bulk degeneration for a single MOS operating in the triode region was recently introduced in [7]. Finally, it is also possible to utilize the bulk to linearize the MOS capacitor as described in [10]. In this work, firstly bulk linearization of the MOS differential pair is introduced, including THD and a low transconductance linearized OTA measurements. Then, bulk linearization of the MOS resistor is presented including practical MOS pseudo-resistors up to few hundreds MΩ. Finally, both techniques are combined to implement a 6.4nS OTA with a linear range > 1V, consuming only 6nA, and with a reduced input referred offset. The latter OTA can be utilized to implement efficient G_m-C filters aimed at biomedical applications, consuming less power than previously reported ones.

II. Bulk Linearization of a MOS Differential Pair

In a practical circuit, the designer must employ linearization techniques if a differential pair handles large input signals or harmonic distortion is a concern. Source-degeneration by means of a resistor like in Fig.1a is perhaps the simplest and widest adopted linearization technique. The effective gain G_{mR} of the pair in Fig.1a can be calculated by a small-signal analysis in terms of $R_{deg} = 2 \cdot R$ and the transconductance g_{m1} of the input transistors, the result being:

$$G_{mR} = g_{m1}/(1+ g_{m1} \cdot R) \quad (1)$$

But source degeneration has its limits, and a minimum bias current close to a hundred nA is required in Fig. 1a, combined with a very long integrated resistor of several MΩs to achieve a linear range above 1V [5, 11]. Bulk degeneration of a differential pair means an increasing differential voltage is applied to the bulks of the input transistors as the input voltage unbalances the pair [4] and may help to further extend the linear range and reduce distortion. Like in the source degeneration, this voltage tends to compensate currents in the pair thus the transconductance is lowered and the linear range increases. A bulk-linearized pair is different to a bulk-input differential pair like in [12-14]; in the former a compensating voltage (not the input) is applied to the bulk, but the pair's input is still the isolated gate. Bulk-linearized pairs exhibit improved linearity, reduced distortion and input offset [5]. A possible embodiment of bulk-degeneration is shown in Fig.1b.

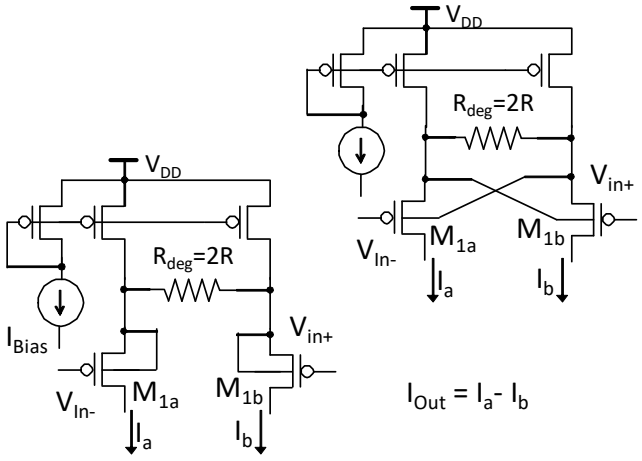

Fig. 1. a) Source degenerated differential pair, b) an embodiment of bulk-source degenerated differential pair. In both cases the output current is defined $I_{Out} = I_a - I_b$.

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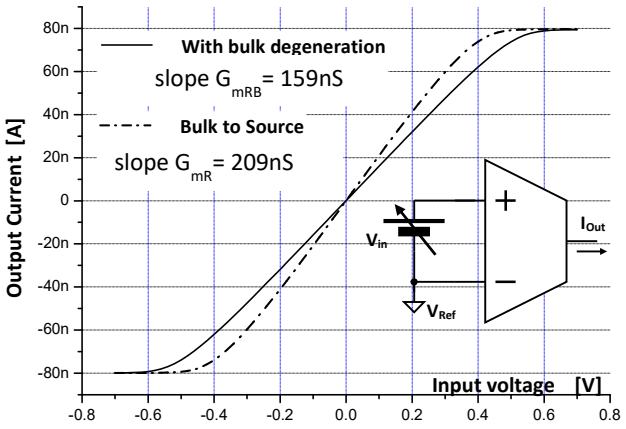

Fig. 2. Simulated transfer characteristic of an OTA based in the pairs of Fig.1 (with/without bulk deg.). $(W/L)_1$=48/12µm, R_{deg}=7.5MΩ, I_{Bias}=40nA.

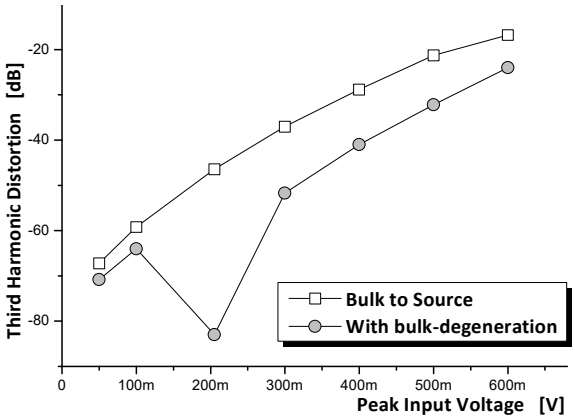

Fig. 3. Simulated third harmonic distortion HD_3 for the OTAs of Fig.2.

The effective transconductance G_{mRB} of the differential pair is:

$$G_{mRB} = g_{m1}/[1+(2n\text{-}1)\cdot g_{m1}\cdot R], \qquad (2)$$

calculated with a small-signal analysis; n is the slope factor [15]; $n > 1$ thus it follows that $G_{mRB} < G_{mR}$ for the same I_{Bias}. Also, since degeneration tends to compensate the current unbalance, the overall linear range is extended. In Fig.2, simulated transfer characteristic of two symmetrical OTAs based on the differential pairs in Fig.1 are shown (R = 3.75MΩ, $(W/L)_1$ = 48µm/12µm, I_{Bias} = 40nA both cases) illustrating the impact of bulk degeneration. The transconductance falls from G_{mR} = 209nS to G_{mRB} = 159nS in accordance with (1), (2), and the bulk linearized pair increases 20% its linear range up to V_{Lin} ≈ 1.1V. In Fig.3, simulated third harmonic distortion (HD_3) is also shown for the same OTAs. A reduction in HD_3 in the case of bulk-degeneration is evident, including a sweet-spot around 200mV where $HD_3 \rightarrow 0$. The HD_3 minimum is a characteristic of bulk linearized pairs, it has been noted in [4, 5, 6] including an analytical demonstration and measurements for the input pair in SI in [6] (but Fig.3 corresponds to moderate inversion (MI)). HD_3 minimum has also impact in total harmonic distortion (THD) thus bulk-linearization can be exploited to implement highly linear amplifiers and filters as required e.g. in RF, audio, and biomedical applications. In Fig.4, THD measurements are shown for symmetrical OTAs using both

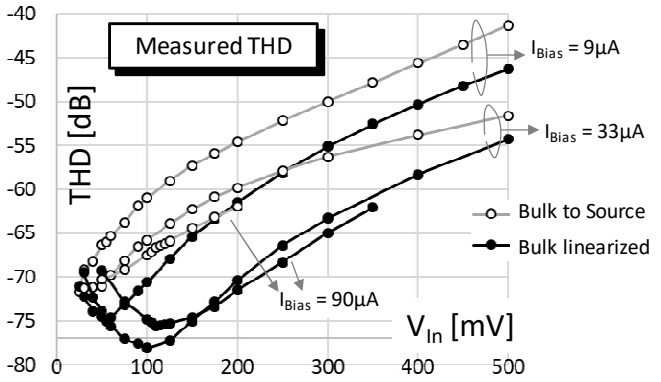

Fig. 4. Measured THD of a symmetrical OTA using discrete transistors.

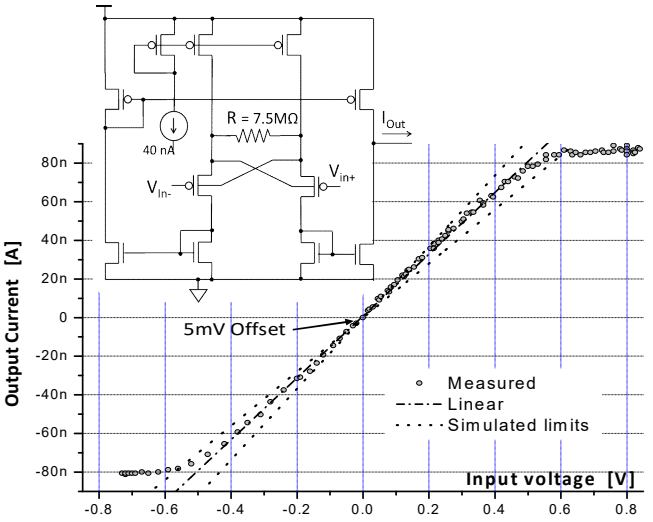

Fig. 5. Measured $I_{Out}(V_{In})$ for the fabricated OTA, closely fits simulations.

input pairs of Fig.1 implemented with ALD1106/07 discrete transistor arrays, while varying I_{Bias} = {9µA, 33µA, 90µA} (pair in MI to SI), R = 22kΩ; the THD reduction for the bulk-linearized OTA is evident in all cases. Finally, the symmetrical OTA of Fig.2 using the bulk-linearized pair of Fig. 1b was fabricated in a 0.6µm technology and tested down to V_{DD} = 1.6V. The measured transfer characteristic is shown in Fig. 5, note the measured G_{mRB} = 160nS close to the simulated value in Fig.2. The current mirrors and input transistors have a large gate area $(W\cdot L) \approx 500\mu m^2$ to minimize offset. The calculated input referred offset was σ_{Offset} = 3.5mV while the measured value was σ_{Offset} = 4.7mV; the OTA die area is 275µm·340µm including a large 275µm·140µm R_{deg} = 7.5MΩ resistor.

III. Bulk Linearization of a MOS Resistor

In the so-called MOS resistor the transistor is operated at the beginning of the triode region where the drain-source voltage V_{DS} is small, with a fixed bulk and gate voltages. The drain current I_D should be proportional to V_{DS} but due to the non-linear nature of the MOS, the linear range is severely limited (like in Fig. 6a). The basic idea of using the bulk to extend the linear region is shown in Fig. 6b, where it is connected to the drain of M_1 (V_{GS} is fixed). The slope $(r_{MOS})^{-1}$ of $I_D(V_{DS})$ is calculated with small signal analysis:

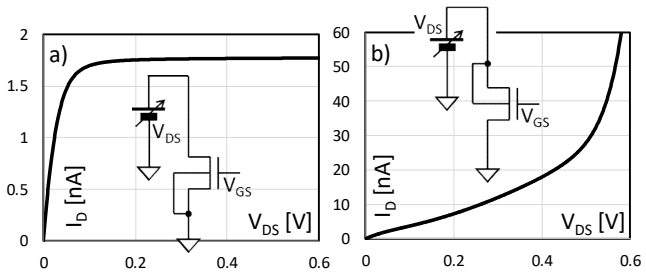

Fig. 6. a) Simulated $I_D(V_{DS})$ for a standard NMOS; b) basic bulk linearized MOS. Both: W/L = 1µm/10µm, V_{GS} close to threshold voltage V_T.

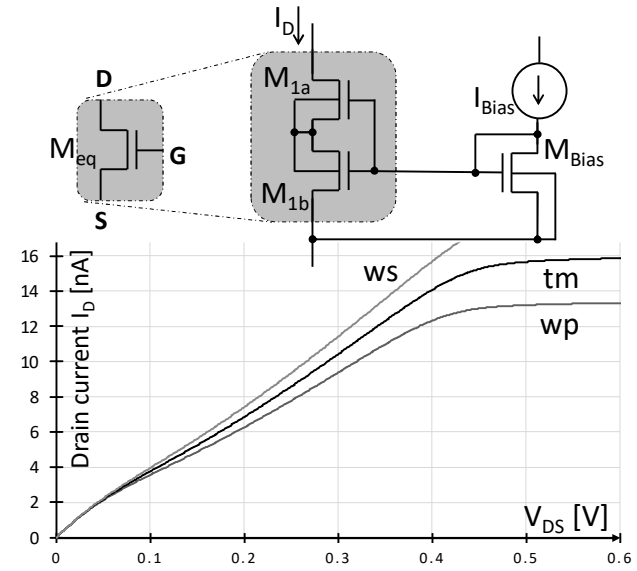

Fig. 7. The proposed asymmetrical bulk-modified MOS M_{eq} on top, and simulated $I_D(V_{DS})$ transfer for typical, worst-slow, worst-power foundry models (tm, ws, wp). Note the equivalent saturation voltage above 400mV.

$$i_D = (g_{mb} + g_{md})\cdot v_{ds} \quad \Rightarrow \quad r_{MOS} = (g_{mb} + g_{md})^{-1} \tag{3}$$

where g_{mb}, g_{md}, are the bulk, drain transconductances respectively. The equivalent resistance r_{MOS} is not constant because both g_{mb}, g_{md}, depend on V_{DS}. @ V_{DS} = 0V, g_{mb} = 0, and the drain transconductance is a given value $g_{md} = g_{mdo}$; when V_{DS} increases g_{md}, decreases and is virtually 0 as M_1 saturates but g_{mb} increases thus the bulk modulates I_D. For the MOS behaving like a resistor, $r_{MOS}(V_{DS})$ in (3) should be constant (g_{mb} increase should compensate g_{md} decay). While for the large signal MOS it is difficult to further develop an analytic expression of (3), the design space can be explored with a SPICE simulator. The result for a long transistor is shown in Fig. 6b with a quasi-linear range up to 400mV when the bulk-source diode starts conducting a significant current, which in fact is a problem because the diode triggers the total drain current and eventually latch-up. To overcome this problem and to further enhance the linear range, a proposed bulk-modified composite transistor is shown at the top of Fig.7: M_1 has been split in two series transistors, M_{1a} sized $(W/L)_{1a}$, and M_{1b} sized $(W/L)_{1b}$, and the bulk voltage V_B is generated from the M_{1a}-M_{1b} MOS divider itself. In Fig.7 also a reference current and a diode-connected transistor M_{Bias} = M_{1b} are used to set V_G. This simple structure was recently proposed in [7] and resembles some pseudo-resistors in biomedical amplifiers [16, 17], but in the former case a bulk linearization is applied, no voltage division is required, and the resistor range will be adequate for a pure resistive feedback network.

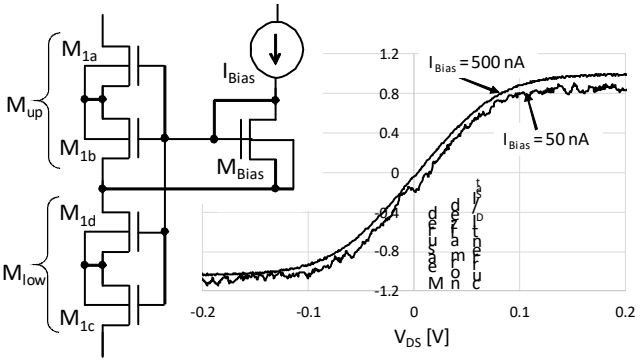

Fig. 8. Proposed circuit block to implement direct-reverse current (bulk-linearized) MOS resistors, and measured results where $M_{1a,c}$ and $M_{1b,d}$, are implemented with 4-parallel and 4-series ¼ ALD1106 respectively .

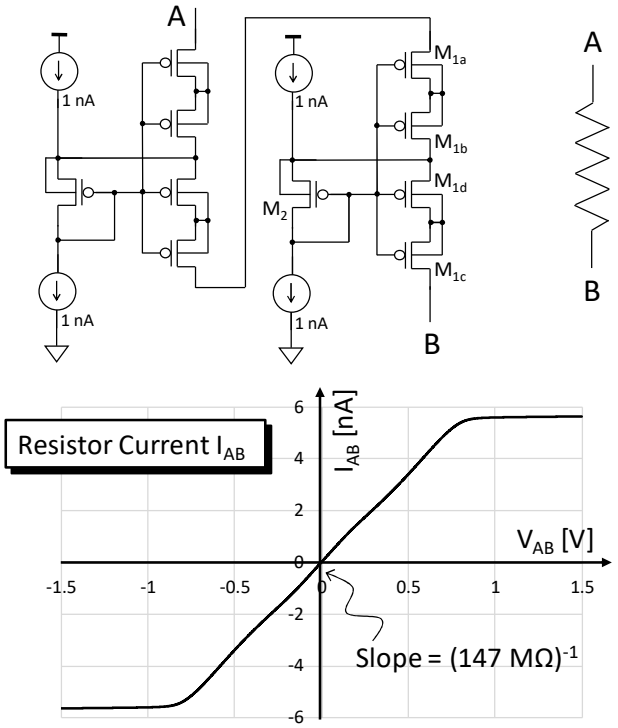

Fig. 9. Two double-sided linearized PMOS form a ≈150MΩ resistor; $(W/L)_{a,c}$=10µm/.4µm, $(W/L)_{b,d}$=.6µm/40µm. Simulated results on the bottom.

Moreover, M_{1a}-M_{1b} can be seen like an equivalent 3-terminal composite MOS M_{eq}, that saturates for a large equivalent saturation voltage V_{Sat_eq} > 400mV. The linear region is greatly extended; the best results were obtained for $(W/L)_{1a}$ >> $(W/L)_{1b}$ thus the composite transistor will be asymmetrical. When V_{DS} increases, as $(W/L)_{1a}$ >> $(W/L)_{1b}$ the voltage drop in M_{1a} is small so M_{1b} rapidly saturates, while M_{1a} remains in the linear region. But as M_{1a} source V_{S1a} (=V_B) increases, V_{GS1a} decreases to such an extent that at certain point I_D will be close to the saturation current of M_{1a}. At this point the voltage drop in M_{1a} will rapidly increase and M_{eq} transistor reaches saturation resembling a cascode. The simulations in Fig. 6, 7, correspond to a 0.6µm technology with $V_T \approx$ 1V threshold voltage; in Fig.7

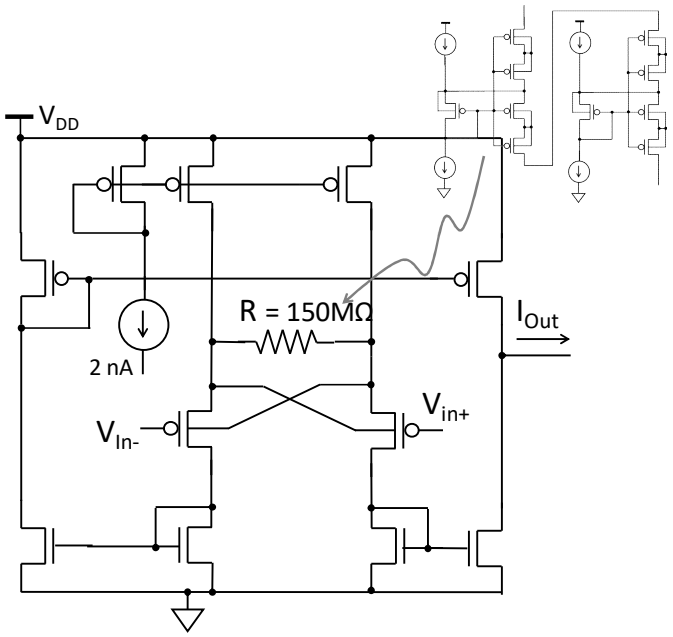

Fig. 10. A bulk-linearized symmetrical OTA, where the linearizing resistor is substituted by a 150MΩ MOS pseudo-resistor. The input pair and current mirrors are sized (W/L) = 1µm/20µm.

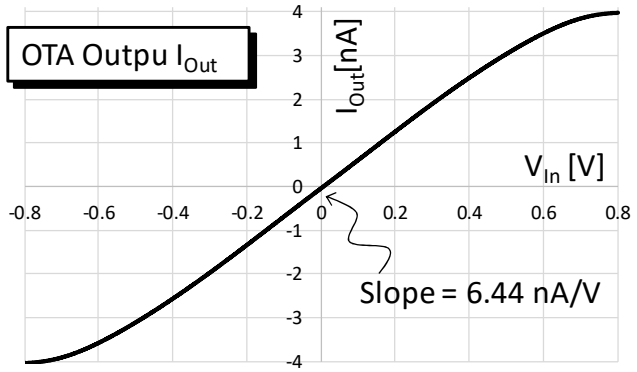

Fig. 11. Simulated transfer function of an ultra-low current consumption OTA, with approx. 1.2V linear range, and a 6.44 nA/V slope.

$(W/L)_{1a}$ = 10µm/1µm, $(W/L)_{1b} = (W/L)_{Bias}$ = 1µm/40µm. Very large pseudo-resistors using MOSFETs can be implemented by stacking successive stages like the one in Fig. 7. In [7] three blocks are connected in series to implement a resistor close to $R_{MOS} \approx 200M\Omega$ with almost 1V quasi-linear range. But a major problem in stacking M_{eq} blocks is that the equivalent resistor cannot be reverse connected, seriously limiting the range of possible applications. An alternative structure is shown in Fig. 8 where two blocks M_{up} and M_{low} like M_{eq} are series connected in opposite direction, sharing the gate ($(W/L)_a = (W/L)_c$, $(W/L)_b = (W/L)_d = (W/L)_{Bias}$). Since V_{GS} for M_{low} is higher, it barely affects I_D. The circuit is symmetrical thus the $I_D(V_{DS})$ is so, as depicted in the plot of Fig. 8 corresponding to preliminary measurements using ALD1106 quad discrete transistors. The measured linearization effect in Fig. 8 is quite limited due to the aspect ratio of the discrete MOSFETs. But the results attract the attention in Fig. 9 where very different aspect ratios for the transistors were simulated, for two blocks analogous to the one in Fig. 8 connected in series, using PMOS transistors in a 0.18µm CMOS technology. The result emulates a 150MΩ resistor, with approximately 1.5V linear range, and consuming only 2nA current to bias the gates. The combined effect of the opposite stacked blocks also helps to compensate slight $r_{MOS}(V_{DS})$ variations in (3) that can be observed in Fig.7 for V_{DS} small (before M_{1b} saturates). Matched sink-source currents are also included for the sake of symmetry, to make $I_A = I_B$ [7].

IV. Combined OTA Circuit Example

As pointed in [5], the problem for the designer of a very low transconductance and highly linear OTA is: to increase the input linear range of a differential input pair with the available current budget, while preserving a low input referred noise, a reduced transistor area, and particularly, a low input referred offset. The linear range ought to be preserved at the lowest possible supply voltage coping with technology parameters variations as well. Then the low transconductance values can be achieved using series-parallel current division to the output [11]. Regardless the transconductance, the best results in [5, 11] require tens nA supply current to obtain a ~1V linear range OTAs (avoiding current division at the input to preserve offset). But both techniques in section II, III can be combined to further improve these results. Previously, bulk-source degeneration of a differential pair was limited because practical poly resistors in standard analog technologies are limited to ~10MΩ to preserve a reasonable die area. But using the pseudo-resistor of Fig.9 lifts this limit. In Fig.10 bulk linearization of a differential pair is utilized in conjunction with a bulk linearized MOS resistor. The large resistor makes possible to reduce the bias current of the pair down to a couple of nA. In Fig. 11 simulated OTA transfer function is shown. The estimated transconductance is 6.44 nS equivalent to a 155MΩ resistor but this value can be increased using series-parallel division [11]. The simulated input offset is σ_{Offset} = 3.7 mV, consuming only 6nA, an order of magnitude below previously reported OTAs in the same range.

V. Conclusions

In this work, the use of the bulk terminal to enhance the linear properties of the MOS transistor is studied in detail. Firstly, bulk-linearization of a MOS differential pair was presented, including harmonic distortion and a fabricated transconductor measurements. Then bulk-degeneration technique was extended to the MOS in the linear region to implement pseudo-resistors. A new topology for CMOS resistors is proposed, which allowed to implement a 150MΩ pseudo-resistor for positive/negative current, by stacking a two (dual)bulk-linearized stages. Finally, bulk-linearization of the MOS differential pair and the MOS pseudo-resistor were combined to implement a 6.44nS transconductor with above 1V linear range, reduced offset, consuming only 6nA, which improves the compromise between linear range and power consumption of previously reported small transconductance OTAs (see [5] for a survey). Bulk linearized building blocks are a valuable family of circuits, with potential application among others in biomedical or RF amplifiers and filters.

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