An Integrated 350V Dimmer

Fabián Torres, Joel Gak, Alfredo Arnaud, Matías Míguez
Electrical Engineering Department
Universidad Católica del Uruguay
8 de Octubre 2738
Montevideo, Uruguay
Email: fabian.torres@correo.ucu.edu.uy, jgak@ucu.edu.uy

***Abstract*—The design of an almost fully integrated phase-cut dimmer is presented. The circuit was designed on a 1um ultra high voltage (UHV) MOS technology in a silicon-on-insulator (SOI) wafer. The dimmer can operate with a duty cycle of up to 95 % power (80 %) and a load of up to 100 W which is adequate for modern domestic dimmable LED lights. The total occupied silicon area is 6.5 mm^2 without pads. *Index Terms*—integrated circuits, ultra high voltage, dimmer, low power**

I. Introduction

By the use of extended and gradual diffusions, varying levels of dopants and a thick oxide, ultra high voltage (UHV) technologies enable the fabrication of several variants of integrated MOS, BJTs, diodes and even IGBTs that can withstand up to hundreds of Volts [1], [2].

In the past, these technologies were highly specific and costly, but with the advent of domotics, LED lights, efficient power sources, micro-actuators and displays, their use has expanded lowering the cost and having frequent multi-project wafer runs (MPW). However, open fabs are still a few and references with specific information such as [3], [4], [5] are scarce. Access to most information about UHV circuits is restricted, since most of the work on UHV requires a specific know-how and is being developed inside companies.

Phase-cut dimmers are circuits that chop the 110 V to 230 V, 50 Hz to 60 Hz AC sine wave to the load to modulate power, as shown in Fig. 1 and Fig. 2.

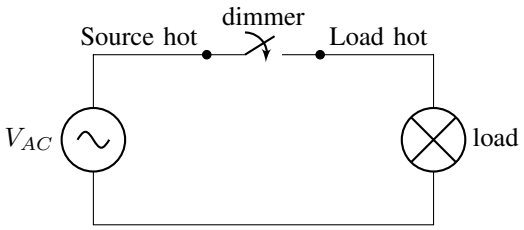

Fig. 1. A diagram of a phase cut dimmer

The classic implementation of this circuit uses a triac as the main switch and a diac to trigger it because of their low cost although they present *leading-edge* limitations [6]. Over the last years, microcontroller [7] and IGBT [8] based solutions have been reported, which allow for a finer control of prepared LED and CFL lamps [9], [10]. Even though

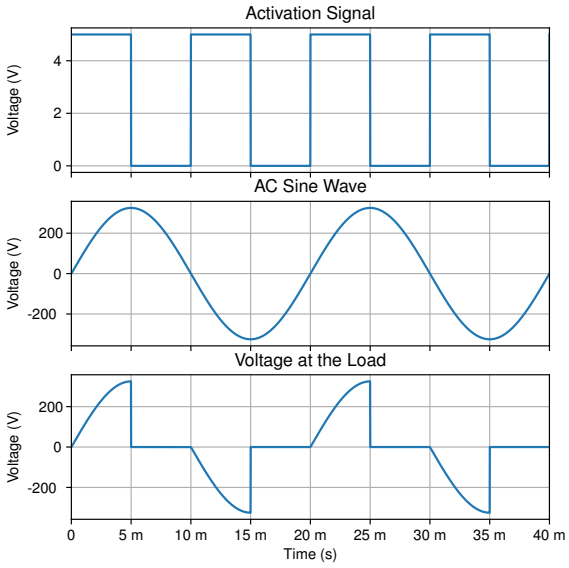

Fig. 2. Load voltage in a phase-cut dimmer.

approximations such as [8] exist, no commercial integrated circuit (IC) exists that implements a complete dimmer with its own power management and a power switching stage. At the time of this paper, no academic papers could be found referencing similar circuits. Therefore, academic research in this area is of interest.

The proposed design is shown in Fig. 3, and it consists of six blocks that can be divided into power and logic related.

The power related blocks (dashed line in Fig. 3) are *Switches* through which power is delivered to the load, a *Gate Driver* to operate the switches, a *Power System* to manage and provide DC voltage from the AC source, and a *Zero Crossing Detector* to keep the system in phase with the 50 Hz to 60 Hz sine wave.

The logic related blocks (solid line in Fig. 3) are a *Delay Block*, that implements a finite state machine (FSM) to control the duty cycle of the switch activation, and an *Analog to Digital Converter* (ADC) to read an analog input to control the duty cycle.

Because the logic related blocks can be implemented with

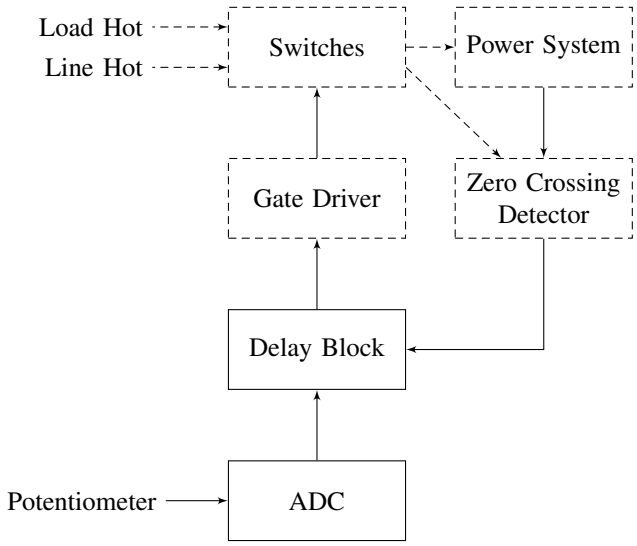

Fig. 3. Top level blocks for the UHV dimmer. *Load Hot* and *Line Hot* are the dimmer terminals that connect to the load and to the grid respectively as shown in Fig. 1. *Potentiometer* is an extra analog input to control the duty cycle. Dashed blocks represent power related blocks and solid blocks represent logic related blocks. Dashed arrows represent UHV connections and solid arrows represent low voltage connections.

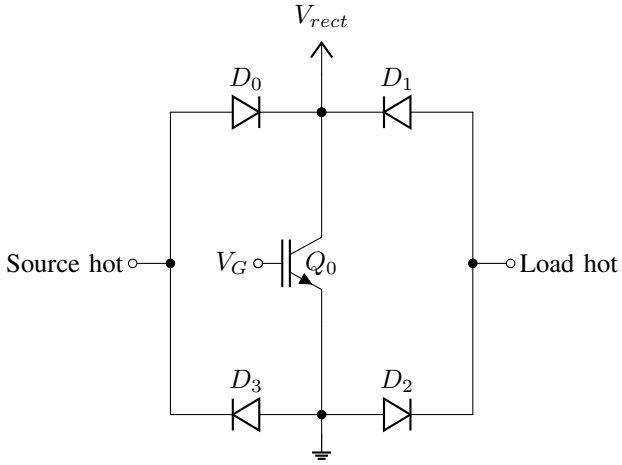

Fig. 4. Switches block.

well known and standard low power microprocessors [11], only the power related blocks are included in the current implementation of the design.

II. Circuit Description

A. Switches

Switches from Fig. 3 are the element of the circuit which blocks or allows feeding power to the load. Since all the current that is reaching the load will be going through this components, the choice of this elements is crucial to determine the power capability of the IC.

IGBTs were finally chosen as the main switching device for the dimmer, since they provide the largest current per unit of area out of all of the devices offered by the used technology.

A configuration like the one on Fig. 4 was chosen due to its simplicity resulting in a reduced number of components.

The inclusion of a rectifier between $Source\ hot$ and $Load\ hot$ makes it possible to determine nodes Gnd and V_{rect} so at all times it can be assumed that $V_{rect} \geq Gnd$. This fact is taken advantage of by the Power Management system described in Section II-C.

Because of the current density limitations established by the used technology for UHV diodes, diodes D_{0-3} could not be integrated into the dimmer and need to be included as discrete components.

B. Gate Driver

Controlling the gate of the Q_0 IGBT shown in Fig. 4 is not a trivial process, because a low on-state voltage will produce low channel conductivity and power delivery to the load will be limited. However, higher on-state voltages are harder to produce and manage by the power management system with diminishing conductivity returns.

In addition, the gate driver needs to be designed to be able to drive a large capacitive load of hundreds of pF such as the gate of a UHV IGBT [12], [13].

An on state voltage level of $15\,\mathrm{V}$ was chosen as a compromise between the $5\,\mathrm{V}$ used for the logic and $20\,\mathrm{V}$, which is the maximum value supported by the technology. The circuit implemented to operate as a gate driver consists of a blind range level shifter. A complete description of a blind range level shifter can be seen in [14] and is not included in this paper for the sake of brevity.

C. Power Management

One of the biggest challenges in the design of the dimmer is to provide a reliable DC source to power the rest of the circuits from the AC grid.

As shown in Fig. 1, the proposed dimmer is a two terminal device. This means that the dimmer will see the complete AC sine wave when the switch is open, but voltage will fall to near zero while power is being delivered to the load.

However, the dimmer needs to power its internal circuits and it cannot do so when near zero voltage is applied to its terminals. This means that the dimmer will not be able to operate at $100\,\%$ duty cycle and a design decision had to be made for the maximum supported duty cycle.

The amount of the energy that is actually delivered to the load as a function of the dimmer duty cycle had to be studied, and is given by equation 1 and shown in Fig. 5.

$$k = D - \frac{\sin\left(2\pi D\right)}{2\pi} \tag{1}$$

Where k is the amount of the energy reaching the load, and D is the dimmer duty cycle.

Based on equation 1, a maximum possible duty cycle of $80\,\%$ was chosen, which can deliver up to $95\,\%$ of the power to the load.

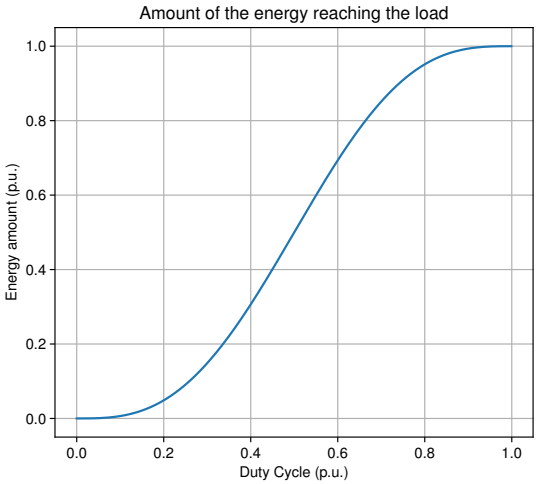

Fig. 5. Portion of the energy reaching the load plotted against the dimmer duty cycle.

As mentioned in Section II-A and Section II-C, the power management system will have to provide two levels of DC voltage (5 V for the logic and 15 V for the gate driver) from a V_{rect} voltage input that is the result of a rectified and potentially chopped sine wave (as shown in Fig. 2).

The system must be able to keep its DC voltages stable when working at a maximum dimmer duty cycle of 80 % and draw in as little current as possible when the dimmer is not in use. For this reason, a low power mode is designed to keep the IC functioning with minimum current consumption at an idle state, and a normal mode is meant to be used for a fast charge of its internal DC sources or to keep the circuit functioning at maximum duty cycle.

The circuit implementation for the power system is shown in Fig. 6, where D_0, D_1, D_2 and D_5 are 5 V Zenner diodes, D_3 and D_4 are Schottky diodes, M_0 is a HV (20 V) PMOS transistor and M_1 is a UHV NMOS transistor. All MOS transistors have their bulk connected to their sources, that are not included in the figure for the sake of simplicity.

The lower part of the circuit consists of a series of 5 V Zenner diodes (D_{0-2}) which will provide 5 V and 15 V when current is applied to them. The excess current (not required to excite the Zenner diodes) will be held at capacitors C_0 and C_1 to be used by the other blocks in the IC.

Diode D_3 is there to prevent capacitor C_1 from leaking its charge into D_{0-2} and C_0, and diode D_4 is there to prevent charge leaking from C_0 when the dimmer is on and V_{rect} is at a near zero value.

The upper part of the circuit can provide a low or high resistance path for current coming from V_{rect} depending on the input signal $Low\ Power$.

When $Low\ Power$ is at a low state, M_0 acts like a closed switch, causing the V_{GS} of transistor M_1 to be near zero, thus acting like an open switch. All current delivered to C_0 and C_1 is limited by an integrated rpolyd R_0 which has a high value

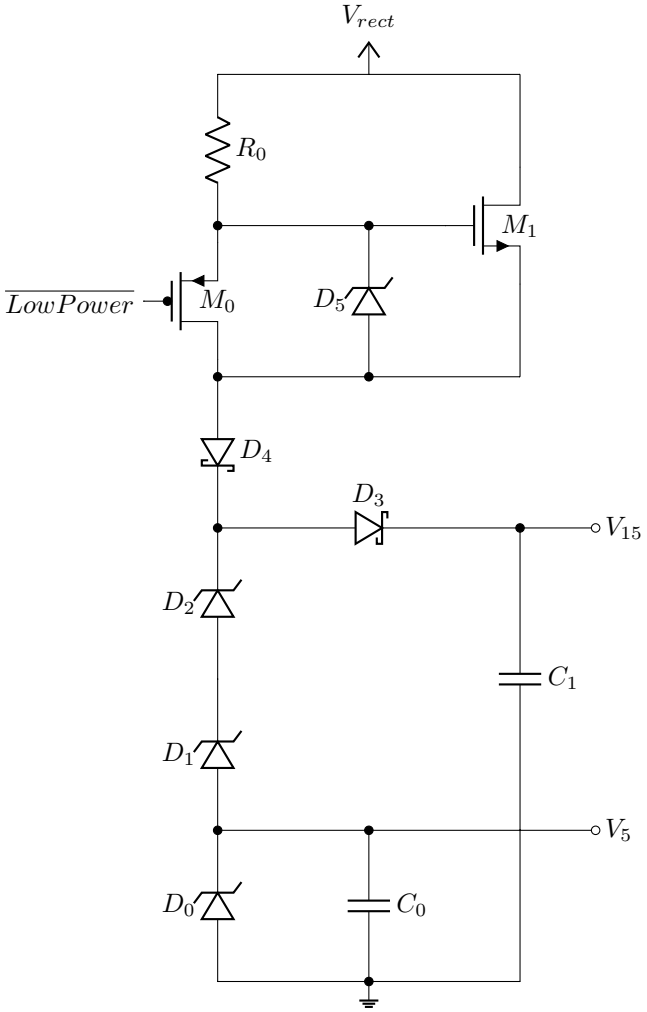

Fig. 6. Power System that delivers 5 V and 15 V from a potentially chopped sine wave voltage.

(1 MΩ).

When $Low\ Power$ is at a high state, M_0 acts like an open switch, causing current to go through D_5 which will impose 5 V V_{GS} on transistor M_1 allowing for a larger current (up to 6 mA) to reach C_0 and C_1.

Low power mode can be controlled from outside the IC with a 0 V to 5 V signal, which will be adapted to the 0 V to 20 V range inside the IC with a pull up resistor.

All devices in this block could be integrated, with the exception of capacitors (C_0, C_1) because of the (100 µF, 10 nF) needed to hold the charge for up to 8 ms (80 % of a semi-cycle for a 50 Hz signal).

D. Zero Crossing Detector

Zero crossing detection is crucial for keeping the dimmer in phase with the 50 Hz to 60 Hz sine wave from the grid. For the designed IC, this is achieved with the circuit shown in Fig. 7, which is based on [15], [16]

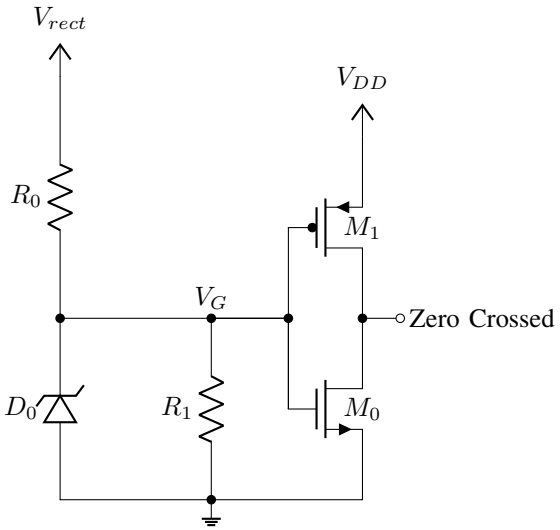

Fig. 7. Zero Crossing Detector

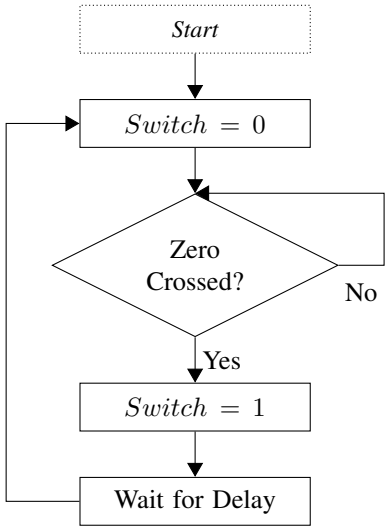

Fig. 8. Flow chart for the control logic of a leading edge dimmer.

Where D_0 is a $5\,\mathrm{V}$ Zenner diode, R_0 is an integrated $1\,\mathrm{M\Omega}$ rpolyd resistor, R_1 is an integrated $500\,\mathrm{k\Omega}$ rpwelld resistor, M_0 is a low voltage NMOS transistor, and M_1 is a low voltage PMOS transistor. Both MOS transistors have their bulk connected to their source. V_{DD} connects to the V_5 output of the Power System from Fig. 6 that provides a fixed voltage of $5\,\mathrm{V}$, and V_{rect} connects to the V_{rect} terminal of the Switches block from Fig. 4.

For values of V_{rect} close to zero, V_G will behave as a voltage divider between R_0 and R_1, and diode D_0 will have no effect. Since M_0 and M_1 act as a logical inverter, the value of $Zero\ Crossed$ will be equal to that of the V_{DD} terminal.

As the value of V_{rect} increases, there will be a point at which the value of V_G is larger than the threshold of the $M_0 - M_1$ inverter and the value of $Zero\ Crossed$ will abruptly go to $0\,\mathrm{V}$.

For very large values of V_{rect}, at which the (R_0, R_1) voltage divider would result in values of V_G larger than that of V_{DD}, diode D_0 will come into play limiting the V_G voltage to $5\,\mathrm{V}$ and preventing damage to M_0, M_1.

E. Control Logic

To fully implement a dimmer, as it would be necessary for a commercial product, some control logic would be needed to manage the turning on and off of the switches as described in Section II-A.

The simplest possible design would consist of a leading edge dimmer, which can be implemented to follow the flowchart presented in Fig. 8 with two digital inputs ($Zero\ Crossed$, $Delay$) and one digital output $Switch$.

$Zero\ Crossed$ is the output of the circuit described in Section II-D, and $Delay$ would be a multi-bit digital input to specify the dimmer duty cycle. Digital output $Switches$ represents the desired state of V_G of the switches described in Section II-A.

This flowchart could easily be translated into a FSM, and, if a clock signal is given, the delay block can easily be implemented with a standard digital counter.

A trailing edge dimmer can also be implemented with slight modifications to Fig. 8.

Because this circuit can be implemented with a standard low power microprocessor [11] and presents no particular challenge from being implemented in a UHV technology, the implementation of this block was left for a future design stage.

III. Simulations

A. Power Management System

A transient simulation of a power up sequence was done for the power management system shown in Fig. 6 for both low and high power modes. In both cases, the $5\,\mathrm{V}$ source was loaded with a $100\,\mathrm{k\Omega}$ resistor to emulate the current consumption of a low power microprocessor. The results are shown in Fig. 9.

As can be seen in in Fig. 9, low power mode is considerably slower, since the capacitors are charging at a lower current. In both cases, the circuit converges to the target voltage levels of $5\,\mathrm{V}$ and $15\,\mathrm{V}$.

B. Zero Crossing Detector

A transient simulation was performed for the zero crossing detector circuit shown in Fig. 7. The results are shown in Fig. 10.

As can be seen in Fig. 10, the zero crossing detector output behaves as expected, giving a high value only when the rectified AC signal is near zero.

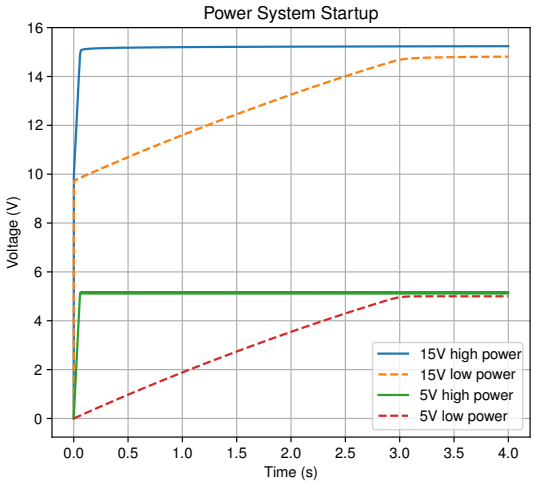

Fig. 9. Power management circuit startup transient simulation for low and high power mode.

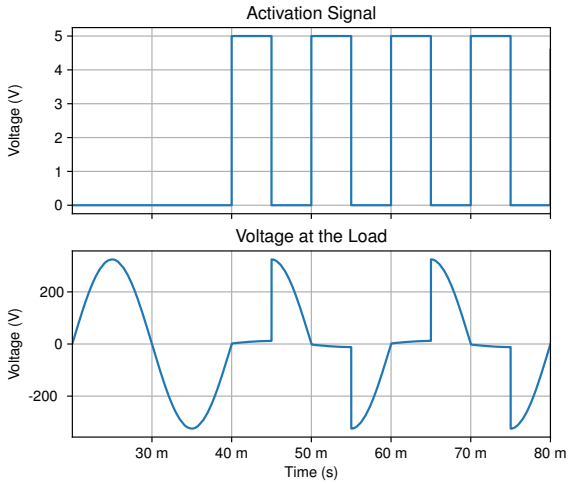

Fig. 11. Top level transient simulation for the UHV dimmer.

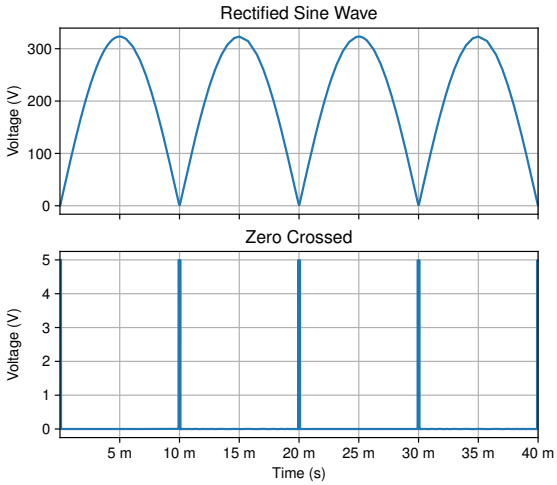

Fig. 10. Zero Crossing detector transient simulation.

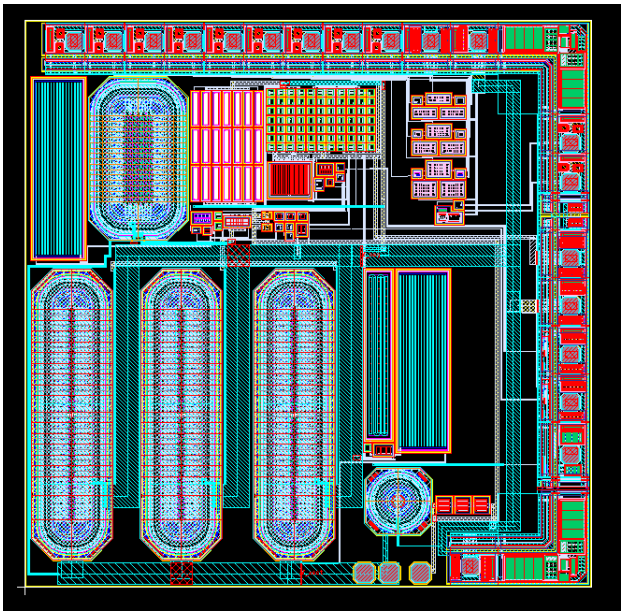

Fig. 12. Top level layout of the UHV dimmer.

C. Top Level Circuit

A transient simulation was performed at top level for the whole design with the same configuration as shown in Fig. 1, Fig. 2. The results are shown in Fig 11.

As it can be seen by comparing Fig. 2 and Fig. 11, voltage seen by the AC load is extremely similar to the expected behavior.

IV. Layout

The layout for the proposed implementation of the dimmer can be found on Fig. 12.

The switches are the three large devices on the lower left, the power management system is directly above the switches (resistor R_0 and M_1 from Fig. 6 can be seen at the upper left corner), and the zero crossing detector is at the center right (of which resistors R_0 and R_1 are distinguishable). The gate driver is at the top center section, but its smaller area makes it difficult to distinguish at top level.

On the top, right and bottom borders, the Input-Output (IO) blocks and ESD protections were placed following the manufacturer guidelines.

As recommended by the manufacturer, all UHV nets were routed using the highest metal offered by the technology because of its drastically higher conductivity and electromigration limits.

The devices on the upper right section, as well as most of the IO blocks on the top and right borders correspond to

a different, unrelated project and are not part of the UHV dimmer.

The total die area used by the IC is $10\,\mathrm{mm}^2$, of which $6.5\,\mathrm{mm}^2$ are occupied by the dimmer itself.

V. Conclusion

In this work, an integrated circuit with UHV switches, a gate driver, a power management system and a zero crossing detector was designed and simulated, aimed at functioning as a phase cut dimmer. Performance of the circuit was per expectations, as shown in Fig. 11.

The initial goal of designing a fully integrated phase cut dimmer could not be met, because of current density limitations of integrated UHV diodes, and the high value capacitors required by the power system.

In future design iterations, the logic related circuits could be integrated, which will produce a lower current consumption and could lessen the required capacitance values.

The ASIC was sent to be fabricated on a MPW in September 2019.

VI. Acknowledgment

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